Name:_____R-Number:_____

ECE4375/5375-001 Microprocessor Architecture
HW2

Write Verilog code to create the logic diagram shown below. It is required that you create the logic circuit below by creating a total of 4 modules. A module for a 2 input NAND gate, a module for a 2 input NOR gate, a module for a three input AND gate, and another Verilog module to instantiate the previous three modules and wire them together. Additionally, create a testbench to extract the truth table of the circuit. Submit all 4 Verilog files with your code along with the testbench file and the truth table obtained (Don't ZIP or consolidate the files in any way before uploading. Upload individually).