MADVLSI Mini-Project 2

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Submission files: https://github.com/JonahSpicher/VLSI-MP2

Schematic Capture and Simulation

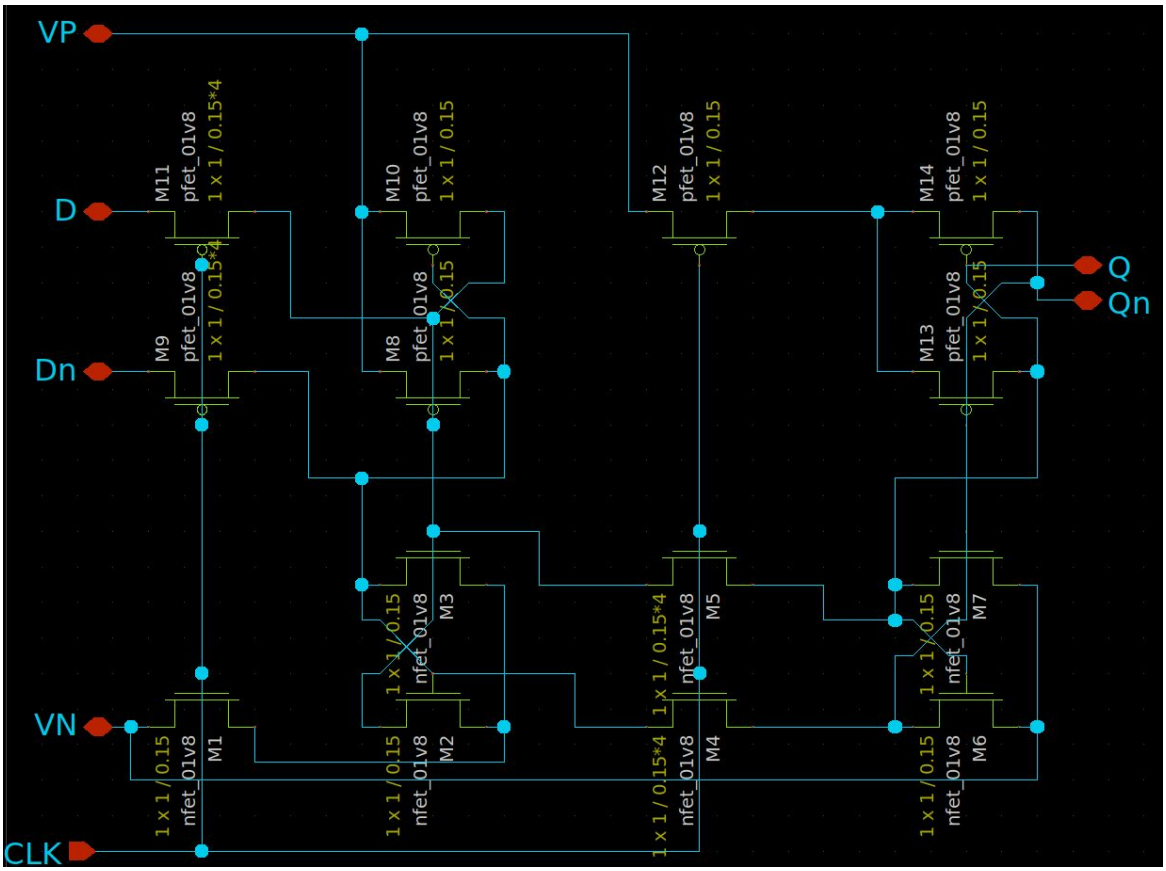

Figure 1: A CRSL D Flip Flop

This schematic shows the circuit the assignment centered around, a CRSL latch based D flip flop. This schematic is designed with layout in mind, so there are relatively few crossings and transistors are lined up vertically where possible. In order to avoid the problems with backwards current flow through the access transistors (here M1, M9, M4, and M5), I set their length to be 4 times the standard. The main difference between the layout suggested here and the eventual layout in magic is that some transistors were squished to the left to save space, so the vertical alignment was not as consistent as it is here, and M1 was placed in the 2nd row from the bottom instead of the lowest.

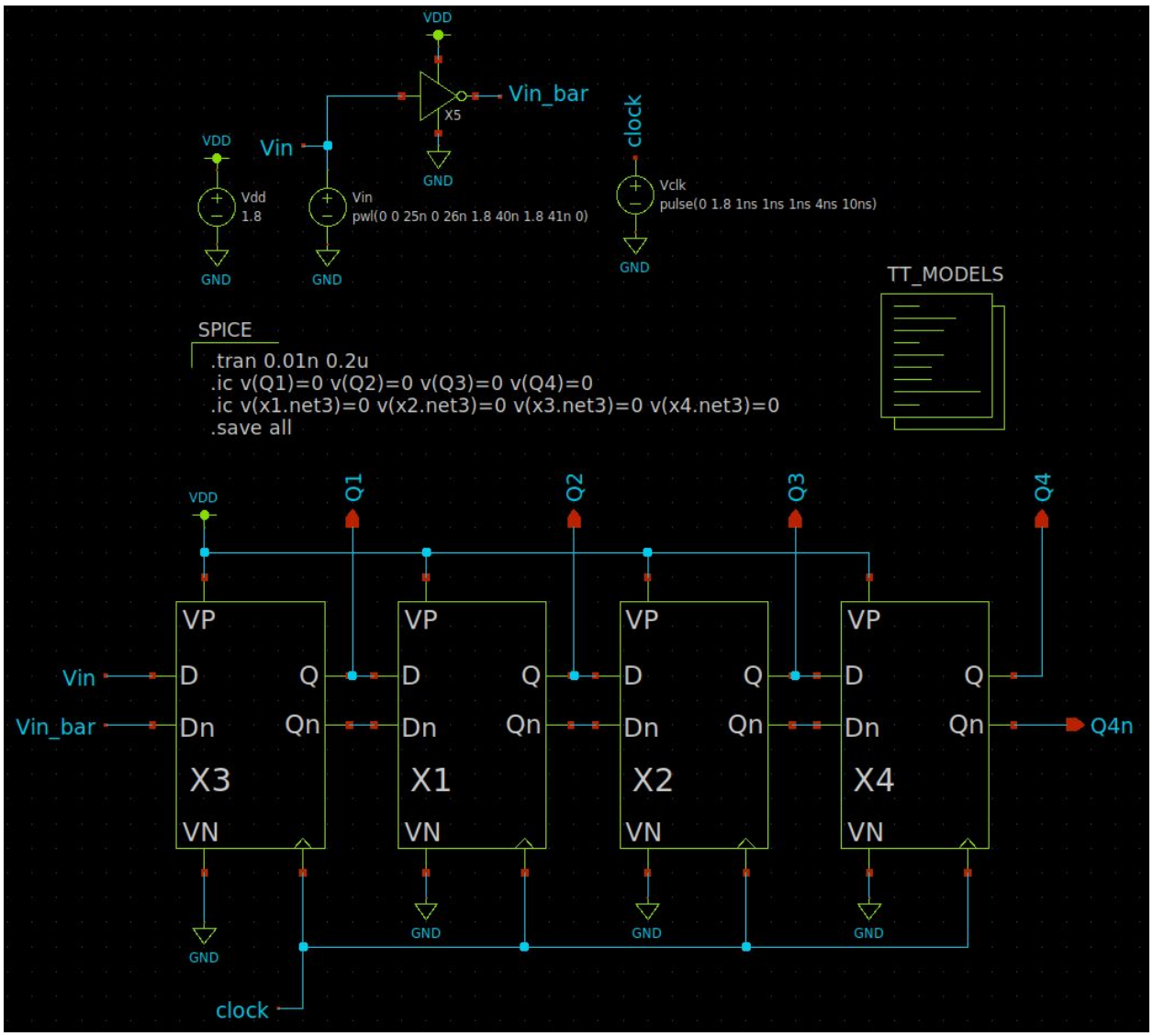

Figure 2: Test Harness Schematic for 4 bit Shift Register

To adapt the D flip flop into a shift register, I placed four of them side by side and routed each intermediate node up to an output. In order to test this device, I connected the clock to a pulsing voltage source and the first D input to a voltage source set to pulse on once and then turn off. In this test, I used the typical models and initialized each node in the bistable elements to be 0, as shown in the tutorials. Note that this is not the file I saved to the shiftreg_xschem.spice file shown in the LVS section, as that file lacks the test harness and spice simulation code.

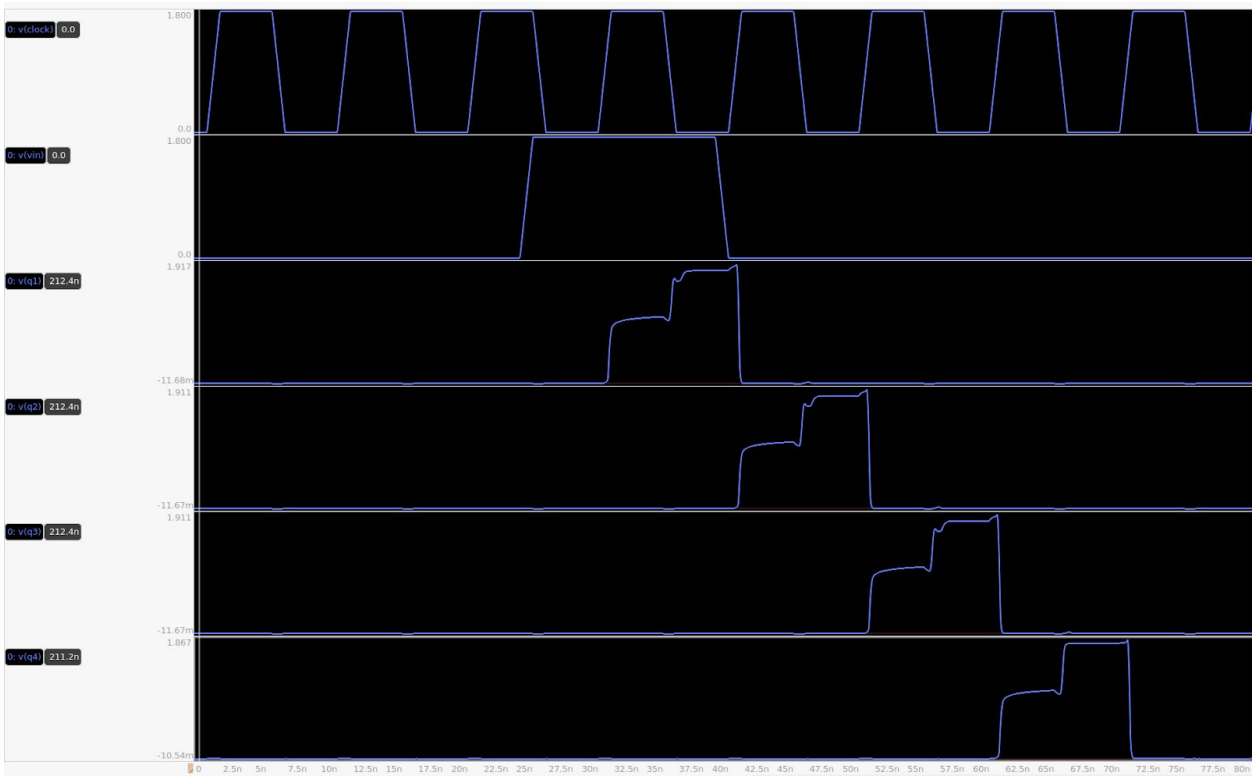

Figure 3: 4-bit Shift Register Test Results

The results were disappointing. The top window shows the clock, then the input, and then each successive stage in the shift register. It is immediately obvious that the D flip-flops are unable to pull high all the way when they should, and so the clean square pulse that went into the shift register is rendered as two separate steps up to high, once at the rising clock edge and once at the next falling clock edge. I repeated a similar test on a single D flip flop, and the same pattern showed up there. To try to fix this, I changed strength ratios some in order to try to correct this, as I assumed I had misinterpreted the instructions in Sivilotti's paper, but I was unable to make any noticeable changes in the output. I am pretty unclear on what went wrong here, and would have loved to figure it out, but due to time constraints I had to move on.

Layout Design

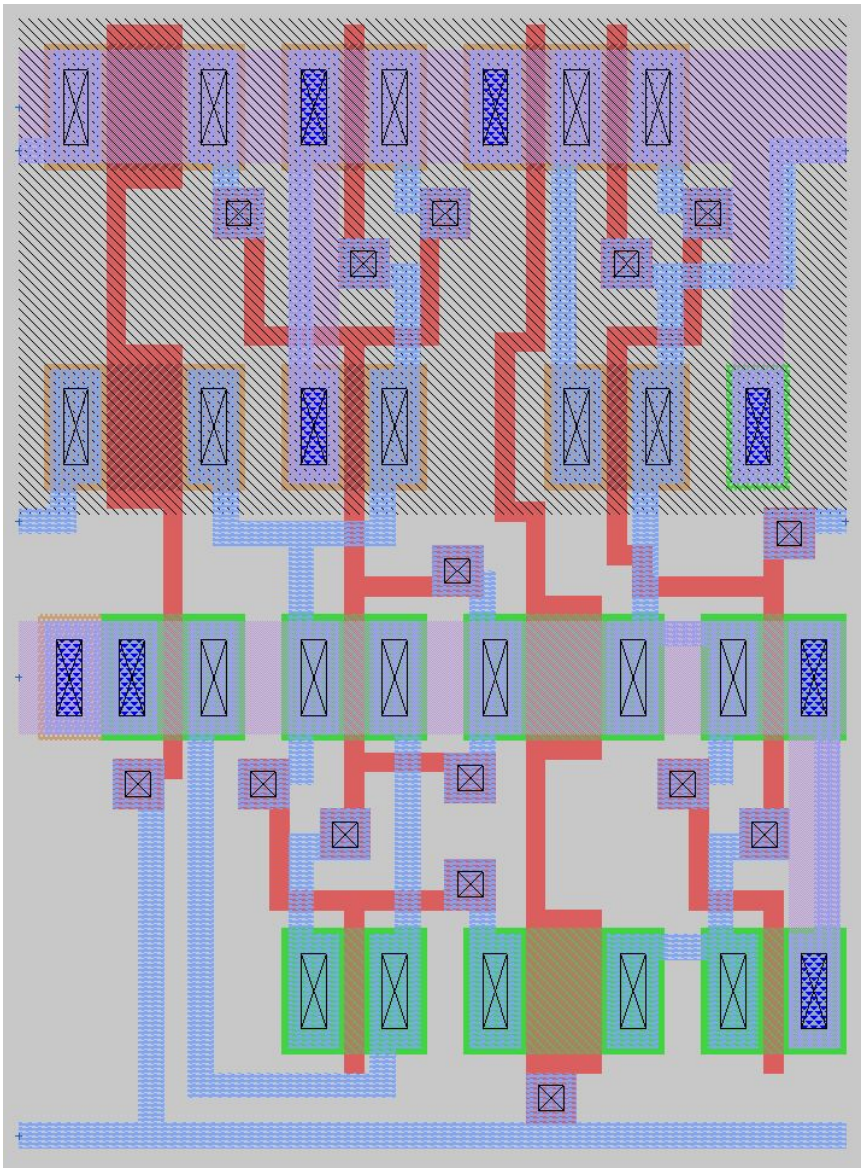

Figure 4: Layout For a Single D flip flop

This image shows the layout for the schematic in Figure 1. From top to bottom, the inputs are VP on the metal1 strip across the top, then D on the local interconnect underneath this metal, then Dn on the local interconnect just below the nwell boundary, then ground on the metal1 strip in the center of the circuit, and finally the clock on the strip of metal along the bottom of the cell. This cell has a pitch of 6.6 um. Note the lengthened transistors connecting the nodes of the two bistable elements on the top left and bottom center. Because there was extra space on the top on the right, I placed the well contact there and connected it to power with a branch off the metal1 strip along the top. This may have been unnecessary, but I was unsure if the well contact could go immediately next to a transistor not connected to Vdd.

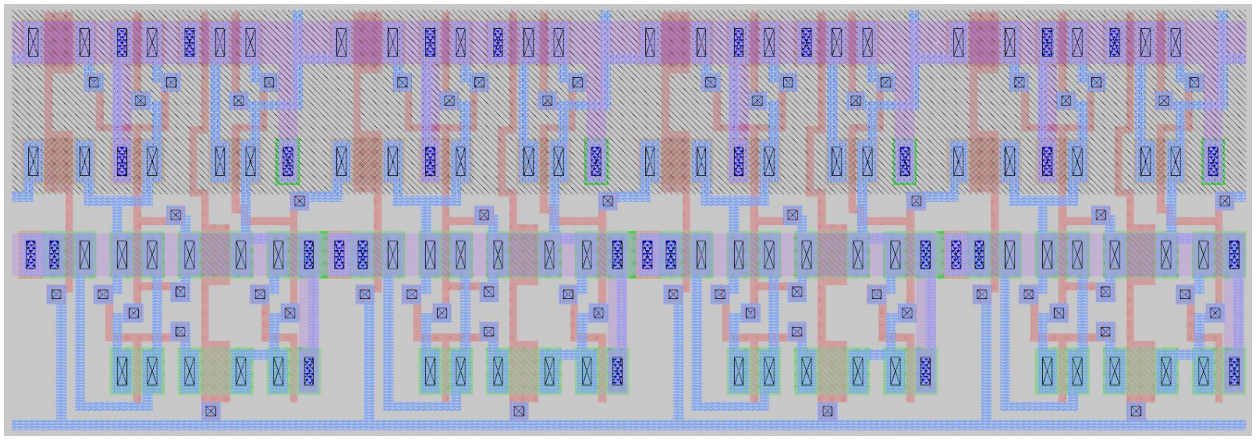

Figure 5: Layout for 4-bit Shift Register

The cells were simple to connect, because each input and output reach the edge of the cell at the correct height. One adjustment was required, which was to connect the row of transistors 2nd from the bottom with n diffusion. This connects the well contact to the previous grounded transistor source, but does not add any width to the total cell. This means that the total width came out to 26.4 um.

Layout Versus Schematic

Results of the LVS comparison are shown below. I bolded the relevant lines for convenience. The output showed that the two were identical at this level (and the cell level).

```
(base) jonah@jonah-MS-7C56:~/VLSI/MP2/layout$ lvs shiftreg.spice
shiftreg_xschem.spice
Netgen 1.5.166 compiled on Tue 16 Feb 2021 09:36:23 AM MST
Warning: netgen command 'format' use fully-qualified name
'::netgen::format'
Warning: netgen command 'global' use fully-qualified name
'::netgen::global'
Reading netlist file shiftreg.spice
Call to undefined subcircuit sky130_fd_pr__pfet_01v8
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_pr__nfet_01v8
Creating placeholder cell definition.
Reading netlist file shiftreg_xschem.spice
Call to undefined subcircuit CSRL
Creating placeholder cell definition.
```

```
Call to undefined subcircuit sky130_fd_pr__nfet_01v8
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_pr__pfet_01v8
Creating placeholder cell definition.
Cell shiftreg_xschem.spice:  Net GND changed to global
Cell CSRL:  Net GND changed to global
Cell shiftreg_xschem.spice:  Net VDD changed to global
Cell CSRL:  Net VDD changed to global
Reading setup file
/home/jonah/skywater/open_pdks/sky130/sky130A/libs.tech/netgen/sky130A
_setup.tcl
Model sky130_fd_pr__nfet_01v8 pin 1 == 3
No property mult found for device sky130_fd_pr__nfet_01v8
No property sa found for device sky130_fd_pr__nfet_01v8
No property sb found for device sky130_fd_pr__nfet_01v8
No property sd found for device sky130_fd_pr__nfet_01v8
No property nf found for device sky130_fd_pr__nfet_01v8
No property nrd found for device sky130_fd_pr__nfet_01v8
No property nrs found for device sky130_fd_pr__nfet_01v8
Model sky130_fd_pr__nfet_01v8 pin 1 == 3
Model sky130_fd_pr__pfet_01v8 pin 1 == 3
No property mult found for device sky130_fd_pr__pfet_01v8
No property sa found for device sky130_fd_pr__pfet_01v8
No property sb found for device sky130_fd_pr__pfet_01v8
No property sd found for device sky130_fd_pr__pfet_01v8
No property nf found for device sky130_fd_pr__pfet_01v8
No property nrd found for device sky130_fd_pr__pfet_01v8
No property nrs found for device sky130_fd_pr__pfet_01v8
Model sky130_fd_pr__pfet_01v8 pin 1 == 3
Comparison output logged to file comp.out
Logging to file "comp.out" enabled
Contents of circuit 1:  Circuit: 'sky130_fd_pr__pfet_01v8'
Circuit sky130_fd_pr__pfet_01v8 contains 0 device instances.
Circuit contains 0 nets.
Contents of circuit 2:  Circuit: 'sky130_fd_pr__pfet_01v8'
Circuit sky130_fd_pr__pfet_01v8 contains 0 device instances.
Circuit contains 0 nets.

Circuit sky130_fd_pr__pfet_01v8 contains no devices.
Contents of circuit 1:  Circuit: 'sky130_fd_pr__nfet_01v8'
```

```
Circuit sky130_fd_pr__nfet_01v8 contains 0 device instances.
Circuit contains 0 nets.
Contents of circuit 2:  Circuit: 'sky130_fd_pr__nfet_01v8'
Circuit sky130_fd_pr__nfet_01v8 contains 0 device instances.
Circuit contains 0 nets.

Circuit sky130_fd_pr__nfet_01v8 contains no devices.
Contents of circuit 1:  Circuit: 'CSRL'
Circuit CSRL contains 14 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   7
  Class: sky130_fd_pr__pfet_01v8 instances:   7
Circuit contains 11 nets.
Contents of circuit 2:  Circuit: 'CSRL'
Circuit CSRL contains 14 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   7
  Class: sky130_fd_pr__pfet_01v8 instances:   7
Circuit contains 13 nets.

Circuit 1 contains 14 devices, Circuit 2 contains 14 devices.
Circuit 1 contains 11 nets,Circuit 2 contains 13 nets. *** MISMATCH
***

  Flattening non-matched subcircuits CSRL CSRL
Flattening instances of CSRL in file shiftreg.spice
Flattening instances of CSRL in file shiftreg_xschem.spice
Contents of circuit 1:  Circuit: 'shiftreg.spice'
Circuit shiftreg.spice contains 56 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  28
  Class: sky130_fd_pr__pfet_01v8 instances:  28
Circuit contains 29 nets.
Contents of circuit 2:  Circuit: 'shiftreg_xschem.spice'
Circuit shiftreg_xschem.spice contains 56 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  28
  Class: sky130_fd_pr__pfet_01v8 instances:  28
Circuit contains 29 nets.

Circuit 1 contains 56 devices, Circuit 2 contains 56 devices.
Circuit 1 contains 29 nets,Circuit 2 contains 29 nets.

Circuits match with 33 symmetries.
```

Resolving automorphisms by property value.
Resolving automorphisms by pin name.
Netlists match uniquely.
Circuits match correctly.
Result: Circuits match uniquely.
Logging to file "comp.out" disabled
LVS Done.