MADVLSI Mini-Project 3

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Github Repository: https://github.com/JonahSpicher/VLSI-MP3

Circuit Summary

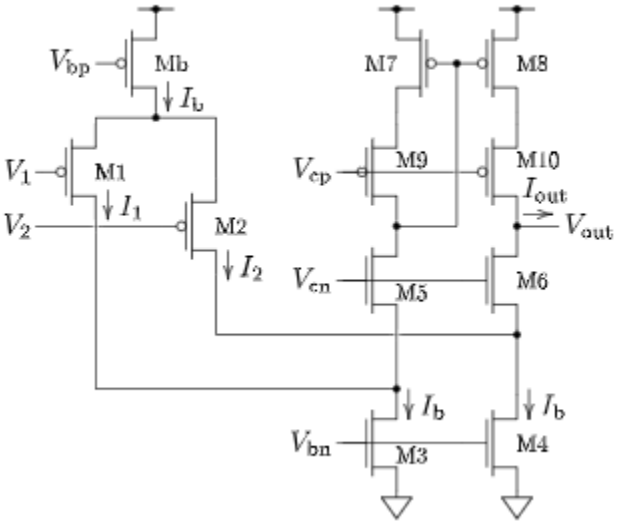

Figure 1: The folded-cascode differential amplifier

1.

a. In this circuit, a folded cascode differential amplifier, the input V_1 is noninverting and the input V_2 is inverting. To show why, we can imagine what happens if both inputs are decreased while everything else is held steady. If V_1 decreases, then the differential pair M1 and M2 will start drawing more current down the M1 branch as the source to gate voltage increases, meaning I_2 will decrease and I_1 will increase. An increase in I_1 means that the current flowing through M5 (we can call this I_5) will decrease as the voltage on its source increases. This decrease in I_5 is reflected across the current mirror, decreasing the current out of M10. This will in turn lower I_{out} and also V_{out}. This means that lowering V_1 lowered V_{out}, so V_1 is non-inverting.

   For V_2, the explanation is simpler. Lower V_2 increases I_2. An increase in I_2 causes a decrease in the current exiting M6, which causes I_{out} (and therefore V_{out}) to increase as less of the current from the current mirror can travel through M6. Here, V_2 was lowered and V_{out} was increased, so V_2 is inverting.

b. V_1 and V_2 should be set so that $\min(V_1, V_2) >= V_{bp} - V_{SDsat}/\kappa$. This means that the lower of the two voltages should be greater than the bias voltage minus the saturation voltage of the pMOS, divided by κ. This allows both a large enough source to drain voltage on the bias transistor to keep it saturated and a large enough source to gate voltage to pass through a substantial amount of the bias current.
c. We can follow the flow of current through the circuit to get that $I_{out} = I_2 - I_1$. This assumes that $I_3=I_4=I_b$, which lets us simplify the current in the current mirror to be equal to I_2.
d. If we don't assume anything about I_3 and I_4, we get that the current expression above is $I_{out} = I_2 - I_1 + I_3 - I_4$. If $I_3 = I_4 = I_c$, it doesn't matter what level they are, they should cancel as far as the output is concerned. In order for this to work, though, I_c must be greater than or equal to I_b so that enough current is pulled from M5 to keep it in saturation.
e. The circuit below is a standard cascode bias voltage generator, laid out (at a higher level of abstraction than was actually used in the project) to mesh well with the fcdiffamp cell design. By making M3 and M8 out of 16 very narrow subdevices they can be placed above and below the cells to reduce width at a smaller cost to height. The nmos cells are placed above the pmos here, which allows the nwell areas to be closer together, allowing less space between the two cells, as well as putting the positive voltage metal1 strips very near each other and reducing clutter in connections. In the actual layout and schematic, the position of the outputs and input currents was changed to better map to their location in the fcdiffamp cell.

   The circuit takes in two currents, I_1 (through the pins in the center in this image) and I_b (through the V_{bn} and V_{bp} pins). These generate both the bias voltages through a current mirror and the cascode voltages.

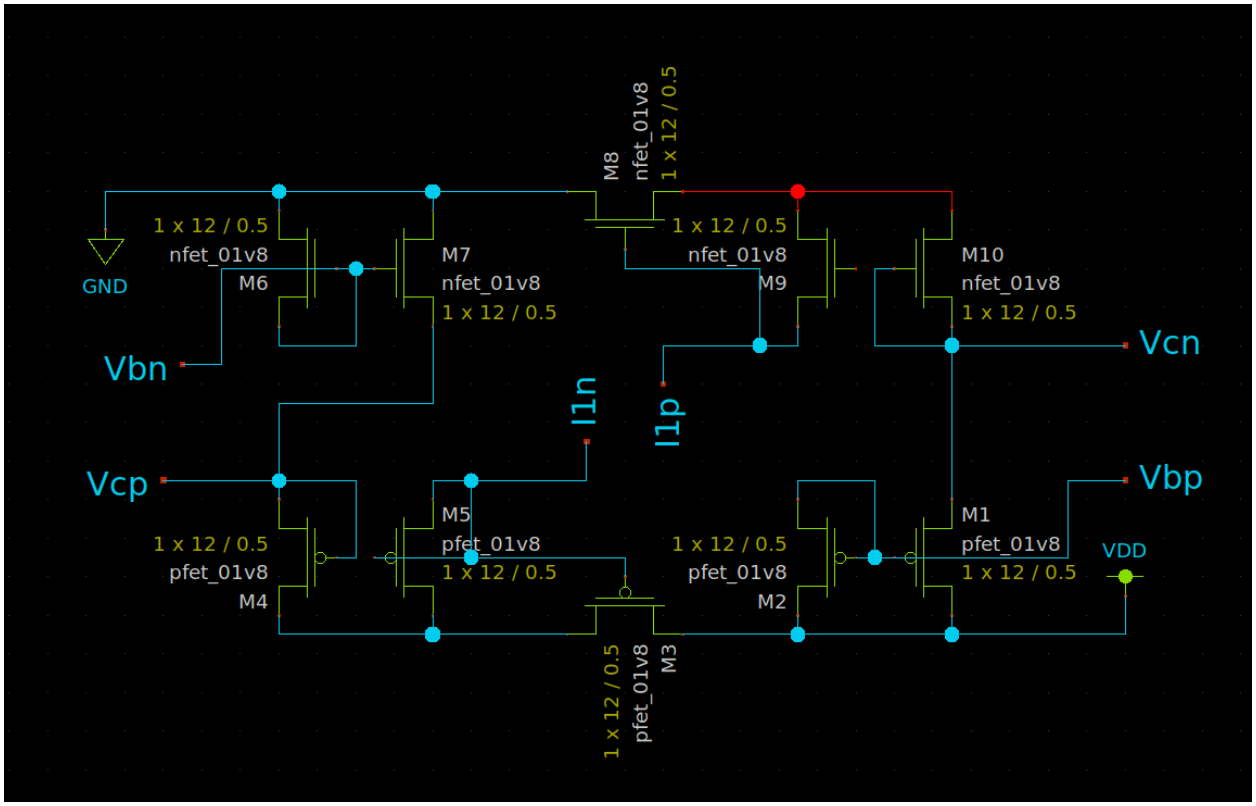

Figure 2: Cascode and bias voltage generation circuit

Schematic Capture and Simulation

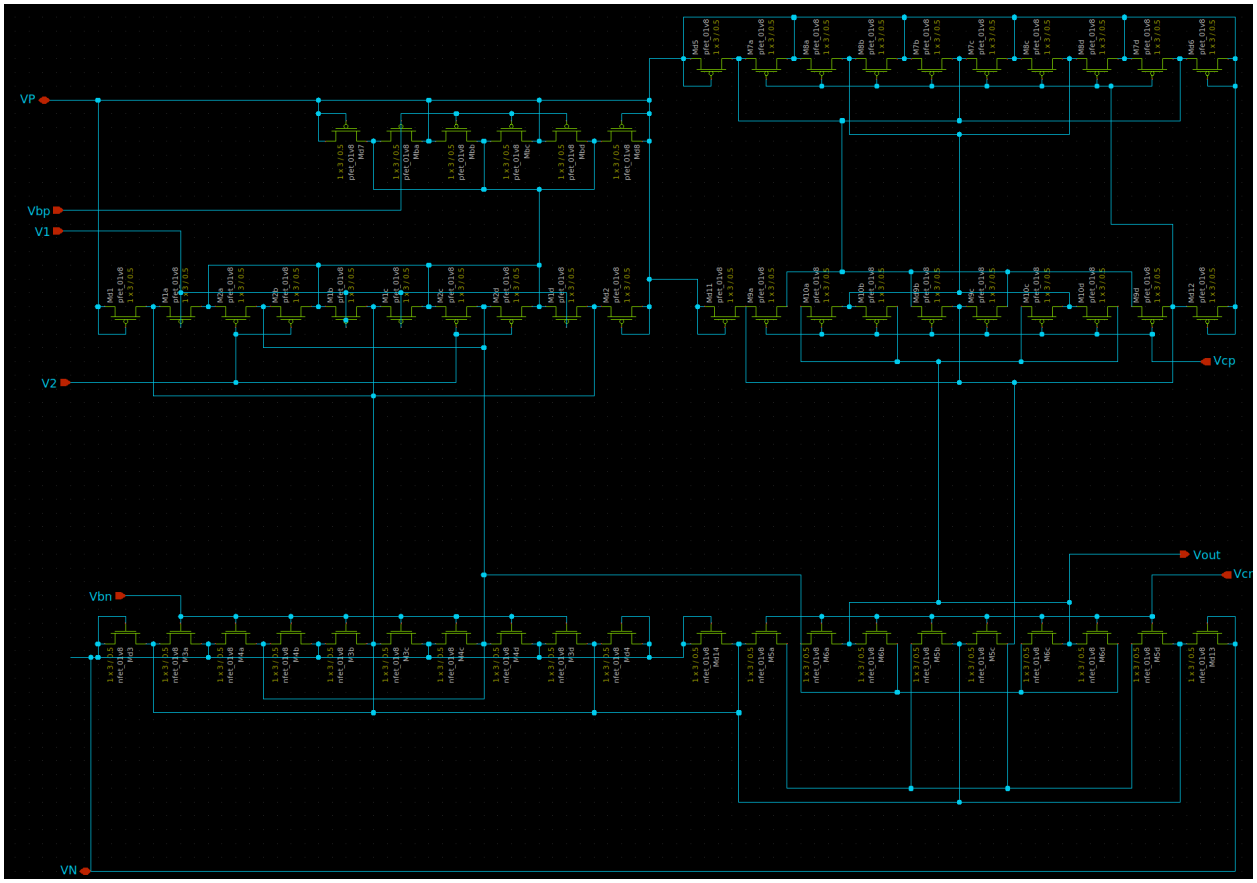

Figure 3: Schematic for the folded cascode differential amplifier

Bias current was chosen to be 10 uA, giving a GBP of 1,004,847.51 Hz.

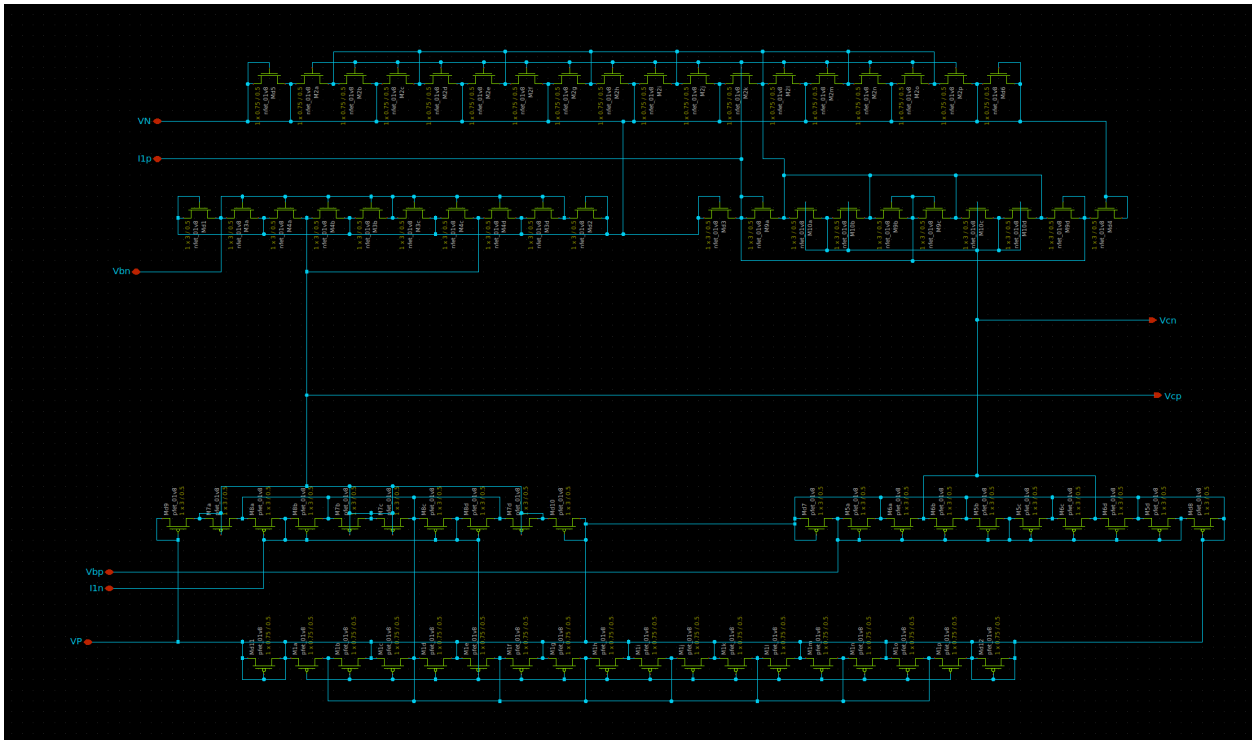

Figure 4: Schematic for bias voltage generation circuit

a. The DC gain was calculated from the curves below to be around 680 on average.

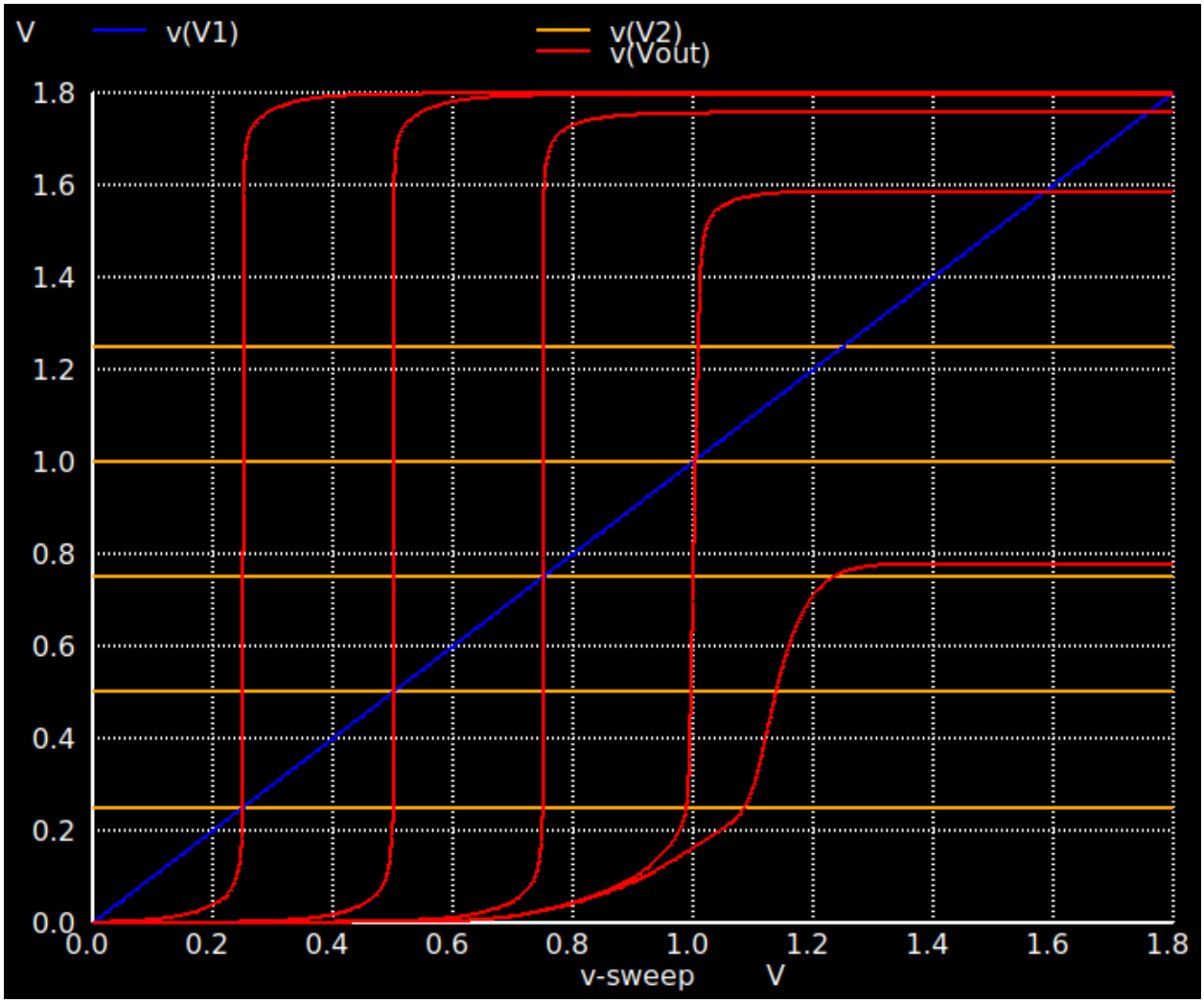

Figure 5: VTC's from 5 sweeps of V1. Notice the clear demonstration of the limits on the input voltages discussed in part b of the first problem.

b. For figure 6, the inverting input was set to 0.25V and the noninverting input was swept from 0 to 1.8 volts while V_{out} was held at 0.7V. The current is limited at about both positive and negative 8.85uA, a bit less than I_b, as expected. The incremental transconductance gain was calculated from this curve to be 18.389uS close to the transition point.

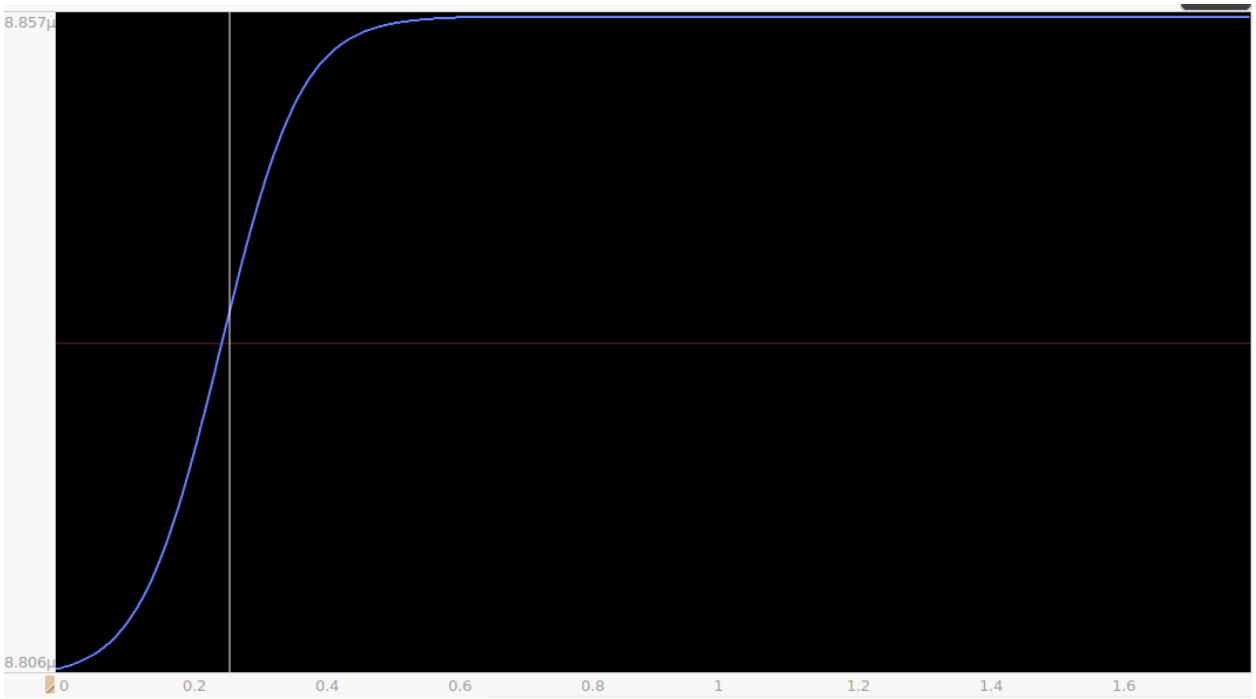

Figure 6: Voltage to current transfer characteristic

c. The loopgain plot shown in figure 6 suggests the low frequency loopgain is about 65 dB or about 1780, which is much higher than the gain was calculated to be in part a, though I am not sure why this is. The unity gain crossover frequency is at roughly 6 Mhz. I am not sure how to compare this to what i would expect from the transconductance gain and the load capacitance. If we try to find the time constant tau of a circuit with a capacitance 2 pF and transconductance of 18.389uS we get 0.10616us which implies that the frequency 9.419 Mhz is important to the circuit somehow, which is somewhat close to the unity gain crossover point (the gain at this point is about -5 dB). I am not sure if that is at all relevant, though.

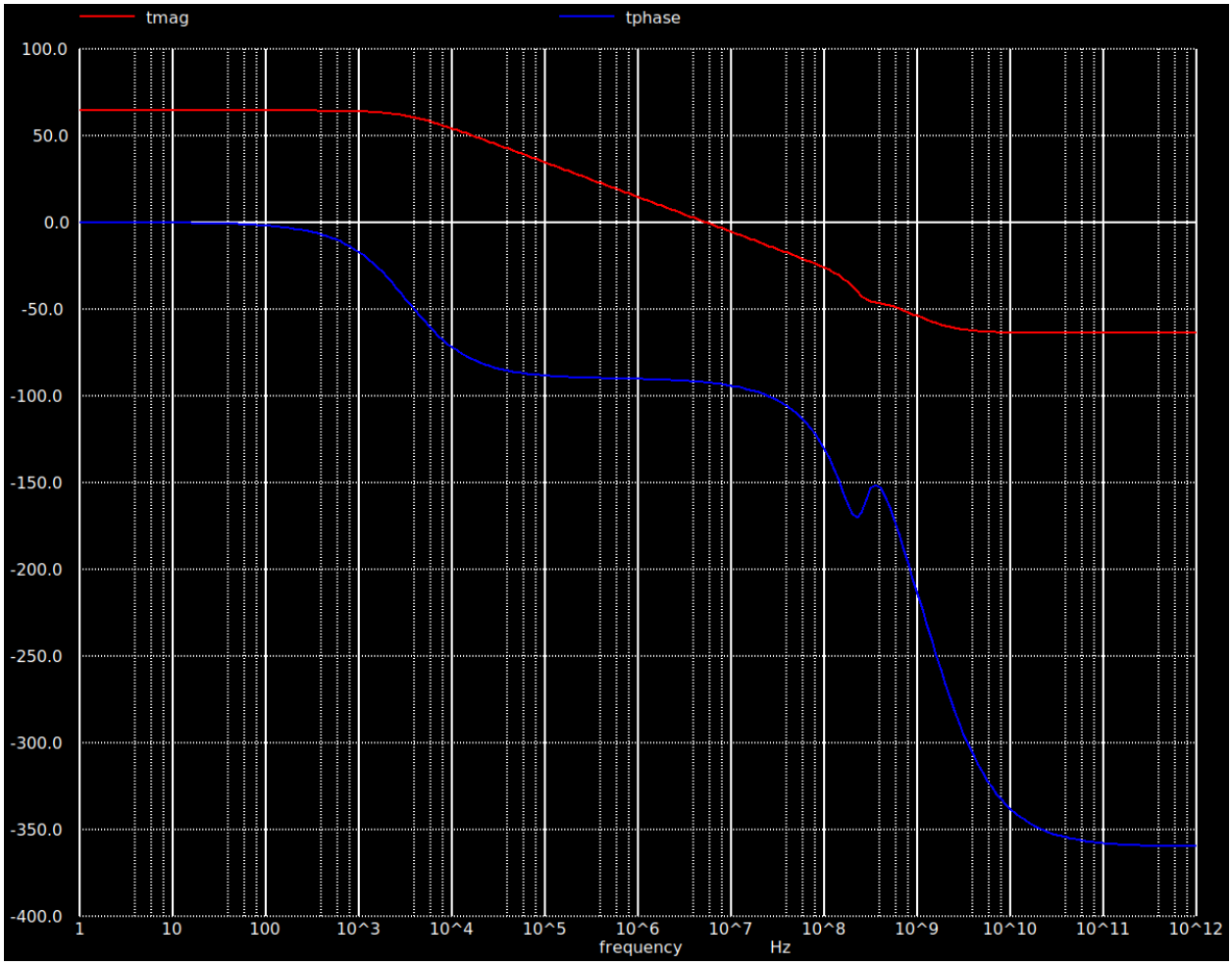

Figure 7: The loopgain and phase of the amplifier

d. Figure 8 shows the system response during AC analysis while configured as a follower. This shows unity gain up to around 1Mhz (which was used to set the bias current). The amplitude is at about -3 dB at the unity gain crossover point found during loopgain, which is as expected.

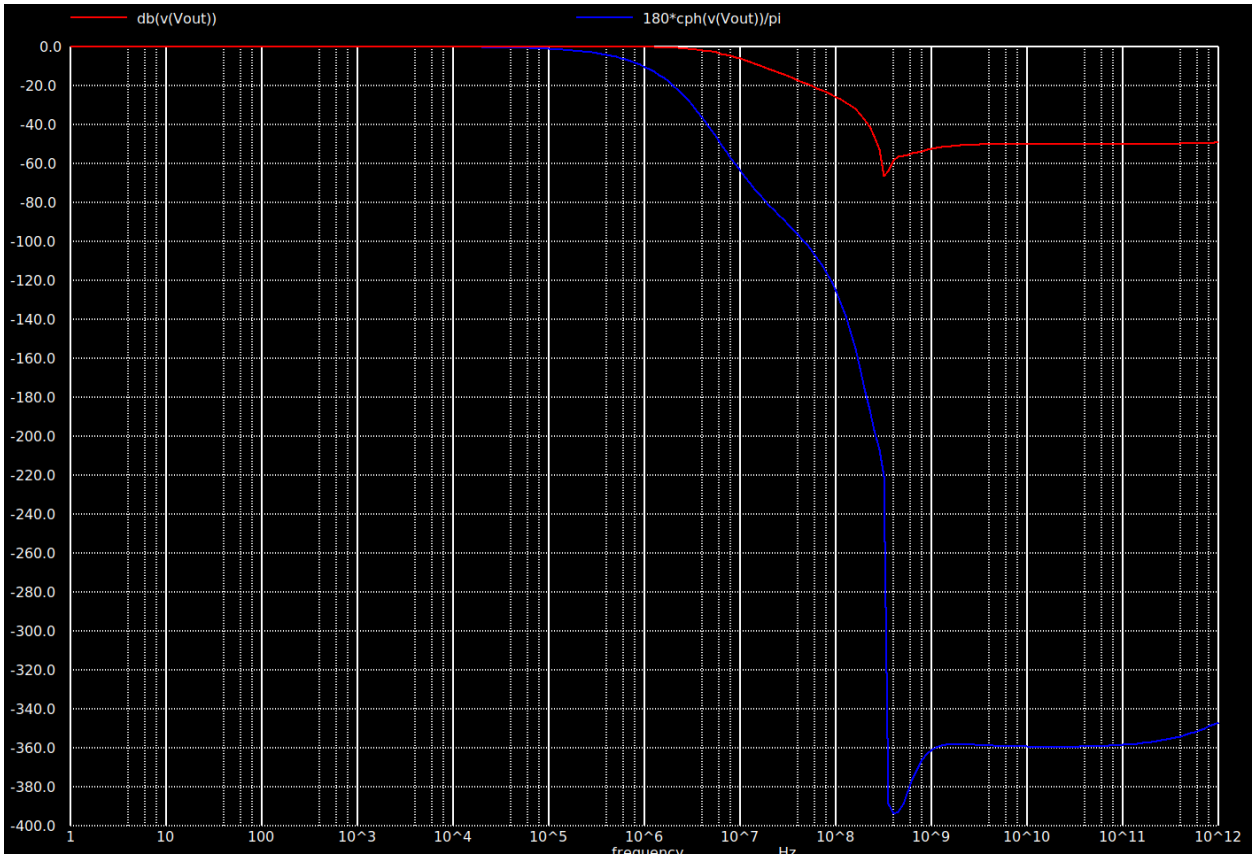

Figure 8: The amplitude and phase of V_{out} when configured as a follower.

d. For the small signal step analysis, a step of 1 mV was chosen and observed roughly linear behavior. I found the full transition period could be captured with a wait time of 1us, for a frequency of 500kHz. The figure is shown below. The time constant for the falling time was 38.13 ns, and the time constant for the rising time was almost exactly the same, at 40 ns. These time constants point to a higher frequency than the corner frequency, the corner frequency indicates a time constant which is about 2.7 times these time constants. This makes sense, as this would be the point where the signal would be roughly halfway to fully risen, and -3dB is roughly half power. They are not perfectly symmetrical, as the output voltage is consistently about 0.15 mV above the input voltage.

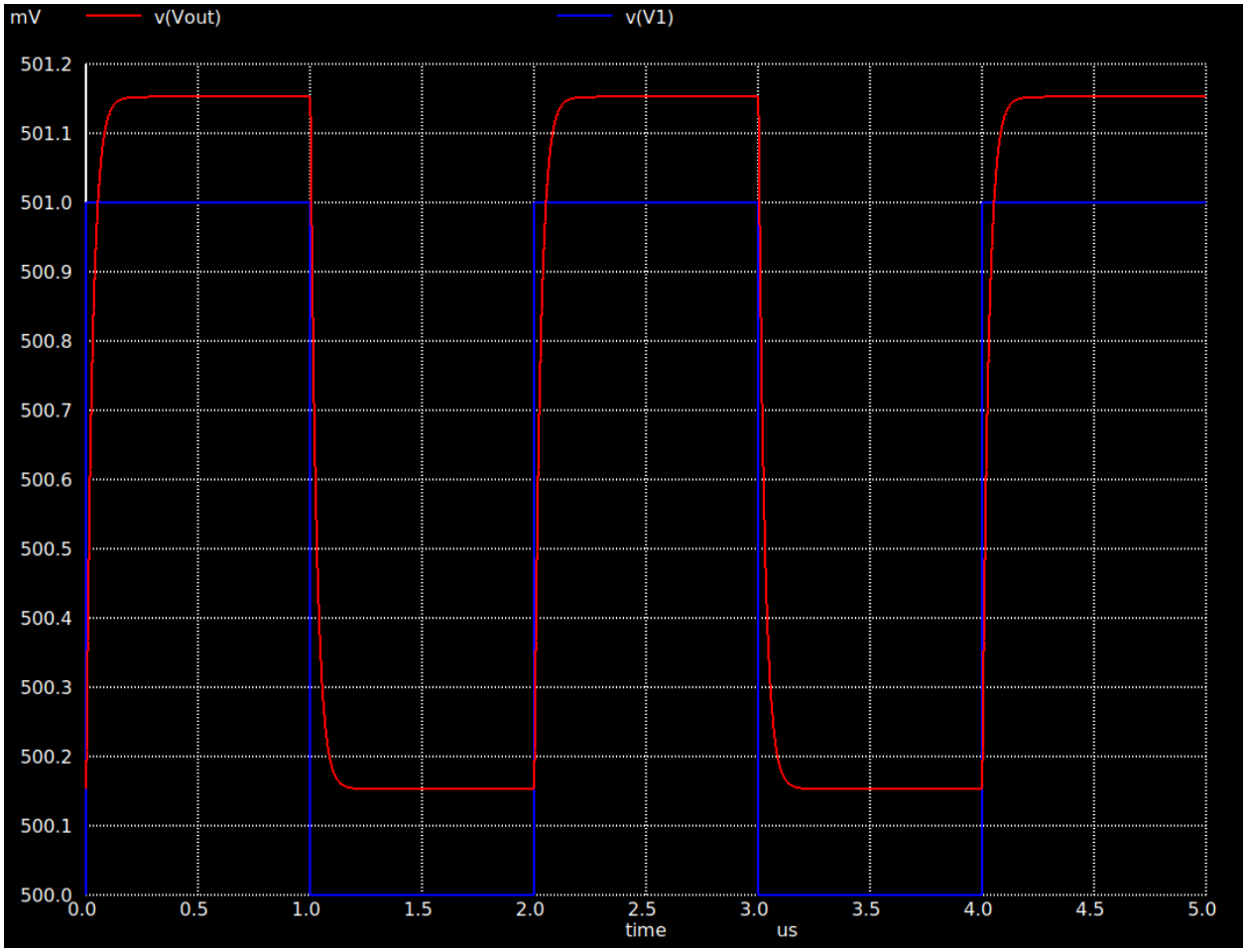

Figure 9: Small signal response of the circuit

e. Using a step size of 0.9V, This response is far from symmetrical. The rise time has a slew rate of 4.210519TV/s, while the falling time has a much lower slew rate of -4.354718 MV/s. However, the rising time slew rate is maintained for much less time, and V_{out} starts to fall off as it approaches the higher level. Multiplying the load capacitance and the max current limit gives an output very close to the falling time slew rate, 4.425 MV/s.

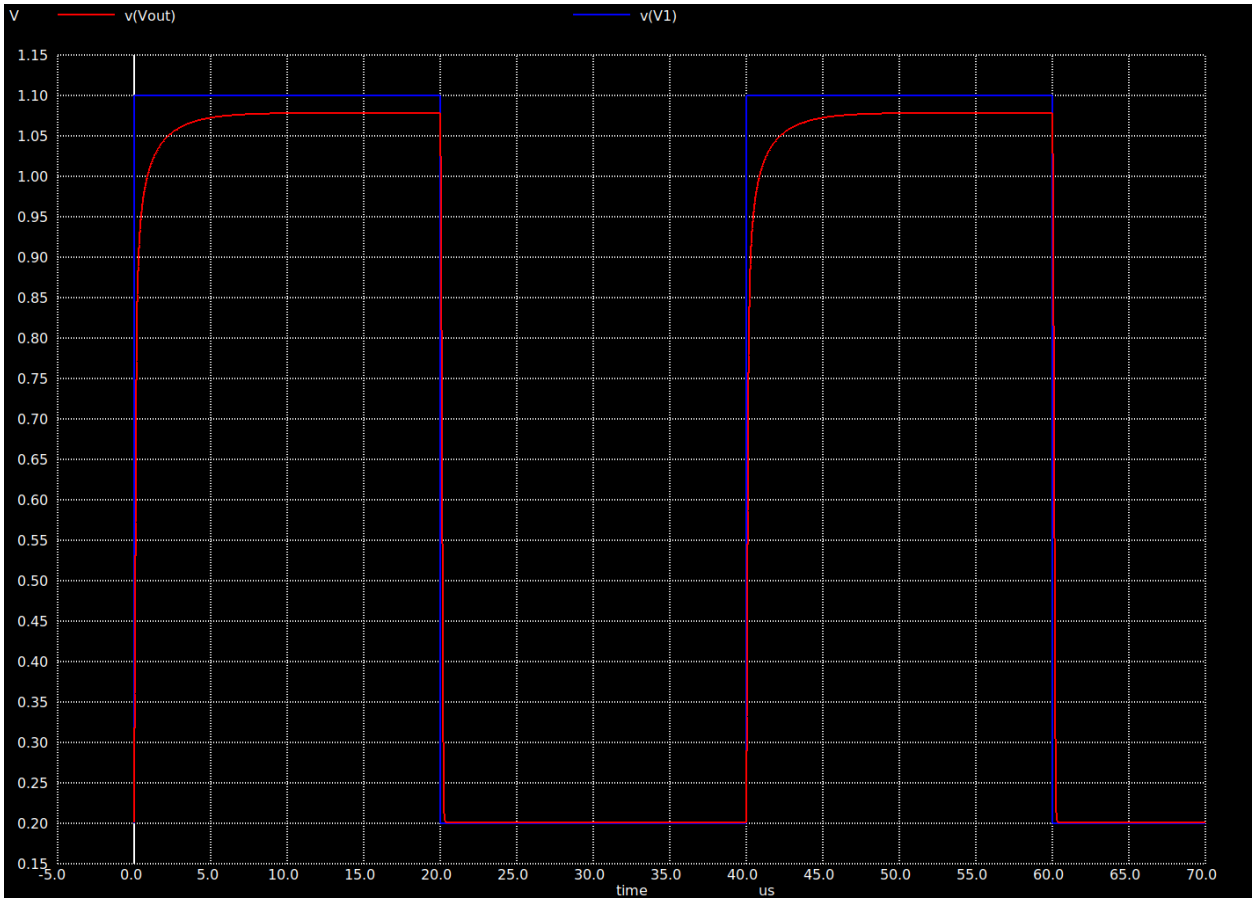

Figure 10: Large signal response of the circuit.

Layout Design

Showing images of the layouts would not be very practical here, but the cells are all in the github repo linked at the top of the report. The total size of the final cell is 25.50um x 28.55um. The inputs VP, VN, V1, V2, I1p, I1n, Vbp and Vbn (to supply a bias current) as well as the output are available in the metal 1 layer at the edges of the cell. All inputs are on the left, and the output is on the right.

Layout Versus Schematic

Below is the lvs output for the full schematic, which concludes that the layout matches the schematic.

```
(base) jonah@jonah-MS-7C56:~/VLSI/MP3/layout$ lvs full_fcdiff.spice
full_fcdiff_xschem.spice
Netgen 1.5.166 compiled on Tue 16 Feb 2021 09:36:23 AM MST
Warning: netgen command 'format' use fully-qualified name '::netgen::format'
```

```
Warning: netgen command 'global' use fully-qualified name '::netgen::global'
Reading netlist file full_fcdiff.spice
Call to undefined subcircuit sky130_fd_pr__nfet_01v8
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_pr__pfet_01v8
Creating placeholder cell definition.
Reading netlist file full_fcdiff_xschem.spice
Call to undefined subcircuit biasgen
Creating placeholder cell definition.
Call to undefined subcircuit fcdiffamp
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_pr__nfet_01v8
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_pr__pfet_01v8
Creating placeholder cell definition.
Cell full_fcdiff_xschem.spice:  Net VDD changed to global
Cell biasgen:  Net VDD changed to global
Cell fcdiffamp:  Net VDD changed to global
Cell full_fcdiff_xschem.spice:  Net GND changed to global
Cell biasgen:  Net GND changed to global
Cell fcdiffamp:  Net GND changed to global
Reading setup file
/home/jonah/skywater/open_pdks/sky130/sky130A/libs.tech/netgen/sky130A_setup.t
cl
Model sky130_fd_pr__nfet_01v8 pin 1 == 3
No property mult found for device sky130_fd_pr__nfet_01v8
No property sa found for device sky130_fd_pr__nfet_01v8
No property sb found for device sky130_fd_pr__nfet_01v8
No property sd found for device sky130_fd_pr__nfet_01v8
No property nf found for device sky130_fd_pr__nfet_01v8
No property nrd found for device sky130_fd_pr__nfet_01v8
No property nrs found for device sky130_fd_pr__nfet_01v8
Model sky130_fd_pr__nfet_01v8 pin 1 == 3
Model sky130_fd_pr__pfet_01v8 pin 1 == 3
No property mult found for device sky130_fd_pr__pfet_01v8
No property sa found for device sky130_fd_pr__pfet_01v8
No property sb found for device sky130_fd_pr__pfet_01v8
No property sd found for device sky130_fd_pr__pfet_01v8
No property nf found for device sky130_fd_pr__pfet_01v8
No property nrd found for device sky130_fd_pr__pfet_01v8
No property nrs found for device sky130_fd_pr__pfet_01v8
Model sky130_fd_pr__pfet_01v8 pin 1 == 3
Comparison output logged to file comp.out
Logging to file "comp.out" enabled
```

```
Contents of circuit 1:  Circuit: 'sky130_fd_pr__nfet_01v8'
Circuit sky130_fd_pr__nfet_01v8 contains 0 device instances.
Circuit contains 0 nets.
Contents of circuit 2:  Circuit: 'sky130_fd_pr__nfet_01v8'
Circuit sky130_fd_pr__nfet_01v8 contains 0 device instances.
Circuit contains 0 nets.

Circuit sky130_fd_pr__nfet_01v8 contains no devices.
Contents of circuit 1:  Circuit: 'sky130_fd_pr__pfet_01v8'
Circuit sky130_fd_pr__pfet_01v8 contains 0 device instances.
Circuit contains 0 nets.
Contents of circuit 2:  Circuit: 'sky130_fd_pr__pfet_01v8'
Circuit sky130_fd_pr__pfet_01v8 contains 0 device instances.
Circuit contains 0 nets.

Circuit sky130_fd_pr__pfet_01v8 contains no devices.
Contents of circuit 1:  Circuit: 'biasgen'
Circuit biasgen contains 76 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  38
  Class: sky130_fd_pr__pfet_01v8 instances:  38
Circuit contains 10 nets.
Contents of circuit 2:  Circuit: 'biasgen'
Circuit biasgen contains 76 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  38
  Class: sky130_fd_pr__pfet_01v8 instances:  38
Circuit contains 12 nets.

Circuit was modified by parallel/series device merging.
New circuit summary:

Contents of circuit 1:  Circuit: 'biasgen'
Circuit biasgen contains 16 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   8
  Class: sky130_fd_pr__pfet_01v8 instances:   8
Circuit contains 10 nets.
Contents of circuit 2:  Circuit: 'biasgen'
Circuit biasgen contains 16 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   8
  Class: sky130_fd_pr__pfet_01v8 instances:   8
Circuit contains 12 nets.

Circuit 1 contains 16 devices, Circuit 2 contains 16 devices.
Circuit 1 contains 10 nets,   Circuit 2 contains 12 nets. *** MISMATCH ***
```

```
  Flattening non-matched subcircuits biasgen biasgen
Flattening instances of biasgen in file full_fcdiff.spice
Flattening instances of biasgen in file full_fcdiff_xschem.spice
Contents of circuit 1:  Circuit: 'fcdiffamp'
Circuit fcdiffamp contains 56 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  20
  Class: sky130_fd_pr__pfet_01v8 instances:  36
Circuit contains 15 nets.
Contents of circuit 2:  Circuit: 'fcdiffamp'
Circuit fcdiffamp contains 56 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  20
  Class: sky130_fd_pr__pfet_01v8 instances:  36
Circuit contains 17 nets.

Circuit was modified by parallel/series device merging.
New circuit summary:

Contents of circuit 1:  Circuit: 'fcdiffamp'
Circuit fcdiffamp contains 16 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   5
  Class: sky130_fd_pr__pfet_01v8 instances:  11
Circuit contains 15 nets.
Contents of circuit 2:  Circuit: 'fcdiffamp'
Circuit fcdiffamp contains 16 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   5
  Class: sky130_fd_pr__pfet_01v8 instances:  11
Circuit contains 17 nets.

Circuit 1 contains 16 devices, Circuit 2 contains 16 devices.
Circuit 1 contains 15 nets,   Circuit 2 contains 17 nets. *** MISMATCH ***

  Flattening non-matched subcircuits fcdiffamp fcdiffamp
Flattening instances of fcdiffamp in file full_fcdiff.spice
Flattening instances of fcdiffamp in file full_fcdiff_xschem.spice
Contents of circuit 1:  Circuit: 'full_fcdiff.spice'
Circuit full_fcdiff.spice contains 32 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  13
  Class: sky130_fd_pr__pfet_01v8 instances:  19
Circuit contains 19 nets.
Contents of circuit 2:  Circuit: 'full_fcdiff_xschem.spice'
Circuit full_fcdiff_xschem.spice contains 32 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  13
  Class: sky130_fd_pr__pfet_01v8 instances:  19
Circuit contains 19 nets.
```

```
Circuit 1 contains 32 devices, Circuit 2 contains 32 devices.
Circuit 1 contains 19 nets,   Circuit 2 contains 19 nets.

Netlists match uniquely.
Result: Circuits match uniquely.
Logging to file "comp.out" disabled
LVS Done.
```