MADVLSI Mini-Project 4

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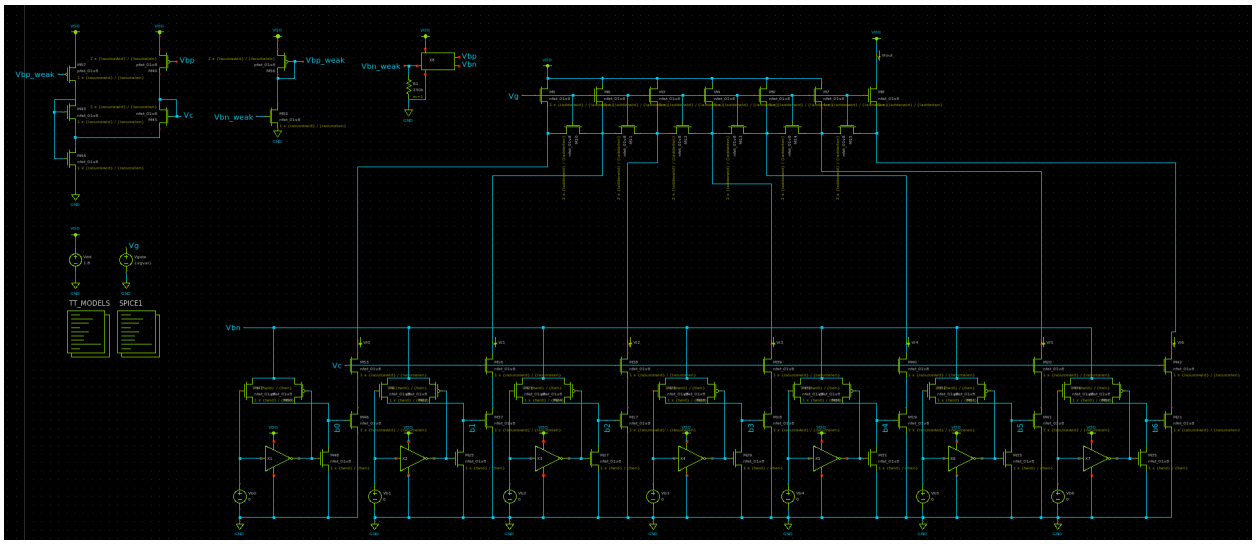
Github Repository: https://github.com/JonahSpicher/VLSI-MP4

Circuit Summary

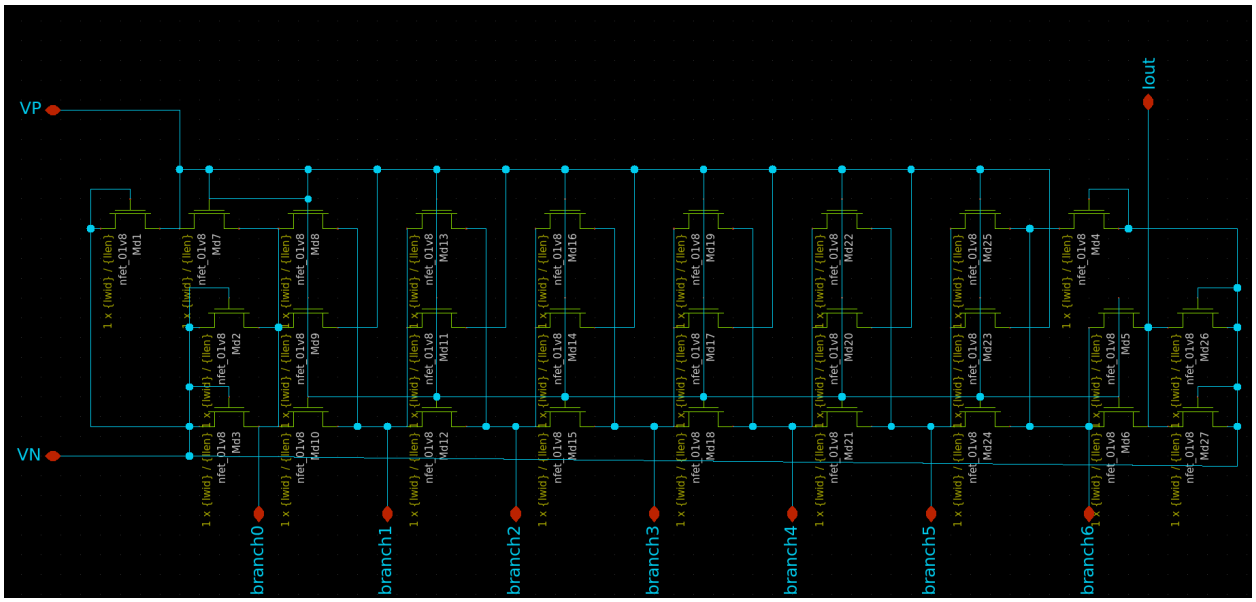
My Digital to Analog converter can be visualized with the following high level schematic:



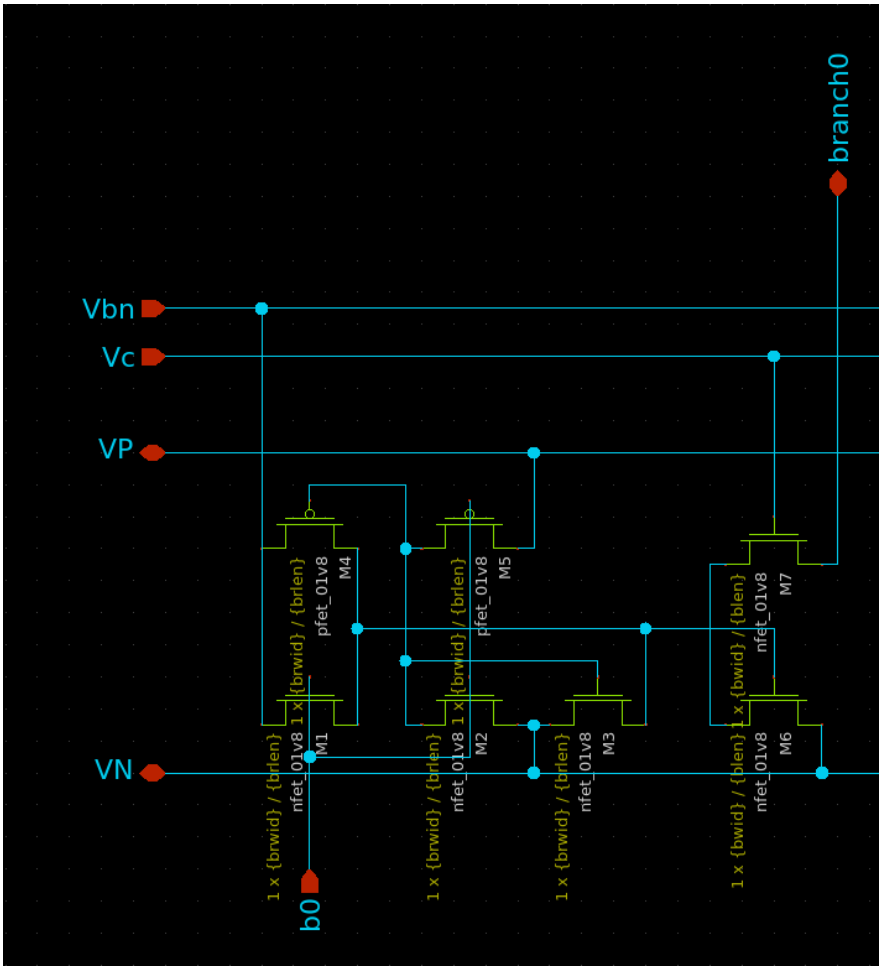
This circuit can be broken into three conceptual pieces: the ladder, the branch logic, and the bias generation circuit. The top left of the image contains the bias generation circuitry. This will be shown in more detail shortly, but this generates a consistent bias current used as a reference current by the ladder. To the right of this circuitry is the ladder, which has seven branches, each of which draws twice the output current of its neighbor when activated. At the bottom of the above image, the branch logic is made up of seven identical cells. Each of these cells consists of an inverter, a transmission gate, and a current mirror. The gate of the current mirror is connected either through the transmission gate to the bias voltage generated above or through an nMOS switch to ground. Seven control signals toggle each individual current mirror, allowing the ladder branches to be activated individually.

Schematic Capture and Simulation

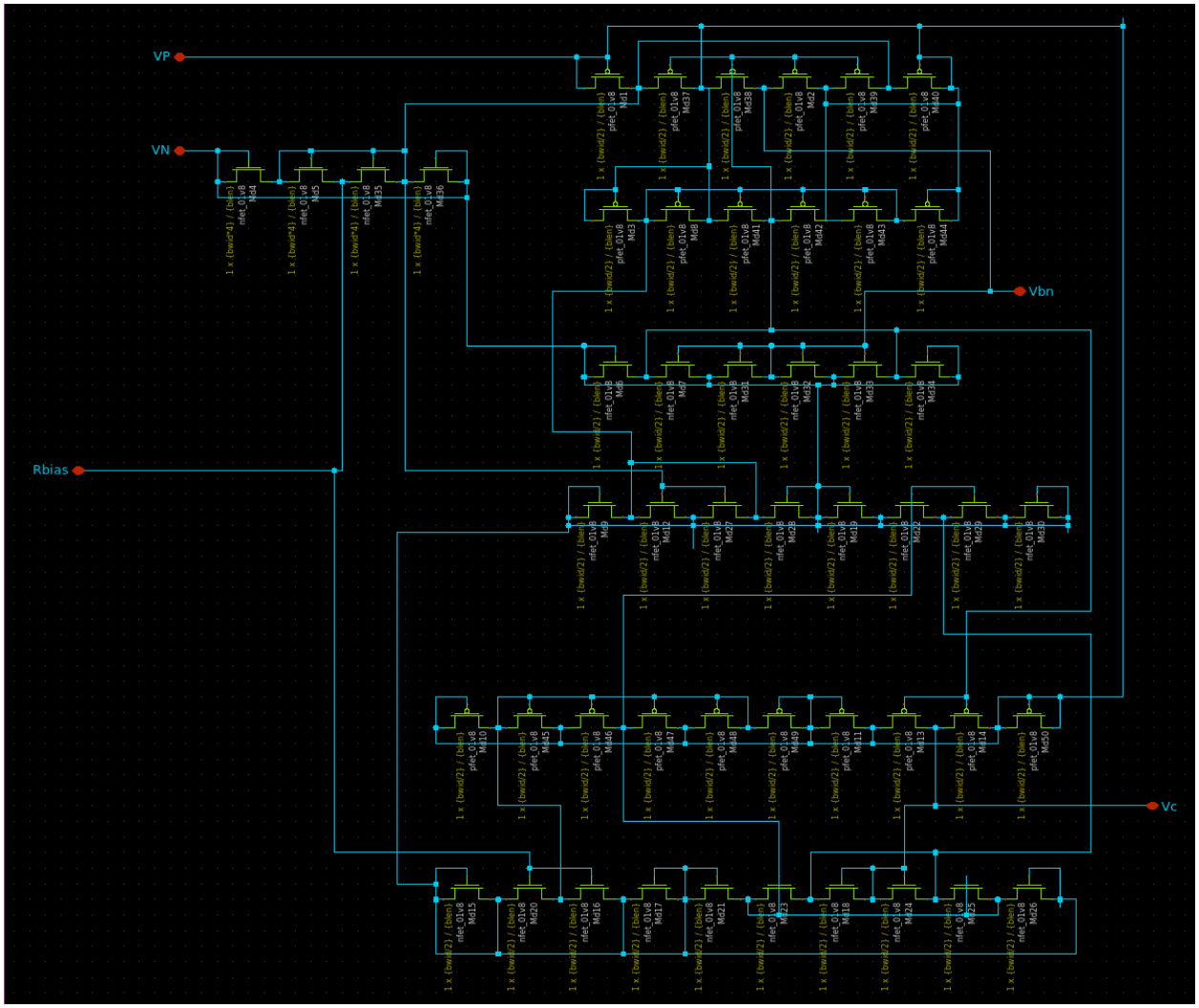
The full schematic design involved designing each of these three components as cells. Below are images of each cell.



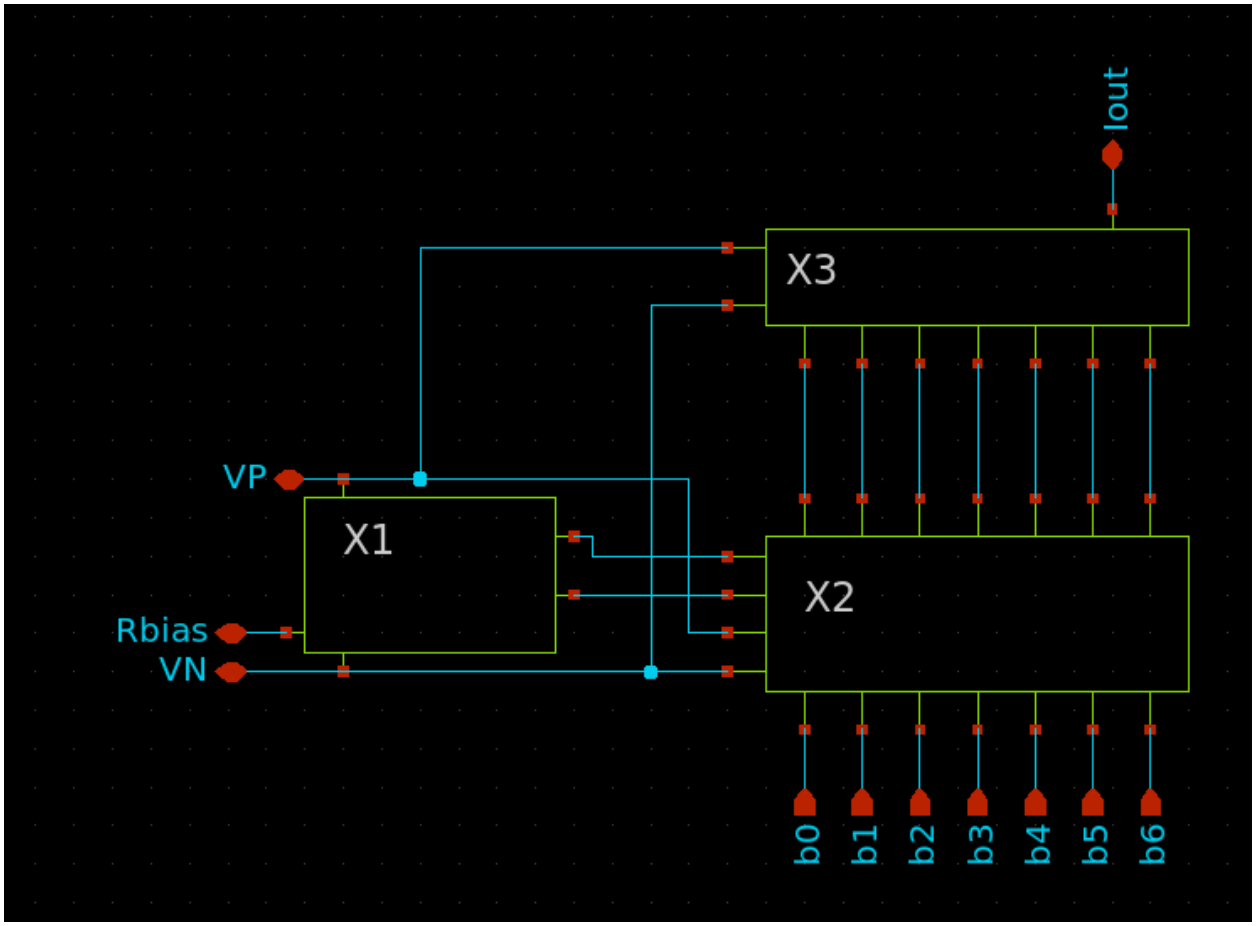
First, the above is the ladder. Each ladder subcell was implemented as three transistors, with the larger transistor (with a strength ratio twice the smaller one) surrounding the center transistor. This was done to give each cell a common centroid.



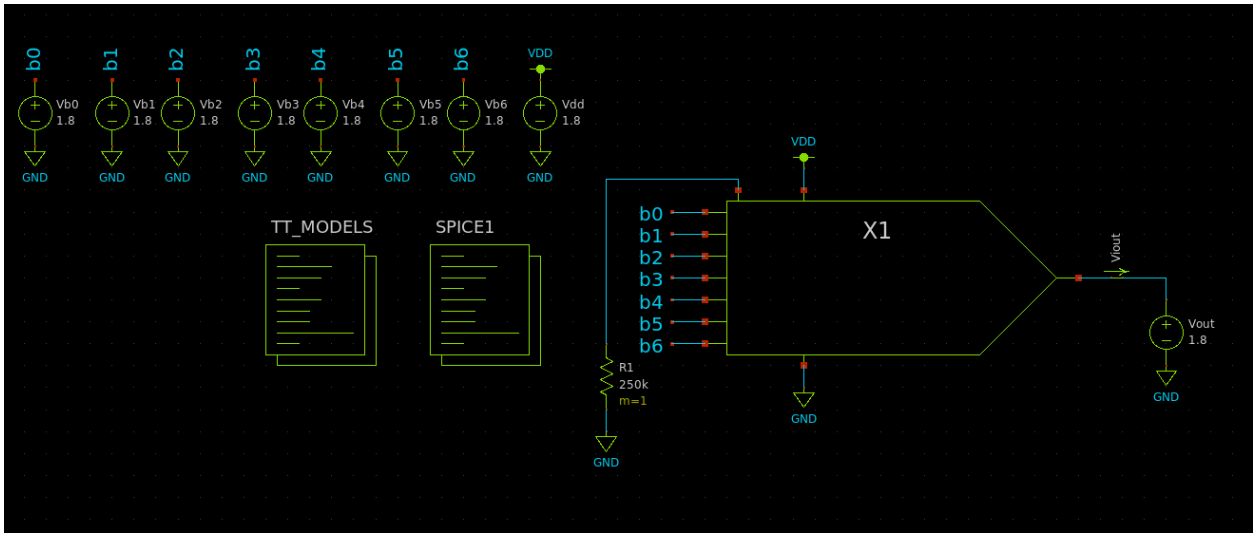
Next, this image is one cell of the branch logic mentioned in the first section. An inverter passes the b0 logic signal to the pMOS gate in the transmission gate, while b0 itself activates the nMOS. The inverted version of b0 also activates the nMOS switch pulling the current mirror transistor to ground. A cascode transistor helps flatten the output curve of the current mirror, keeping the branch current more equivalent for each branch.



Finally, this circuit generates the bias voltages. This follows the design introduce in week 7, and gets very good results. This design does use one off chip resistor to generate the bias current. The asymmetry of this layout is somewhat offset by the fact that the transistors on the left in this image are 8 times larger than the transistors on the right. This will be more apparent in the layout images later.



The three components were connected as shown above, and this was the schematic used in LVS comparison. Finally, this circuit was tested using the harness below.



This harness was modified for some tests. An identical setup was used (only with MC_SWITCH=1) for Monte Carlo testing, while different code was used to test the consistency of I_{out} as V_{out} varies. In general, however, the setup above produced the graphs below. One

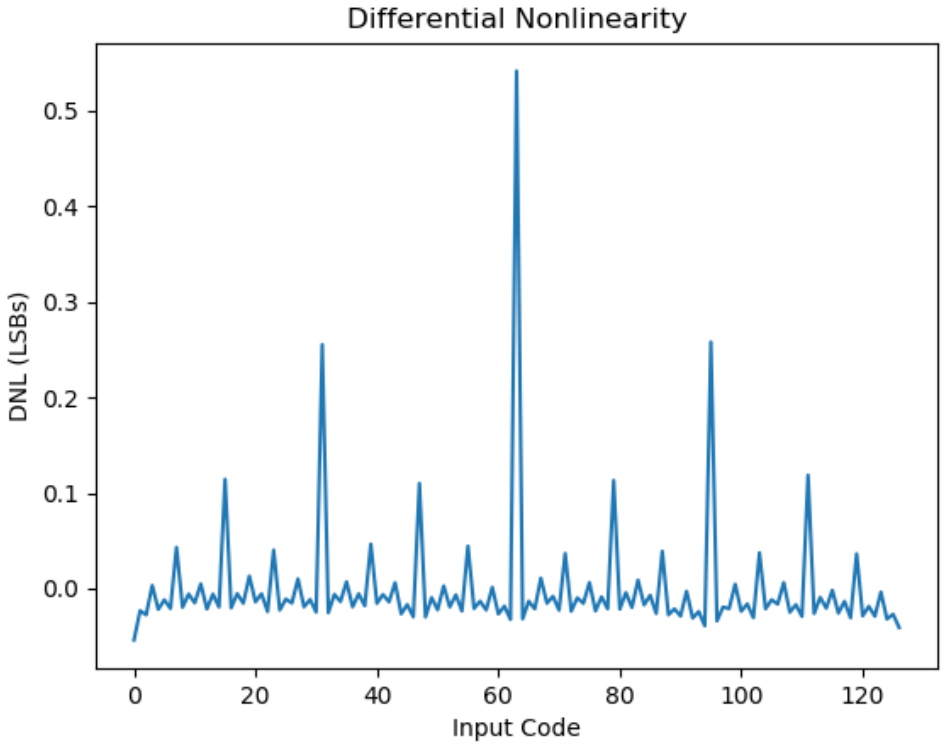
feature of these files to point out is that the width and length of the transistors is parameterized, so that changes to the design can be made quickly from the highest level. This allowed the design to be optimized for certain conditions with python (the code used to do this can be found in the opt folder in the github). In this code, the python script minimized a cost function which as inputs took a vector of transistor dimensions as well as the bias resistor value, modified a netlist file, ran ngspice with a .os call, and parsed the output for nonlinearity. In the version shown in plots below, the widths and lengths were as follows:

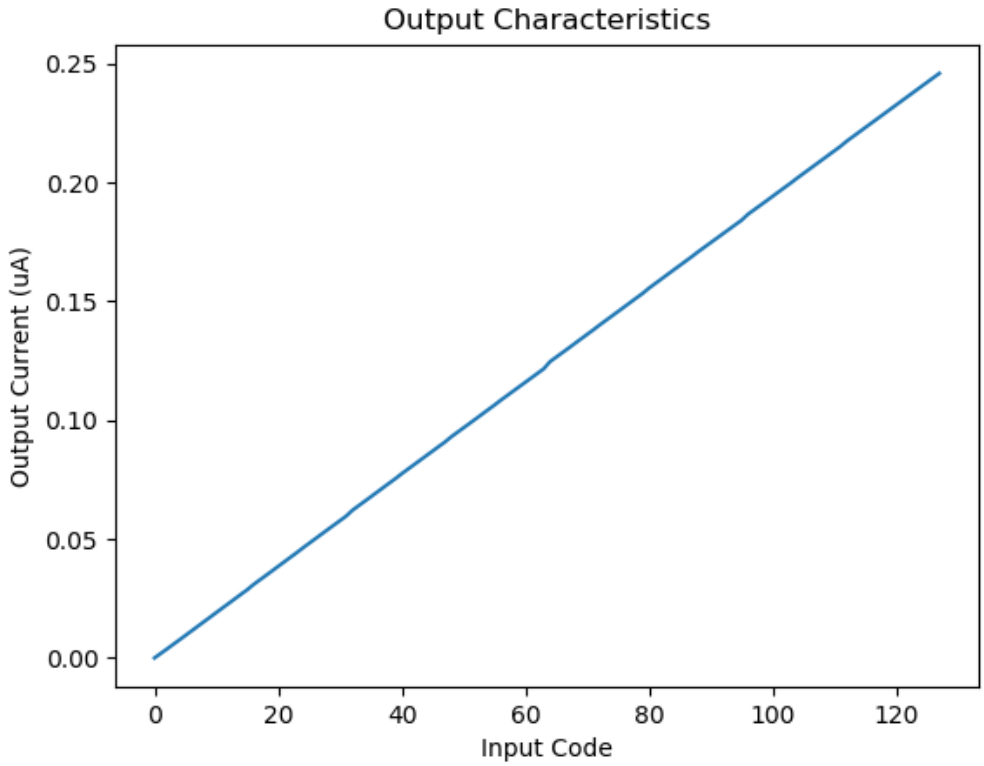
Ladder transistors:
- Length = 1.4um
- Width = 5.7um

Bias Generation transistors (including current mirror transistors):
- Length = 0.5um
- Width = 1.4um

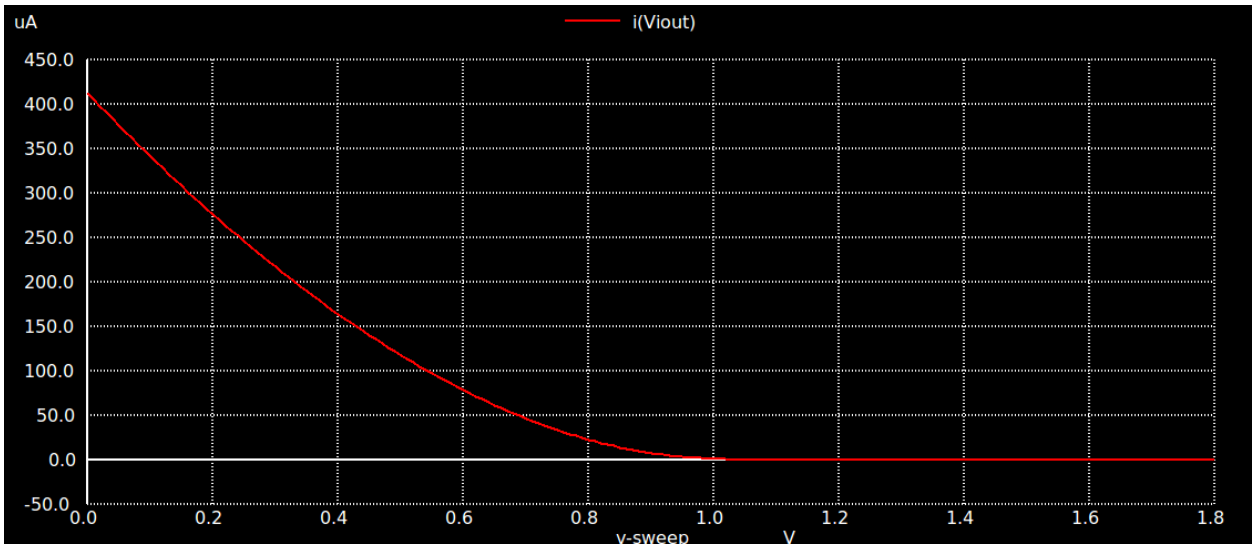
Branch Logic transistors:
- Length = 0.3um
- Width = 3.15um

This set of parameters gave the following plots:

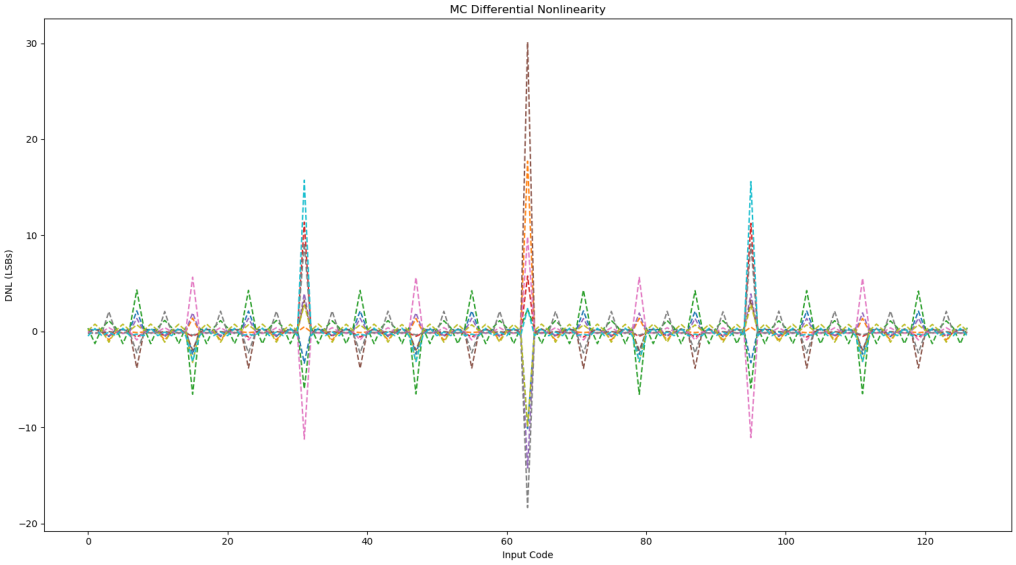


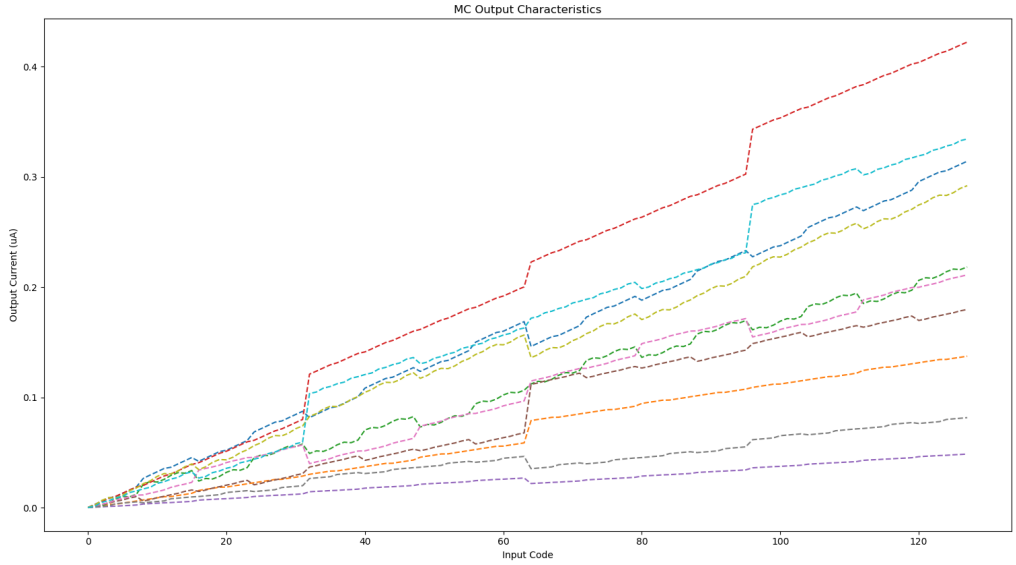


The optimizer was configured to focus on linearity (without Monte Carlo simulations), and so it achieved good results in this space. Here, the maximum DNL is 0.54 LSB, and the INL was also small, at -0.011. Unfortunately, this is the end of this designs list of good traits.



The plot above shows I_{out} as V_{out} is swept from ground to the power supply. The output current gets very large below about a volt, and only stays within 5% of a central value for about 0.7 volts.





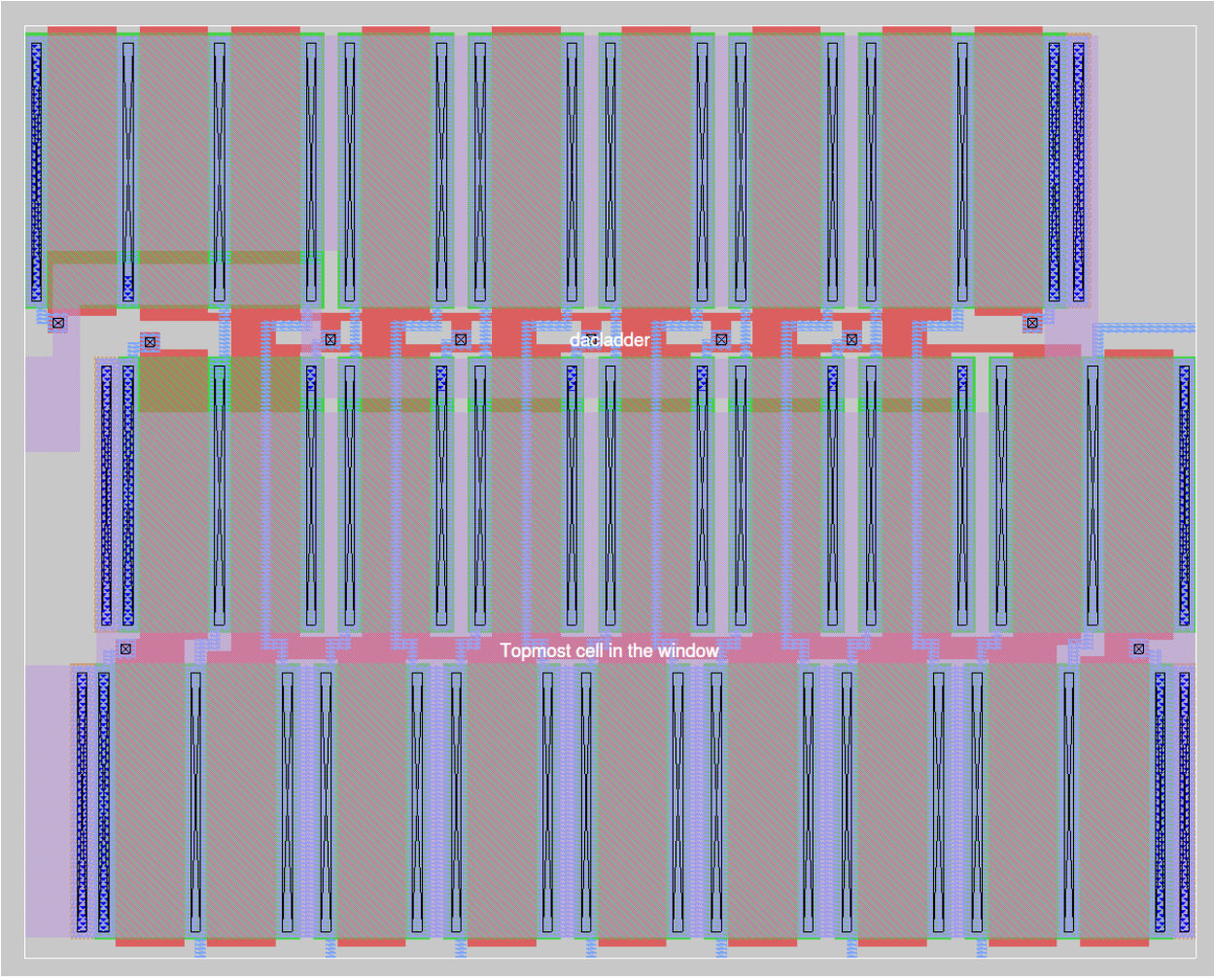
Worse still, I did not set up the optimizer to penalize small transistors, so the variation from Pelgrom's rule is quite extreme. This causes a max DNL of 30 from the ten runs shown here (this is particularly high, compared to many other tests, but isn't as uncommon as I would prefer) and large INLs as well.

Seeing these results, I put a few hours into attempting to improve the design, but I had a hard time meeting all of the constraints with my base design. I modified the optimizer to also consider

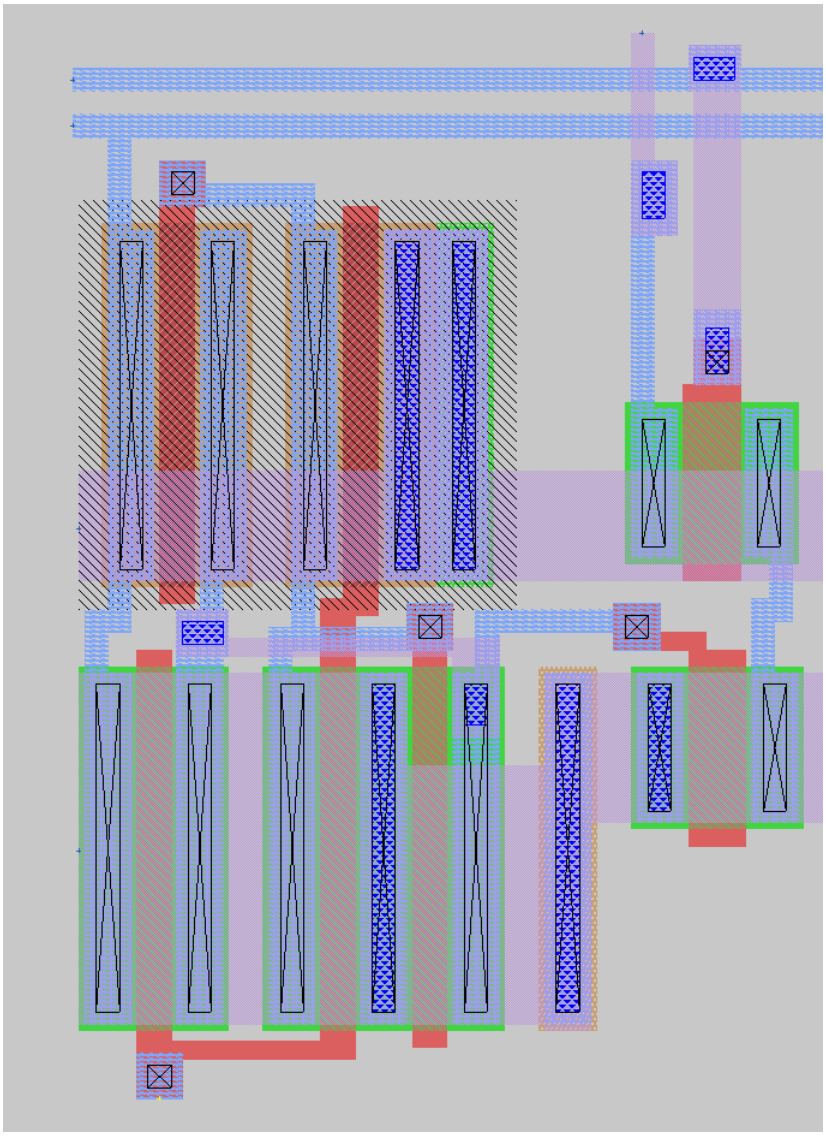
the results of monte carlo simulations and V_{out} sweeping, but I did not have time to thoroughly experiment with this before the final project really kicked in and the first few (very time consuming) results were not promising, so I had to abandon this pursuit.

One final issue worth noting is that I have had trouble getting these files to run on machines other than the ones they were written for. I suspect this is because of the older version of ubuntu running on my laptop. It is very possible that while these files can generate the plots above for me, they will not run in ngspice without error on other machines.

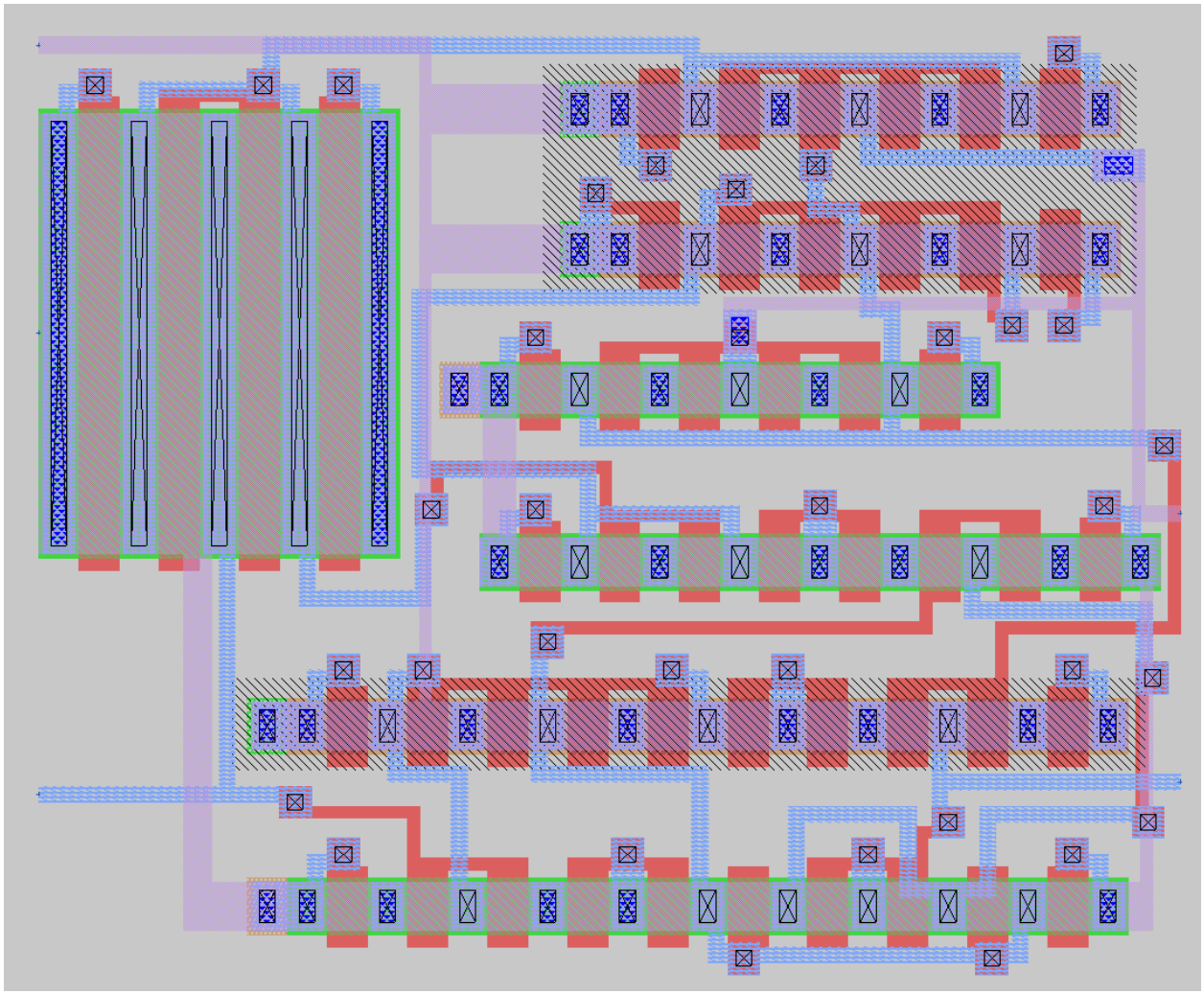
Layout Design



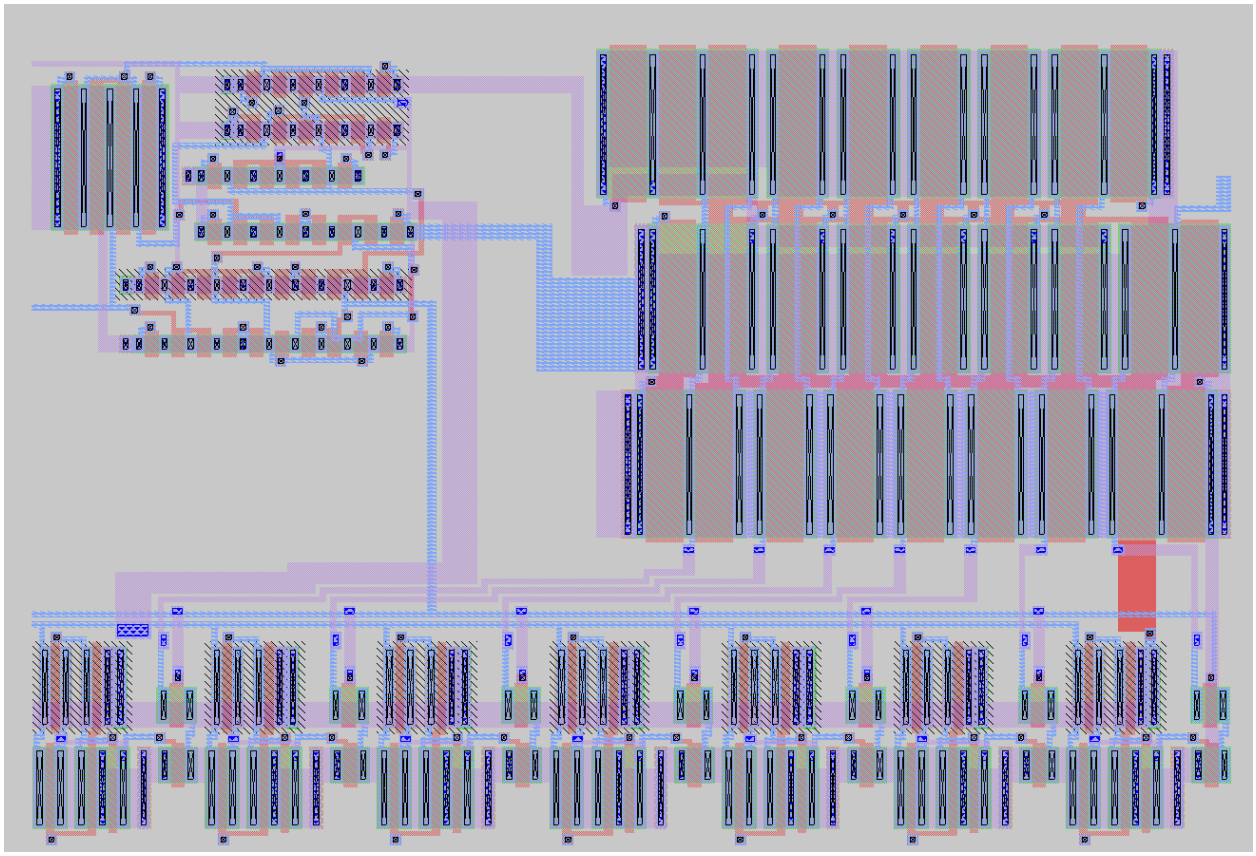
Above is my layout for the ladder portion of this cell. This looks very similar to the schematic shown above, except the transistors have been shifted somewhat to waste less space. The dimensions of this cell are 24.3umx19.3um.



Again, this shows a single cell in the 7 cell branch logic system. There are six identical copies of this to its right, just as in the schematic above. The dimensions of all seven cells together are 45.95umx9.25um.



Finally, this is the bias generation circuit (which includes a cascode generation circuit on the bottom). The transistors do not fit as neatly into a square as I had hoped, but by using the longer cascode strips underneath the large bias generation transistors, I was able to almost fully make this layout a square. Its dimensions are 14.25umx11.7um.



All three cells fit together similarly to how they did in the schematics shown above. The small size of the bais generation circuit means there is a lot of wasted space in the top left quadrant of this cell, unfortunately. The final dimensions for the full DAC are 45.95umx30.65um.

LVS Verification

Possibly due to using an older version of ubuntu on my laptop (which I had to use while travelling), the LVS output contains a lot of warnings and errors. It does report at the end that the netlists match, however. Pasting the text into this document adds roughly 60 pages, so I have chosen to link to the file on github instead, here.