BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

EEE 466 (July 2023)

Analog Integrated Circuits and Design Laboratory

Final Project Report

Section: G1

Group: 08

Design of Instrumentation Amplifier

Course Instructors:

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Signature of Instructor: _____

Academic Honesty Statement:

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"In signing this statement, We hereby certify that the work on this project is our own and that we have not copied the work of any other students (past or present), and cited all relevant sources while completing this project. We understand that if we fail to honor this agreement, We will each receive a score of ZERO for this project and be subject to failure of this course."

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Introduction:

Instrumentation amplifiers are specialized operational amplifiers (op-amps) designed to provide precise amplification of differential input signals while rejecting common-mode noise. Instrumentation amplifiers play a pivotal role in scenarios like offering high precision, gain control and excellent common-mode rejection. This project aims to design and implement an instrumentation amplifier circuit for reliable signal amplification in diverse instrumentation and measurement systems.

An instrumentation amplifier typically consists of three operational amplifiers (op-amps) configured in a specific manner. These op-amps amplify the voltage difference between two input terminals while maintaining high CMRR. A set of resistors allows for adjustable gain.

The key features of an instrumentation amplifier are:

- **Differential Amplification**: In-Amps amplify the voltage difference between two input terminals while rejecting common-mode signals. This makes them particularly useful in applications where the signal of interest is small compared to noise or interference.

- **High Common-Mode Rejection Ratio (CMRR)**: One of the most critical features of an In-Amp is its ability to reject common-mode signals. High CMRR ensures that the amplifier responds primarily to the differential input signal while ignoring any common-mode noise.

- **High Input Impedance**: In-Amps typically have high input impedance, which ensures that they do not load down the source signals, thus preserving signal integrity and accuracy.

- **Low Drift and Offset Voltage**: To maintain accuracy over time and temperature variations, it's important for an instrumentation amplifier to have low drift and offset voltage. This ensures that the amplifier's output accurately represents the input signal.

- **Adjustable Gain**: Many instrumentation amplifier designs feature adjustable gain settings, allowing users to tailor the amplification to the specific requirements of their application.

- **Wide Bandwidth**: In-Amps often operate over a wide frequency range to accommodate various signal types and applications.

- **Low Noise**: In applications where signal fidelity is crucial, low noise performance is essential. In-Amps are designed to minimize noise contributions to the output signal

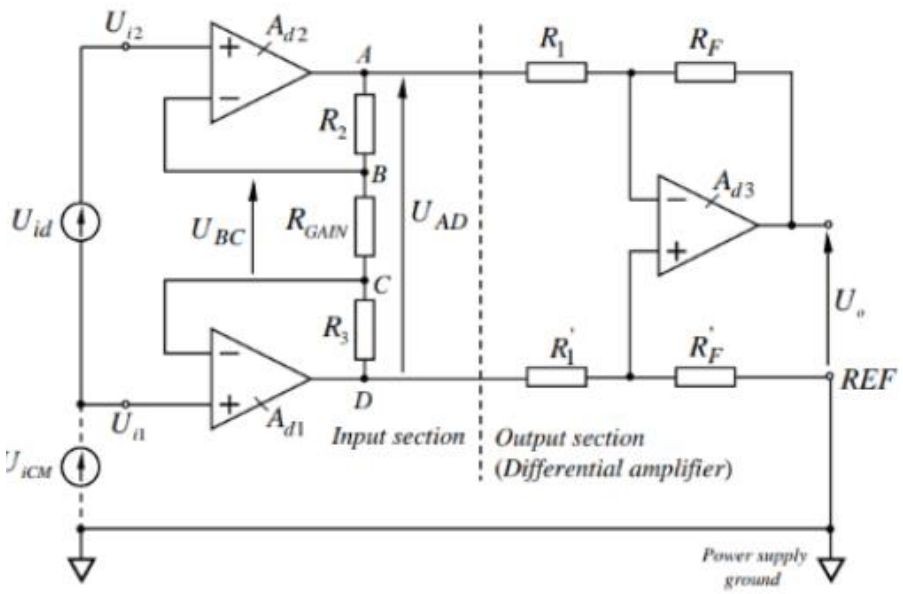


Figure: Schematic of An Instrumentation Amplifier

Theory:

Common-Mode Rejection Ratio (CMRR):

CMRR is a measure of how effectively an electronic circuit, particularly amplifiers, can reject or attenuate unwanted common-mode signals present on both input terminals while amplifying the desired differential signals. It is expressed in decibels (dB) and represents the ratio of the gain for differential signals to the gain for common-mode signals. A higher CMRR value indicates better rejection of common-mode signals and, therefore, improved performance in applications where it's essential to isolate and amplify only the difference between two input signals while rejecting noise or interference that affects both inputs equally.

-3dB Bandwidth:

The -3dB bandwidth is the frequency at which the output voltage or power of a system or component has decreased to half (1/2 or -3dB) of its maximum value compared to its response at lower frequencies. It is a common metric used to characterize the frequency response of amplifiers, filters, and other electronic systems.

Slew Rate:

Slew rate refers to the rate at which an electronic component, such as an operational amplifier (op-amp), can change its output voltage in response to a rapid change in its input signal. It is typically measured in volts per microsecond (V/μs) and indicates the maximum speed at which the device can respond to input voltage changes without distortion.

Voltage Input Offset:

Voltage input offset is the tiny, unintentional voltage difference that appears across the input terminals of electronic components, such as op-amps, when there is no differential input voltage (i.e., when the input terminals are at the same potential or shorted together). This offset voltage can lead to errors in amplification and signal processing, especially in applications where high precision is required.

Current Input Bias:

Current input bias is the small, unintended electrical current that flows into or out of the input terminals of electronic components, like op-amps, even when there is no input voltage. It can affect the biasing of semiconductor devices and introduce offset voltages, potentially impacting the accuracy of amplification and signal processing circuits.

Calculation:

The formulae that need to be used to meet the desired specifications:

1. At condition, that the op amps are ideal active elements and $\frac{R_F}{R_1} = \frac{R'_F}{R'_1}$ for the differential voltage gain is obtained

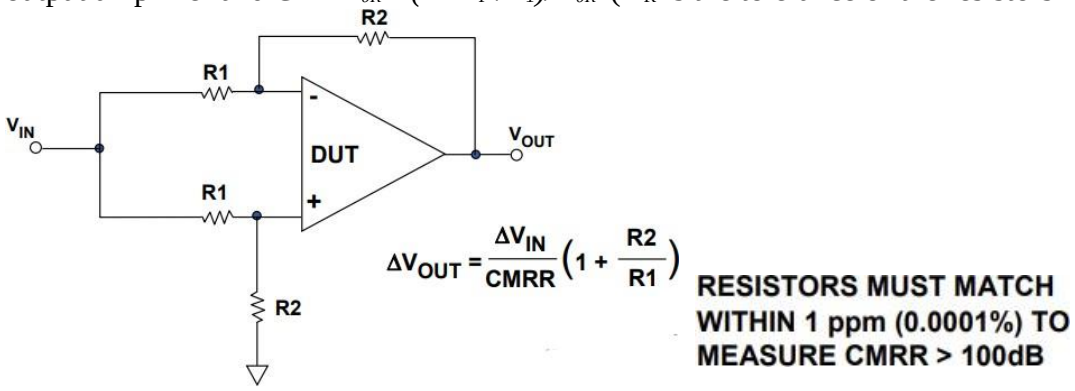
$$A_U = \frac{U_o}{U_{id}} = A_{U1}A_{U2} = \left(1 + \frac{R_2 + R_3}{R_{GAIN}}\right)\frac{R_F}{R_1},$$

where $A_{U1} = \frac{U_{AD}}{U_{id}} = 1 + \frac{R_2 + R_3}{R_{GAIN}}$ is the differential gain of the input section and is the differential gain of the output section.

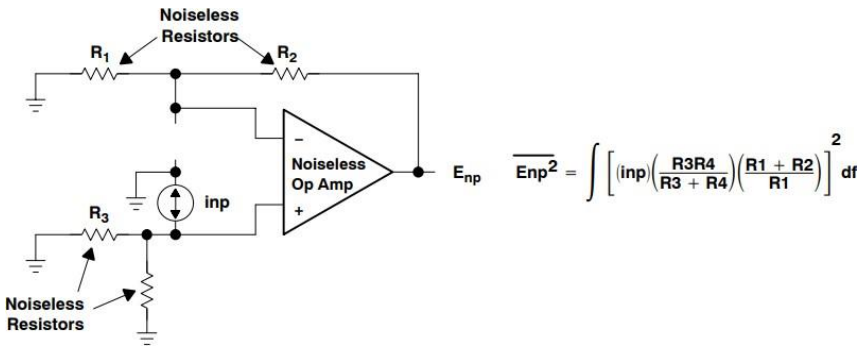
$$A_{U2} = \frac{U_o}{U_{AD}} = \frac{R_F}{R_1}$$

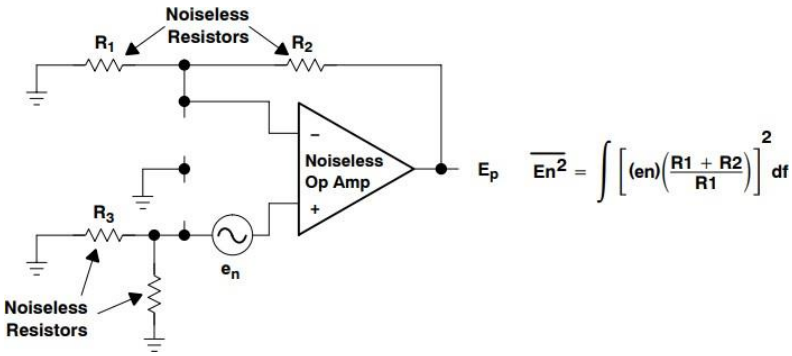
From this equation, it can be seen, that the necessary voltage gain for differential signals can be varied by changing the value of the resistor R_{GAIN} , without affecting the symmetry of the circuit. If $R_{GAIN} = \infty$ the input section operates as a voltage follower and the differential voltage gain of the circuit is determined only by the gain of the output section.

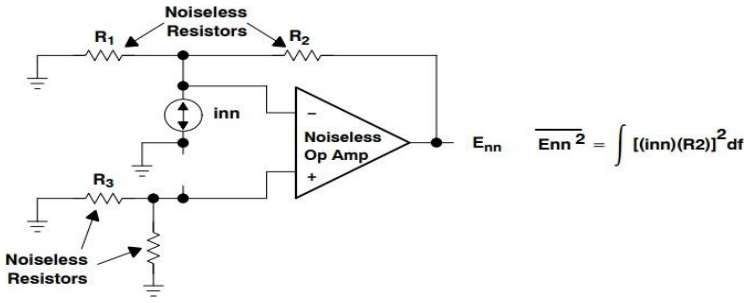
2. Mathematically, the total common-mode rejection of the in-amp is $CMRR = AU\ CMRR_3$ Where, $CMRR3 = CMRR_{\delta R} || CMRR_{A,\ A3}$, $CMRR_{A3}$ is the common-mode rejection of the output amplifier and $CMRR_{\delta R} = (1+R_F/R_1)/4_{\delta R}$ (δ_R is the tolerance of the resistors R1 , RF , R1' and RF').



3. For calculating noise in differential op-amp circuits,







Combining to arrive at the solution for the circuit's output rms noise voltage, E_{oarms}, due to the input referred op amp noise in the circuit:

$$E_{oarms} = \sqrt{\overline{En}^2 + \overline{Enp}^2 + \overline{Enn}^2}$$

$$E_{oarms} = \sqrt{\int\left[((inn)\,R2)^2 + \left((inp)\left(\frac{R3R4}{R3 + R4}\right)\left(\frac{R1 + R2}{R1}\right)\right)^2 + \left(en\left(\frac{R1 + R2}{R1}\right)\right)^2\right]df}$$

Normally $R_1 = R_3$, $R_2 = R_4$, and $inn = inp = in$. Making this substitution reduces the above equation to:

$$E_{oarms} = \sqrt{\int\left[(2inR2)^2 + \left(en\left(\frac{R1 + R2}{R1}\right)\right)^2\right]df}$$

$$R1 = R3,\ R2 = R4 \text{ and } inn = inp = in$$

For a MOS device, noise can be calculated with following formula

$$\frac{\overline{i_{nd}^2}}{\Delta f} = 4kT\gamma g_{do}$$

For Flicker Noise,

$$\frac{\overline{i_{nf}^2}}{\Delta f} = \frac{K_f}{f}\frac{g_m^2}{C_{ox}WL} \qquad \frac{\overline{v_{nf}^2}}{\Delta f} = \frac{K_f}{f}\frac{1}{C_{ox}WL}$$

4. For calculating offset voltage of the differential op-amp

$Vout = A_{OL}\,Vos$ Here, A_{OL} is the open loop gain

5. For calculating input bias current,

$$V_O = \left[1 + \frac{R2}{100}\right] V_{OS} + \left[1 + \frac{R2}{100}\right] I_{B+} R_S - \left[1 + \frac{R2}{100}\right] I_{B-} R_S$$

6. For calculating offset error and CMRR,

$$\text{ERROR (RTI)} = \frac{V_{CM}}{CMRR} = \frac{V_{IN}}{CMRR}$$

$$V_{OUT} = \left[1 + \frac{R2}{R1}\right]\left[V_{IN} + \frac{V_{IN}}{CMRR}\right]$$

$$\text{ERROR (RTO)} = \left[1 + \frac{R2}{R1}\right]\left[\frac{V_{IN}}{CMRR}\right]$$

7. For calculating slew rate,

$$\text{Slew rate } SR = \frac{I_5}{C_c}$$

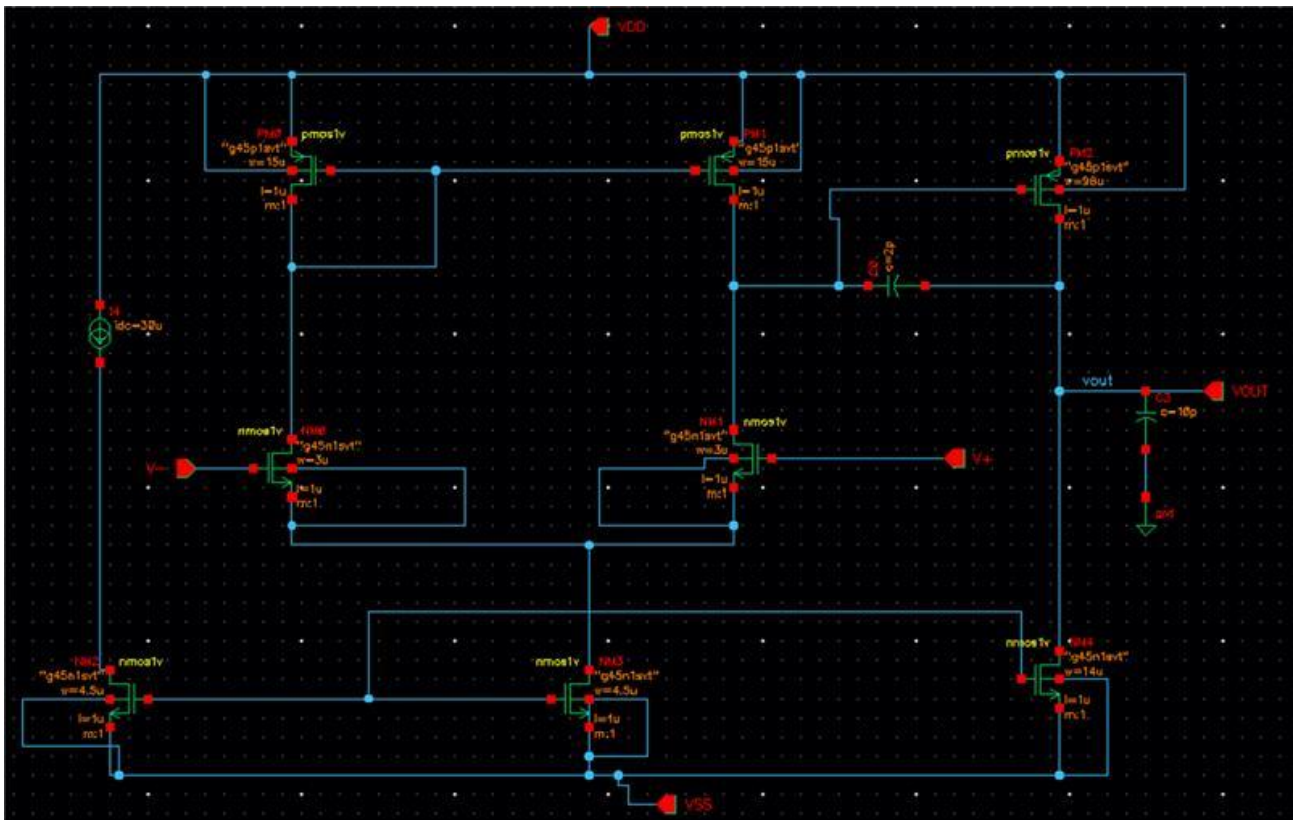
8. For calculating gain-bandwidth,

$$\text{Gain-bandwidth } GB = \frac{g_{m1}}{C_c}$$

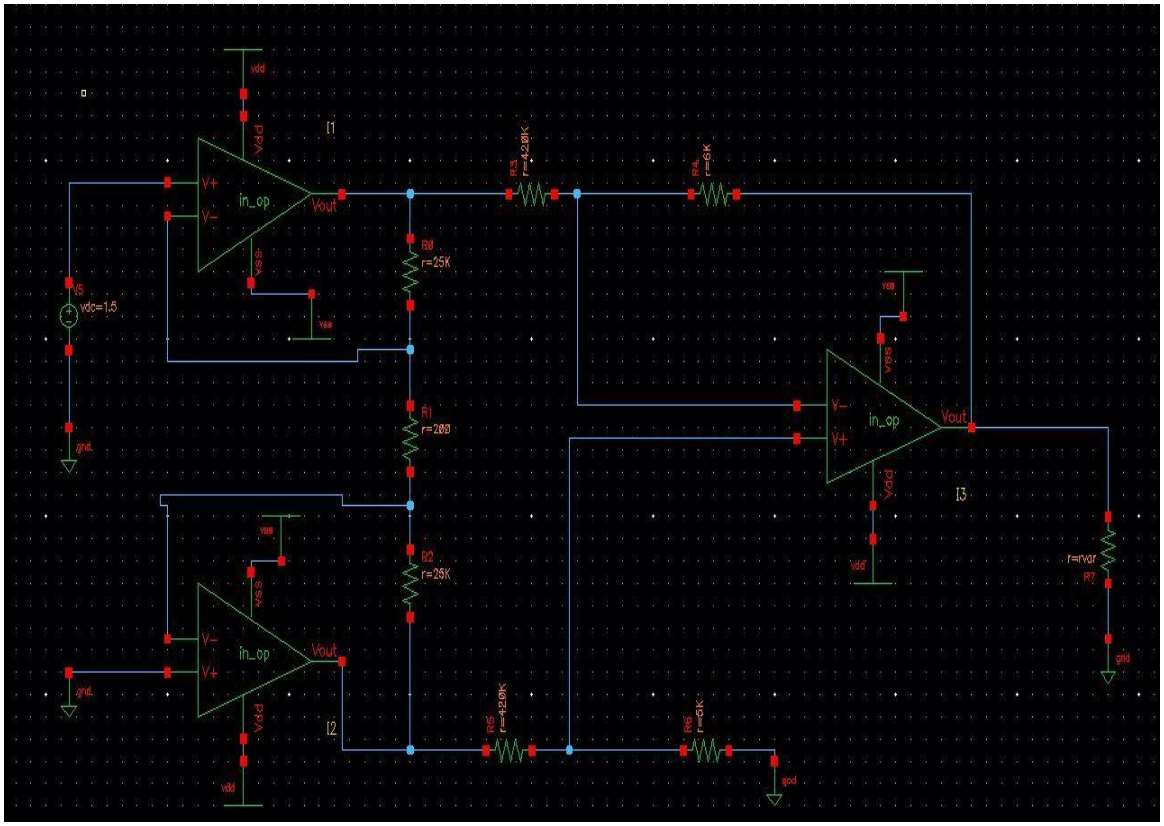
9. For calculating offset voltage,

$$Vo = Vio + R_f I_{\bar{B}}$$
$$Vo = Vio - R_i I_{\bar{B}}$$

Op-amp circuitry:



Instrumentation amplifier circuitry:



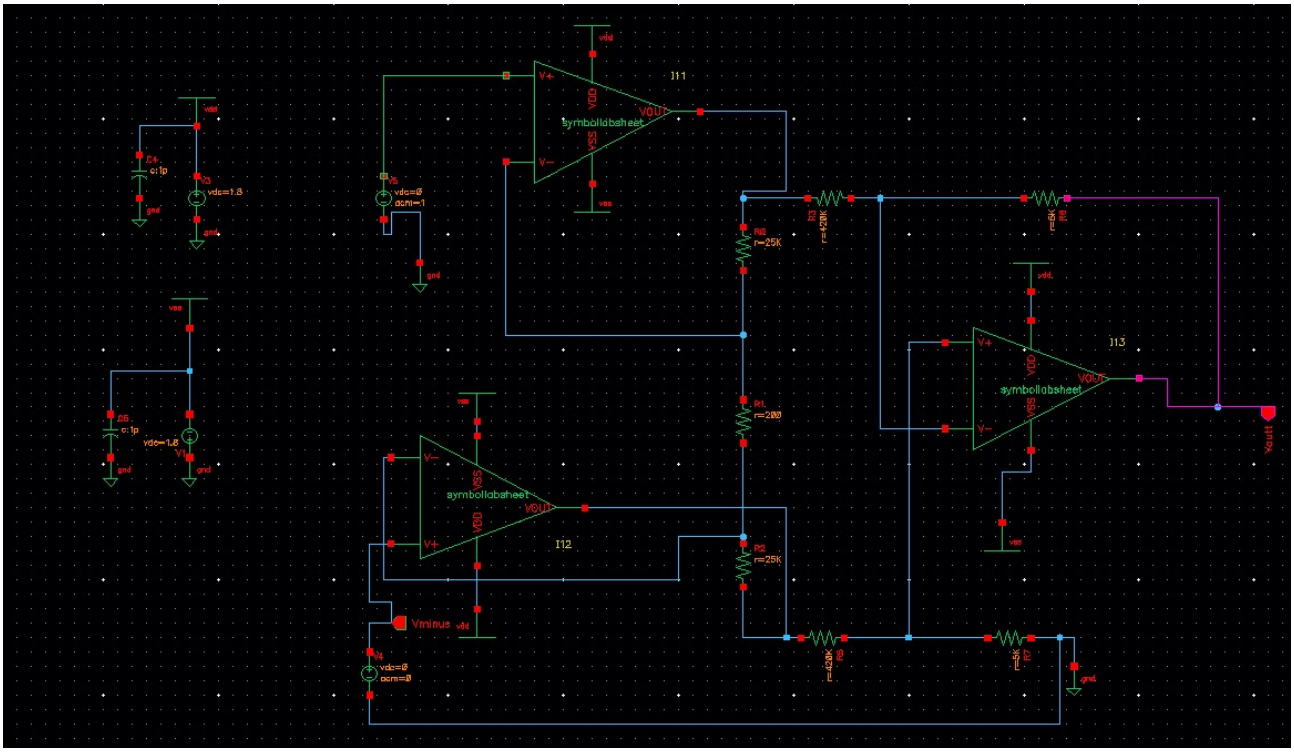
Gain and -3db Bandwidth design:

$$A_U = \frac{U_o}{U_{id}} = A_{U1}A_{U2} = \left(1 + \frac{R_2 + R_3}{R_{GAIN}}\right)\frac{R_F}{R_1},$$

$$\text{Gain-bandwidth } GB = \frac{g_{m1}}{C_c}$$

We adjusted capacitance value to achieve 100kHz bandwidth.

Schematics:



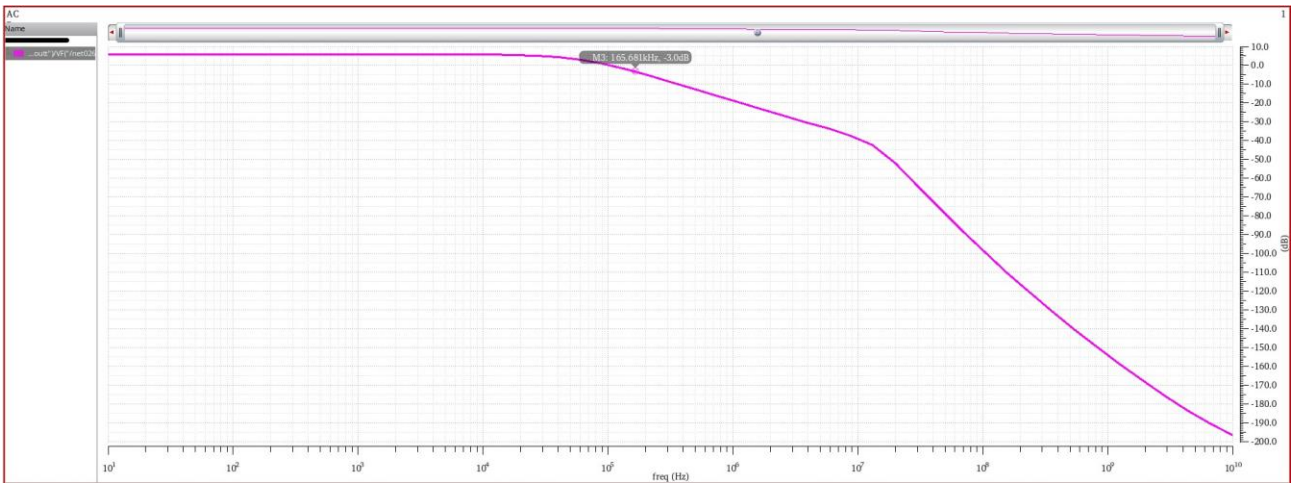


Figure: Vout vs Frequency

The peak voltage level is 100V. So the voltage level for cutoff $\frac{100}{\sqrt{2}} = 70.7V$. From the plot it is will be
evident that 70.7V occurs at 165.68kHz. So, the required -3dB bandwidth is achieved.

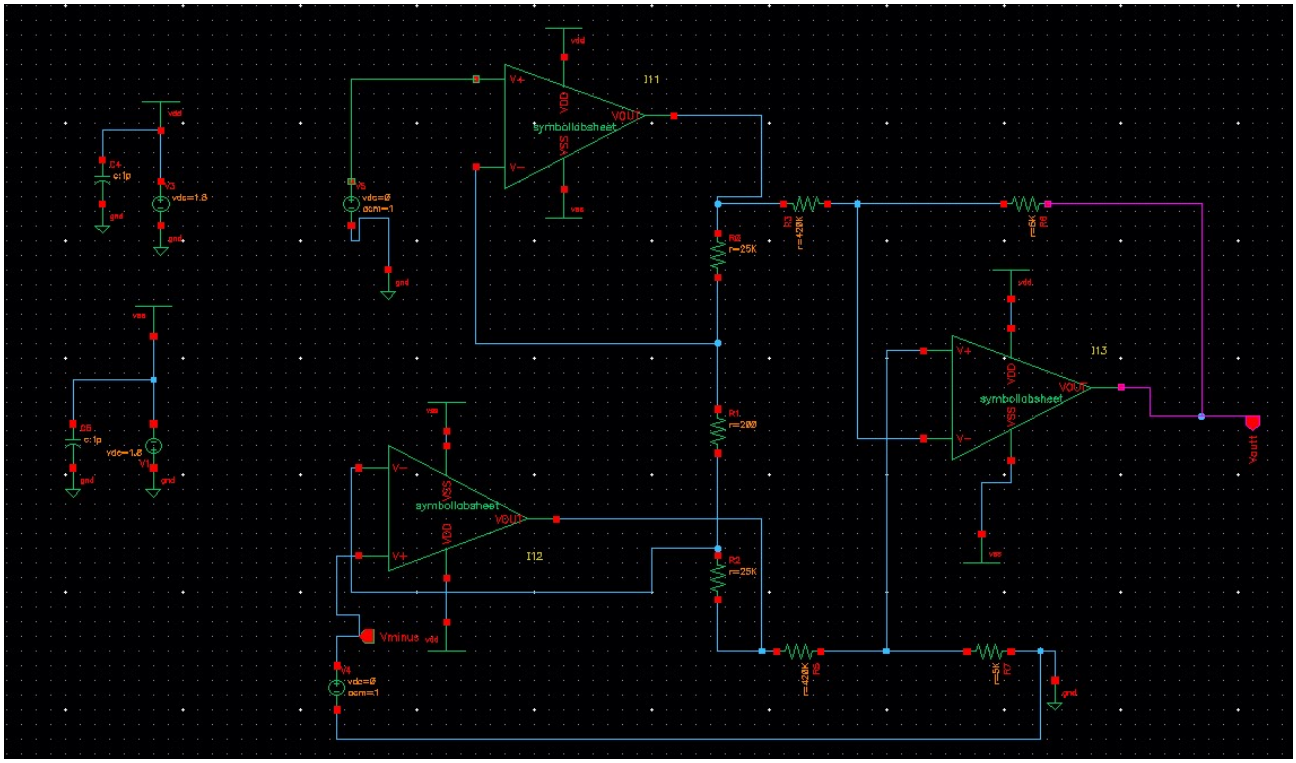
CMRR analysis:

$$\Delta V_{OUT} = \frac{\Delta V_{IN}}{CMRR}\left(1 + \frac{R2}{R1}\right)$$

RESISTORS MUST MATCH WITHIN 1 ppm (0.0001%) TO MEASURE CMRR > 100dB

As CMRR of instrumentation amplifier is dependent on the CMRR of the last op-amp and the mismatch between resistors, R_f and R_1 connected with this op-amp.

Circuit for determining CMRR:



CMRR response:

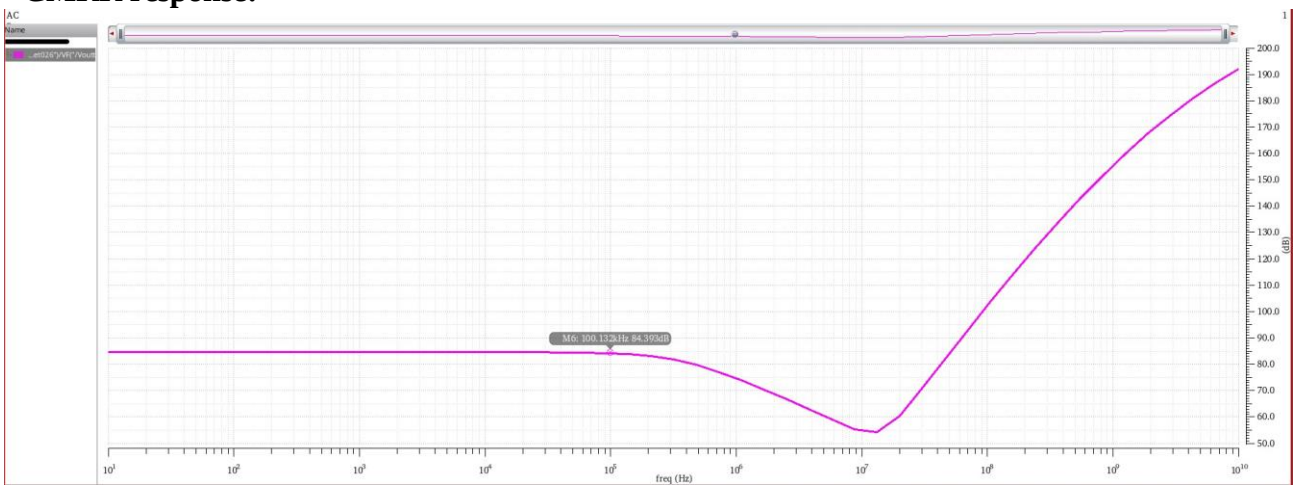
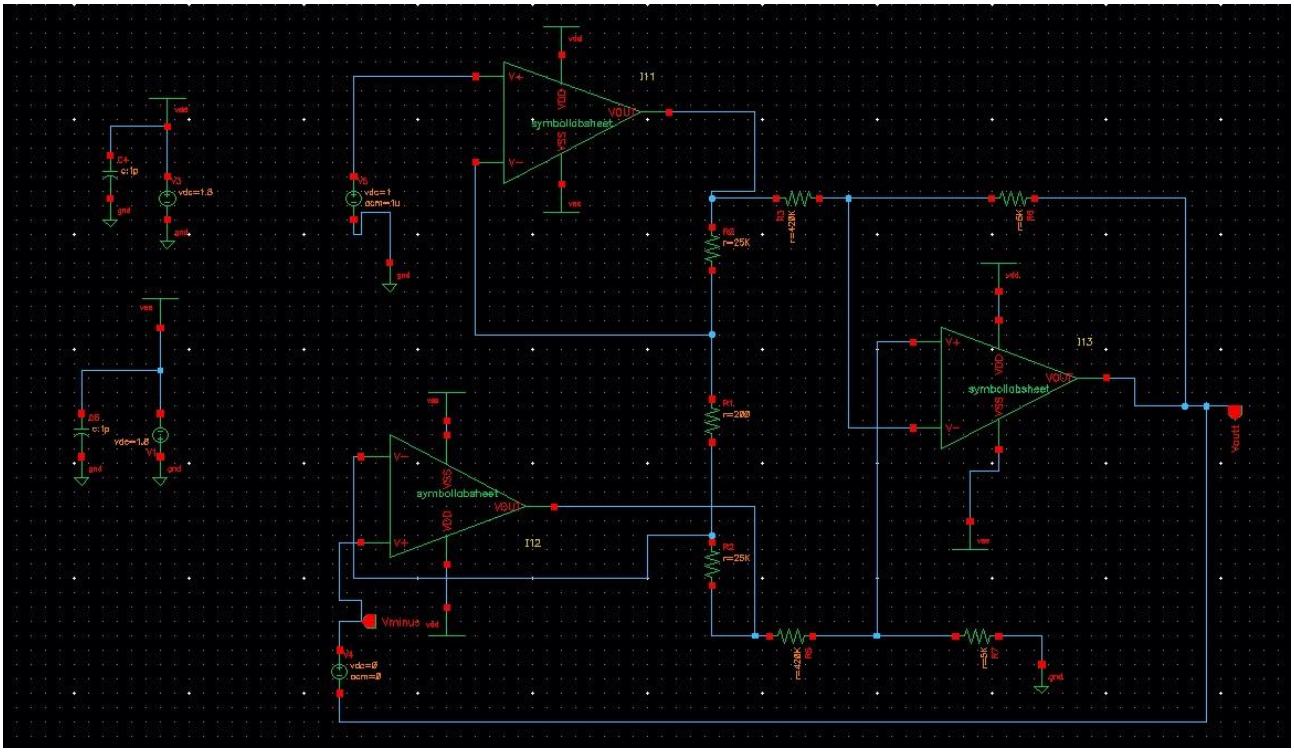


Figure: CMRR vs Frequency

The design requirement for CMRR was 80dB (at G=100). For the operating region up to 100kHz, 80dB or more than 80dB CMRR is maintained which is 84dB. So design requirement is satisfied.

Noise analysis:

Schematics



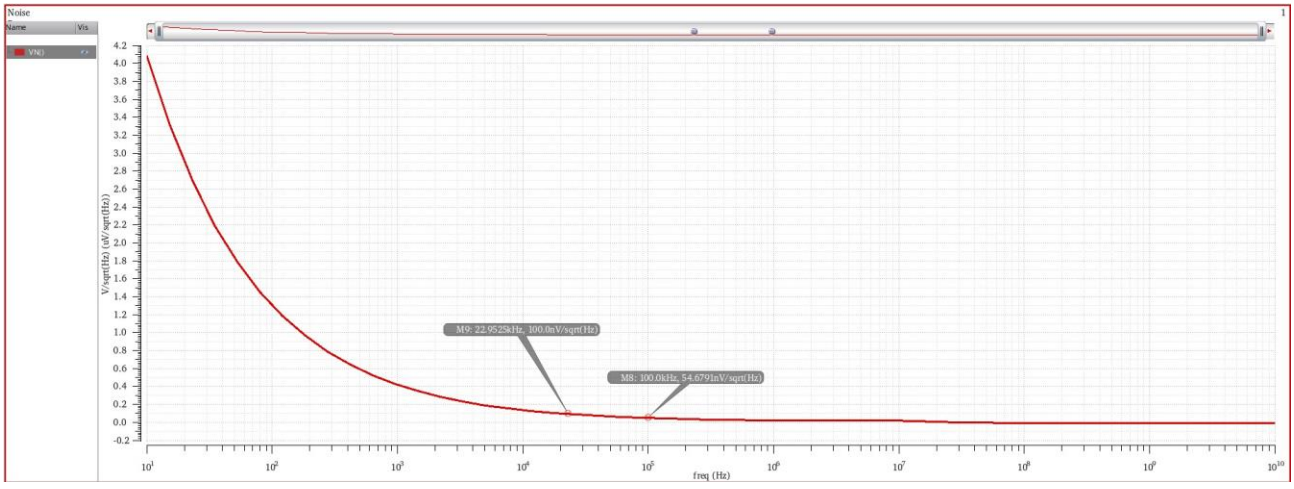
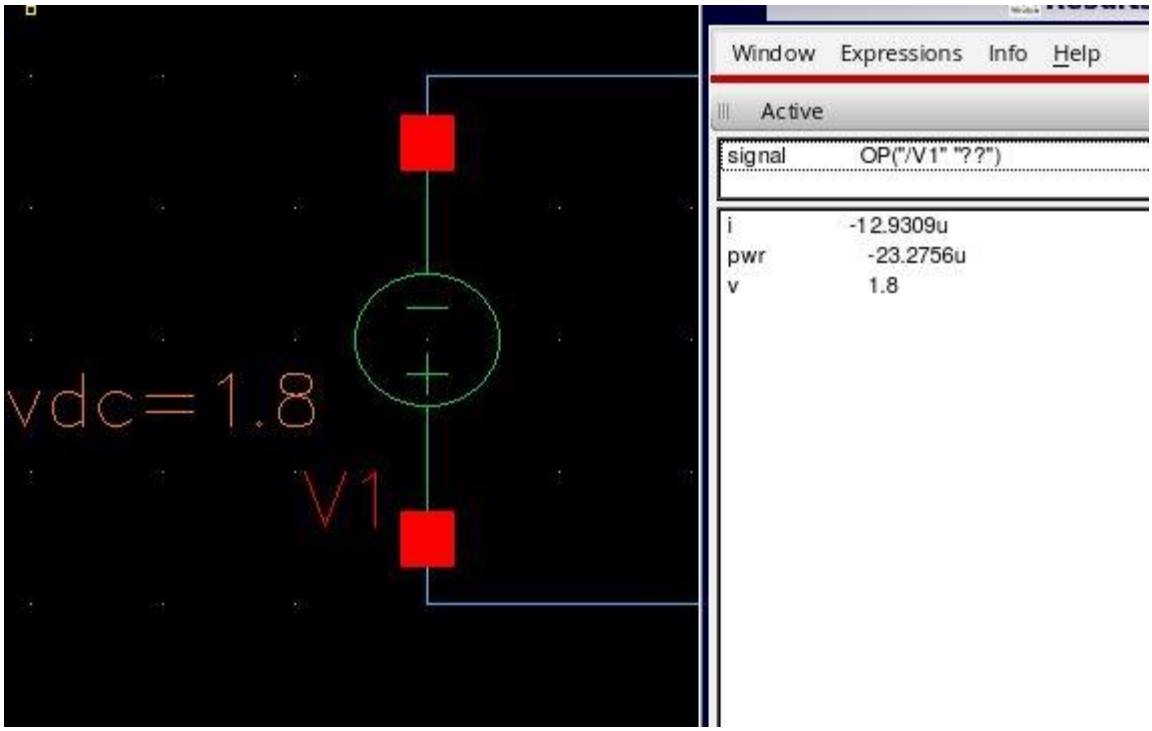


Figure: Noise vs Frequency

The design requirement for noise was 100 nV/√Hz or less. From the noise analysis of the circuit it is evident that 54.76 nV/√Hz noise level is achieved at 1kHz. The circuit has better noise coefficient at larger frequencies. However, at low frequencies noise level is high.

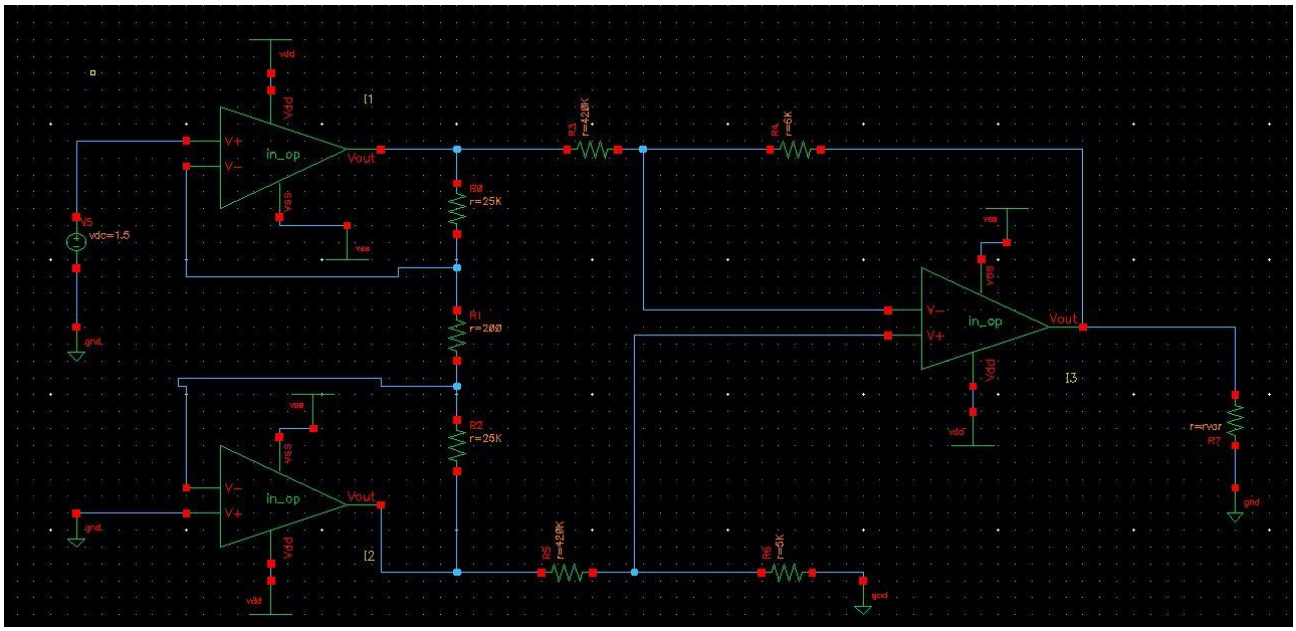
Current – Supply analysis:



The current drawn at VSS and VDD are around 12.9309uA. The design requirement was 1mA. So, the design prerequisite has been attained.

Output voltage and current analysis:

Schematics:



Considering the loading effect, the output voltage-current for different load is plotted using resistance sweep:

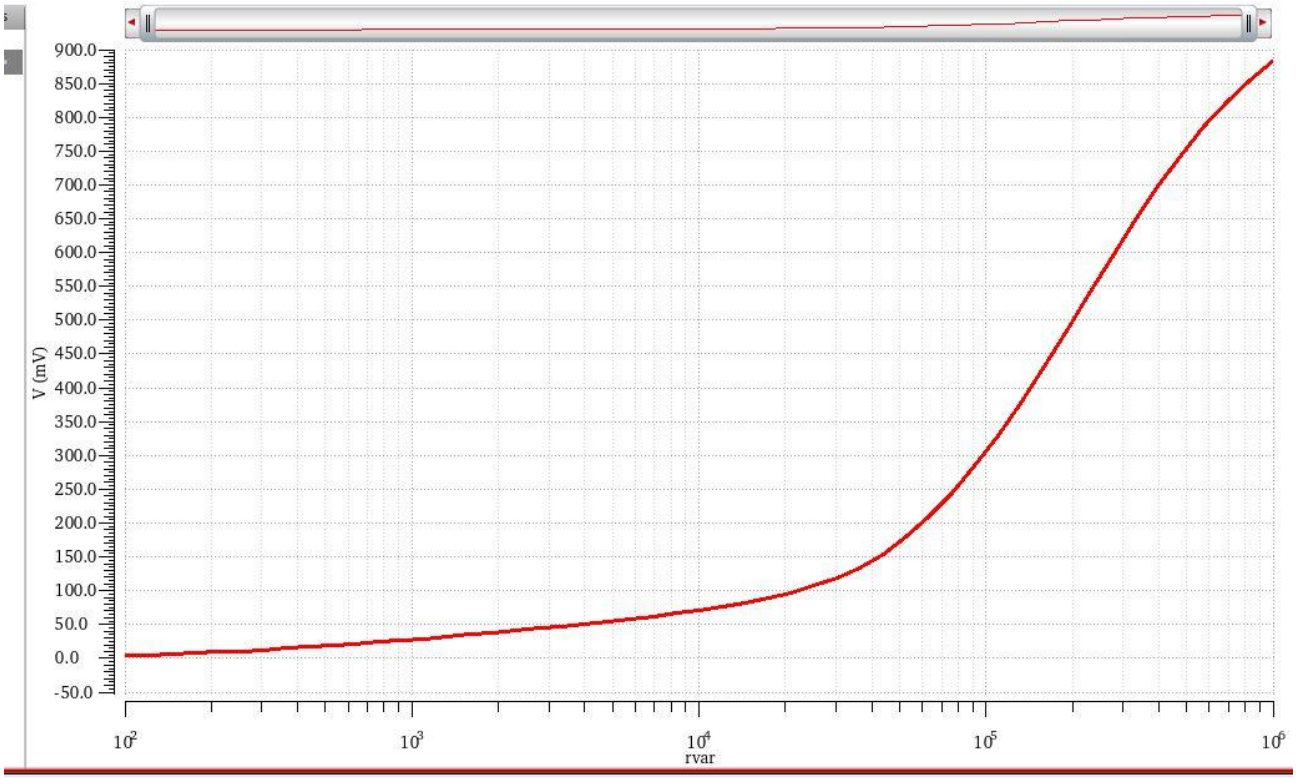


Figure: Vout and Current vs Frequency

We performed resistance sweep to observe output voltage and output current range.The design requirement for output range was 0 to Vs-0.3. As Vs=1.8 was used, the required range is 0 to 1.5V. From the graph it is seen that for our circuit, output voltage varies from 0 to 1V. So, the design is nearly in compliance with the requirement, with slight error. The design requirement for output range was 50 uA whereas we got 5-25 uA.

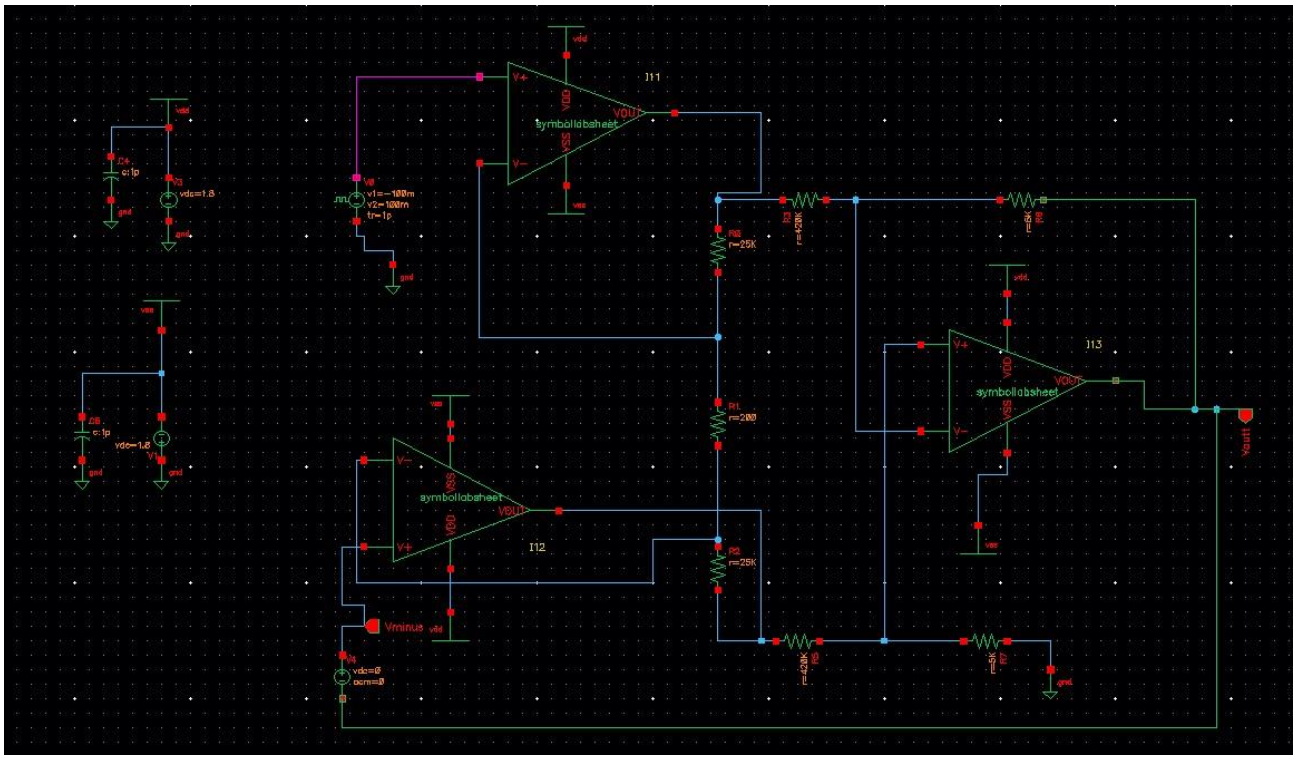
Slew rate analysis:

For increasing slew rate, we increased the width of mosfet below the current source, so that from the

$$\text{Slew rate } SR = \frac{I_5}{C_c}$$

We could decrease the slew rate by decreasing the tail current. In this case, we had to adjust the bandwidth again.

Circuit used for calculating slew rate:



Output voltage for square pulse input:

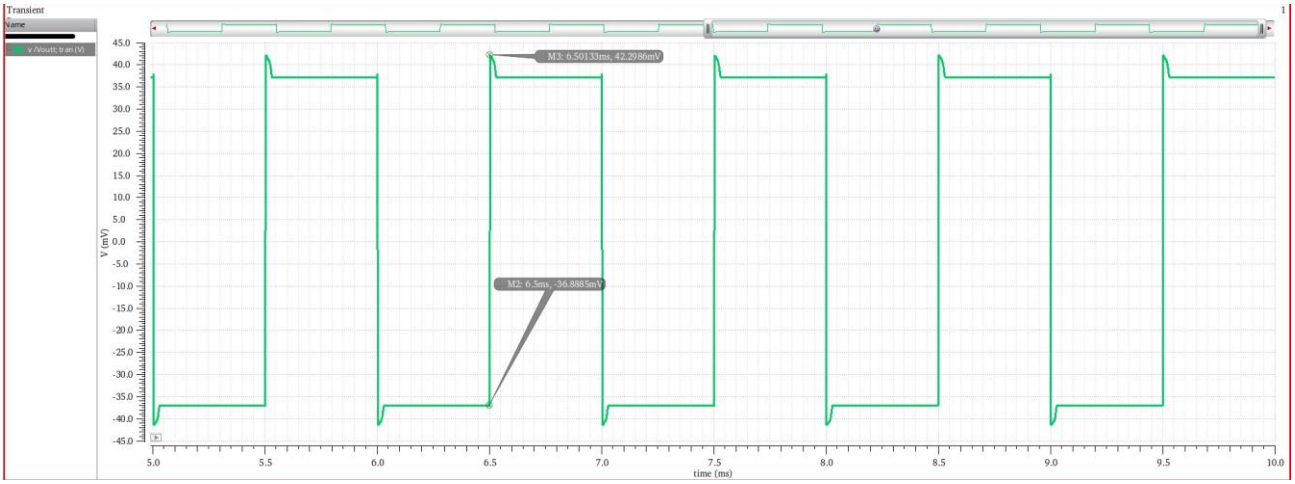


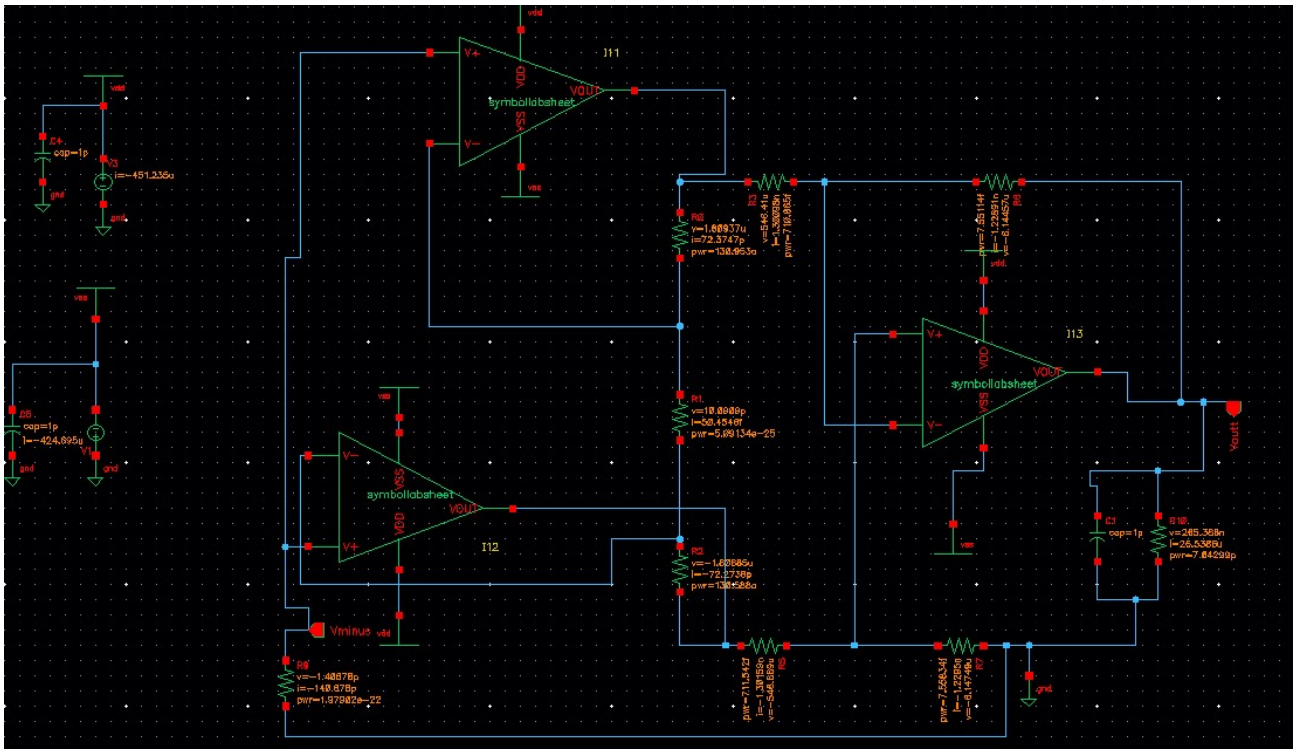
Figure: Vout vs time

Using slew-rate-calculator the slew rate was calculated as:

Which is 0.06V/us. The design requirement was 0.1V/us or higher. So we've met the necessary design benchmarks.

Input Offset Voltage analysis:

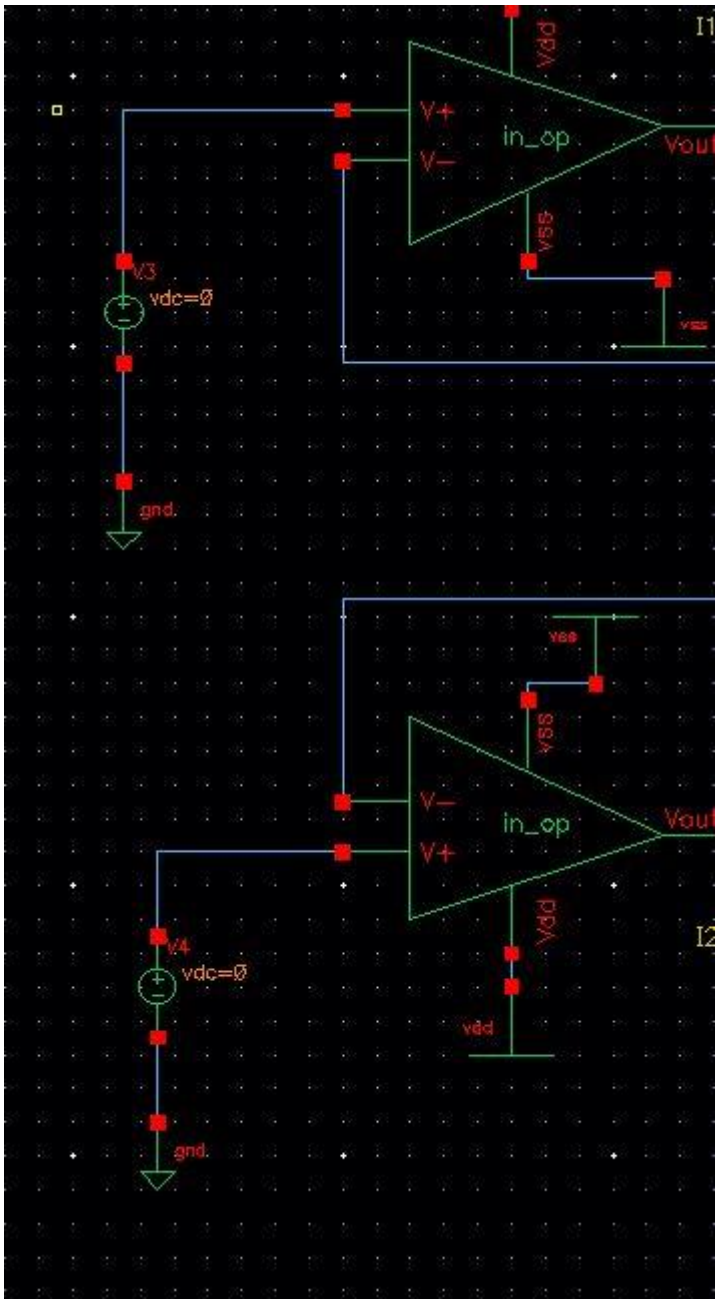
The circuit used for calculating off-set voltage is given by:



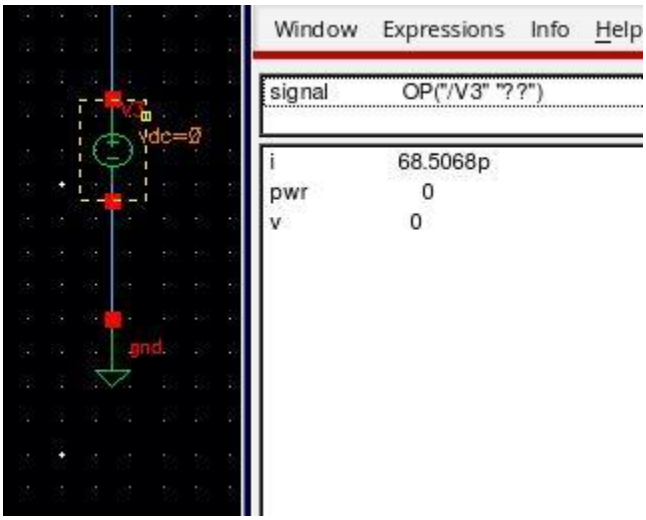
As we can see from the circuit analysis the input offset voltage is 265.35 nV. The design requirement was 20uV or lower. So the design adheres to the mandated conditions.

Bias current analysis:

Circuits:



Input bias current:



Using theoretical calculation, the positive bias current was calculated as 68.5068 pA. The design requirement was 100pA or lower. So the design requirement was met.

Analysis:

Slew Rate vs. Stability: For effective signal processing, a high slew rate is must but it can also introduce stability issues, especially in complex amplifier configurations. Engineers must carefully analyze the amplifier's transient response and ensure it remains stable under various conditions.
In our project, addressing these trade-offs involved a combination of simulation, component selection, circuit optimization, and iterative testing. Ultimately, the design team made informed decisions based on the specific application requirements and the project's objectives, striving to create an instrumentation amplifier that optimally balanced these design trade-offs to meet the overall performance criteria effectively and efficiently.

Low Noise vs. Bandwidth: Reducing noise typically involves selecting low-noise components and minimizing amplification stages. However, these measures may compromise the amplifier's bandwidth.Striking a balance between noise and bandwidth is essential, particularly in applications where wide frequency coverage is crucial.

CMRR vs. Bandwidth: Achieving a high CMRR often requires careful component matching and balanced circuitry, which can limit the amplifier's bandwidth. Balancing CMRR and bandwidth demands meticulous design to ensure that the amplifier retains its accuracy across the required frequency range.

Input Offset Voltage vs. Input Bias Current: Minimizing input offset voltage usually necessitates the use of precision components, which can be more susceptible to input bias current. Designers must consider how to manage these two parameters simultaneously to maintain signal accuracy.

Supply Current vs. Low Power: In applications where power efficiency is paramount, minimizing supply current is essential. However, achieving this may lead to trade-offs in other aspects, such as bandwidth or slew rate. Optimizing the trade-off between low supply current and other performance criteria is often a critical design decision.

Result analysis:

The design requirement and the achieved parameters are as follows

Parameters	Required	Achieved
Supply Voltage	3-5V	3.6 (+1.8/-1.8)
Output Range	0 to Vs-0.3(1.5)	0 to 1
Slew Rate	0.1 V/us	0.06V/us
Current - Input Bias	100 pA	68.0568 pA
Voltage - Input Offset	20 uV	265.35nV
-3db Bandwidth	100 kHz	165.68 kHz
Current - Supply	1 mA	5-25 uA
Current - Output	50	5-25 uA
CMRR (at G = 100)	80	84 dB
Noise (at G = 100)	100 nV/√Hz	54.76nV/√Hz

Conclusion:

In conclusion, this instrumentation amplifier project has demonstrated the successful design, implementation, and evaluation of a high-performance amplifier circuit capable of accurately amplifying small differential signals in noisy environments. Through meticulous circuit design, component selection, and rigorous testing, we have achieved our objectives of creating a robust amplifier with improved common-mode rejection ratio and reduced noise. The performance evaluation has shown that the amplifier meets or exceeds the specified requirements, providing reliable signal amplification for various measurement and instrumentation applications. While challenges were encountered during the design and testing phases, innovative solutions were devised to overcome them, resulting in a functional and efficient amplifier design. Moving forward, potential enhancements could include further optimization of the circuit layout, integration of additional filtering techniques for noise reduction, and exploration of alternative component configurations to expand the amplifier's versatility and applicability in diverse settings. Overall, this project contributes valuable insights to the field of instrumentation and measurement, offering a solid foundation for future research and development endeavors in this domain.