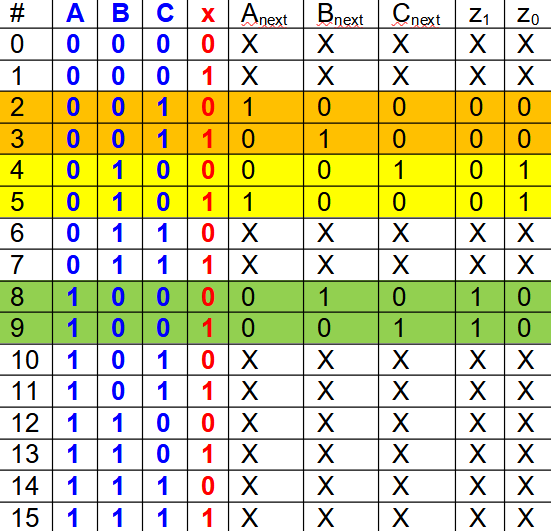
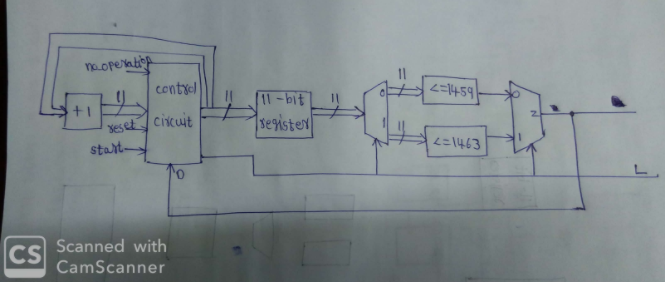
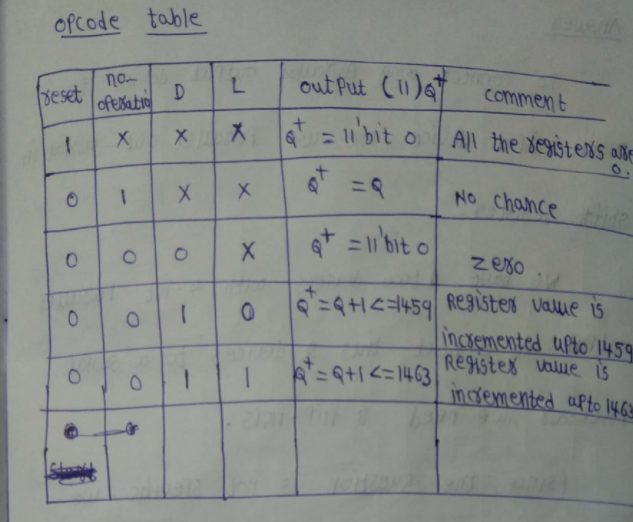
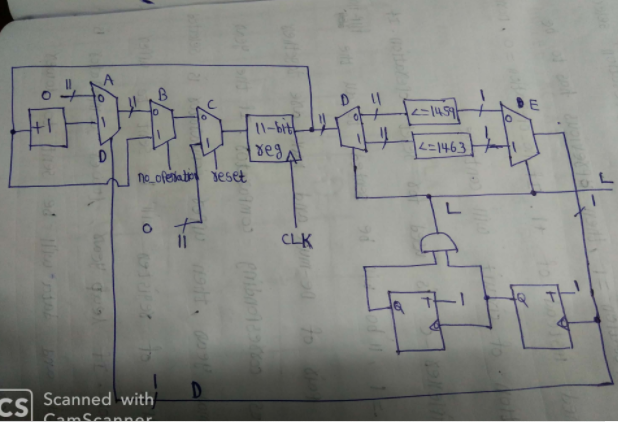
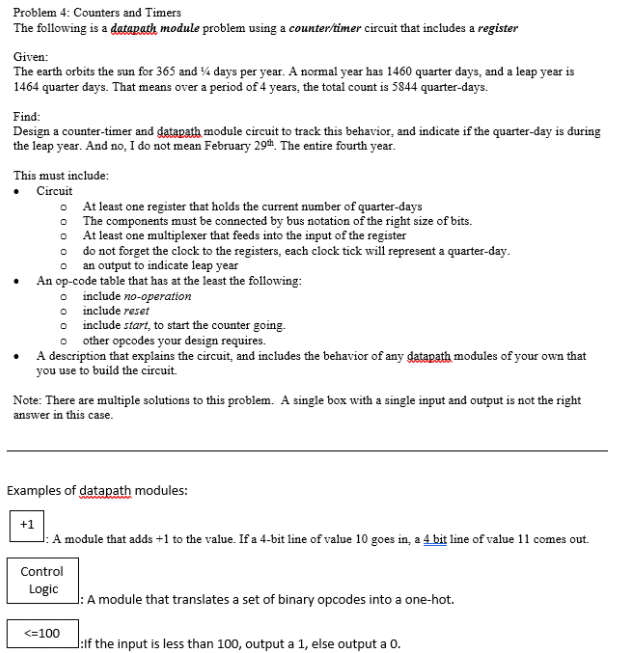
Sequential Logic

Registers, Counters, and Timers





A picture containing text, furniture, cabinet

Description automatically generatedMemory

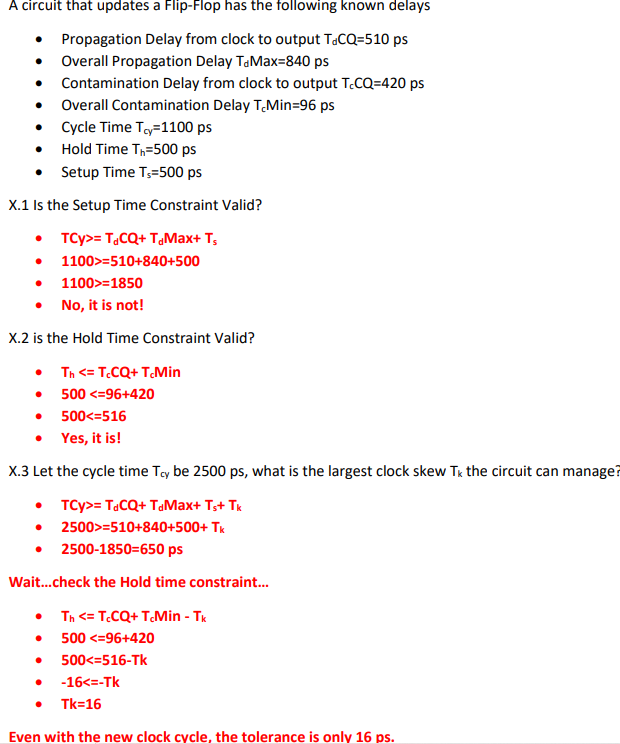


RTL and ASM

A picture containing chart

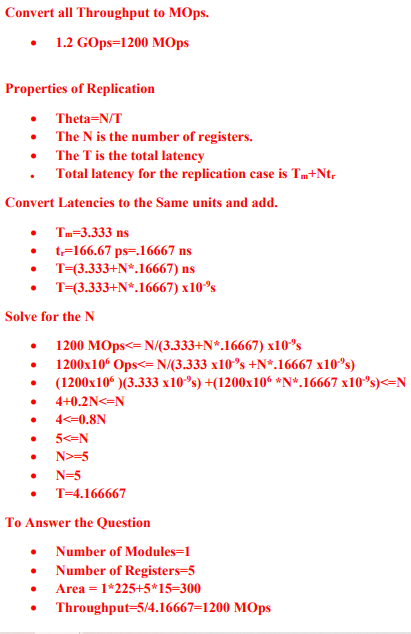
Description automatically generatedDiagram, schematic

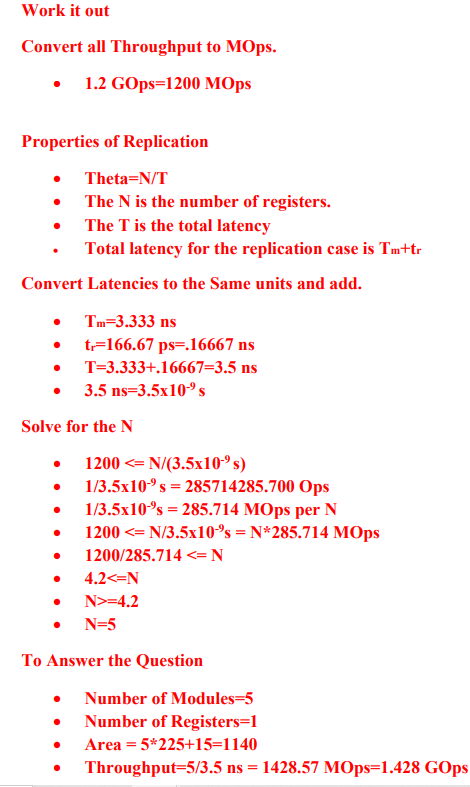
Description automatically generated

Timing Constraints

Diagram

Description automatically generated





Pipelining

Chart

Description automatically generatedText

Description automatically generated