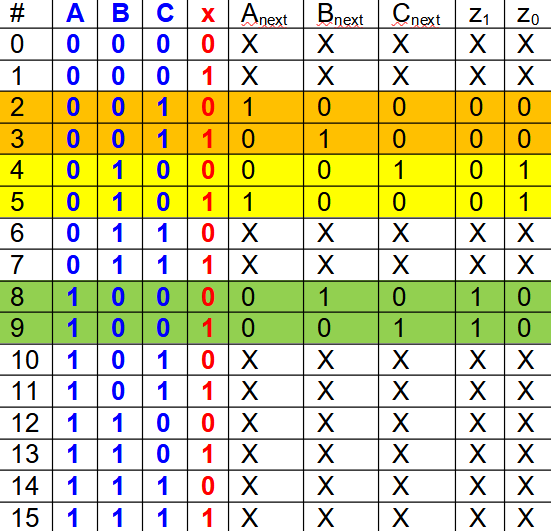
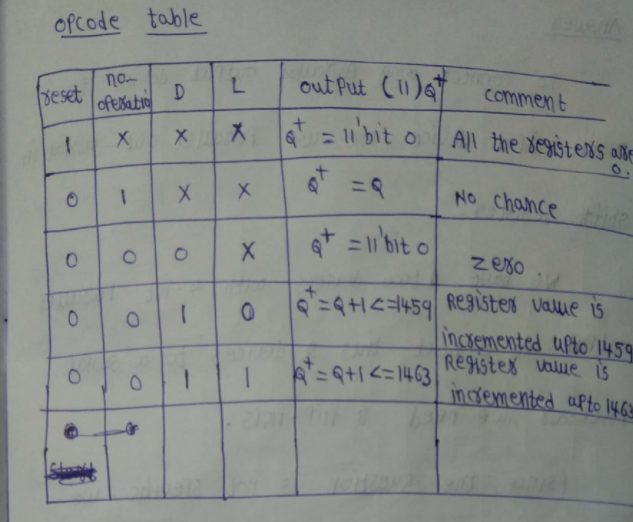
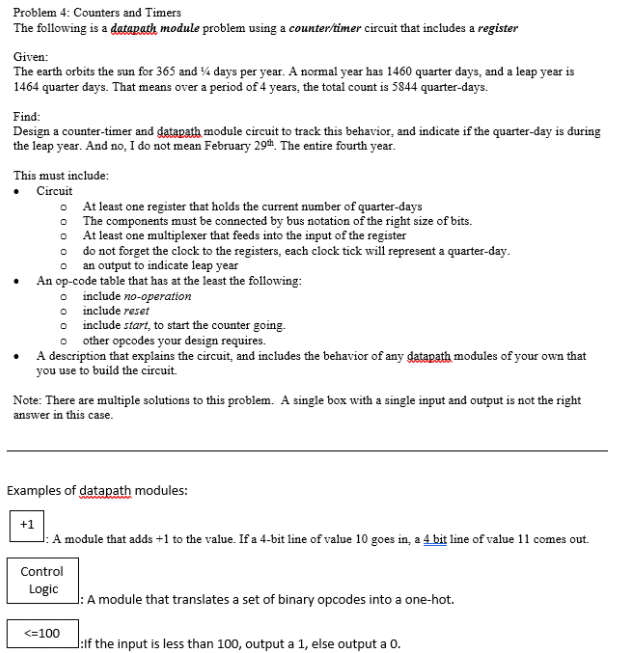
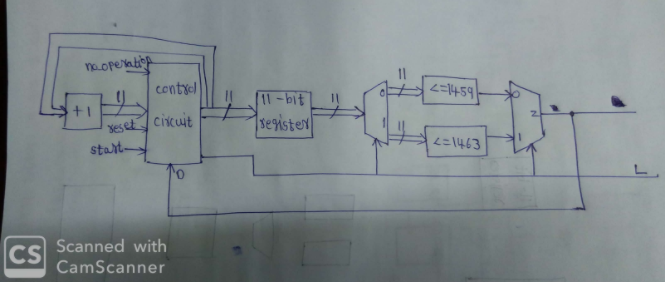
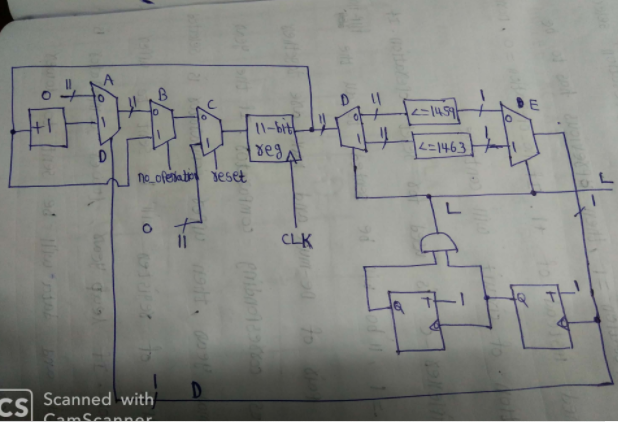
Sequential Logic



Registers, Counters, and Timers



Memory

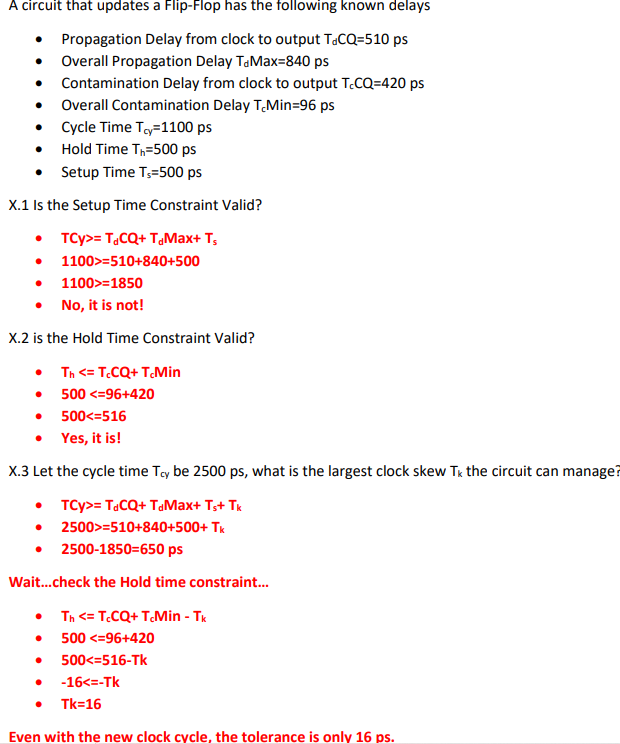
RTL and ASM

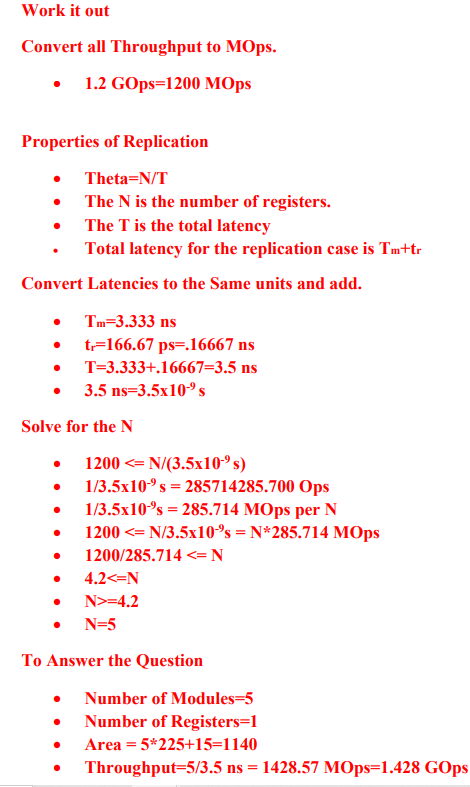
Table

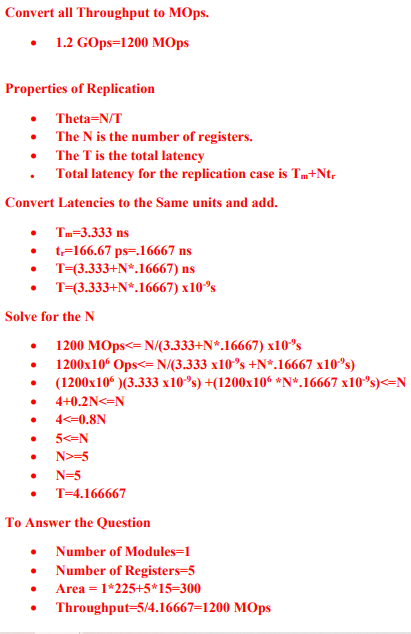
Description automatically generatedDiagram, schematic

Description automatically generated

Timing Constraints







Pipelining