CAPITOL
Technology University

CACTUS-1

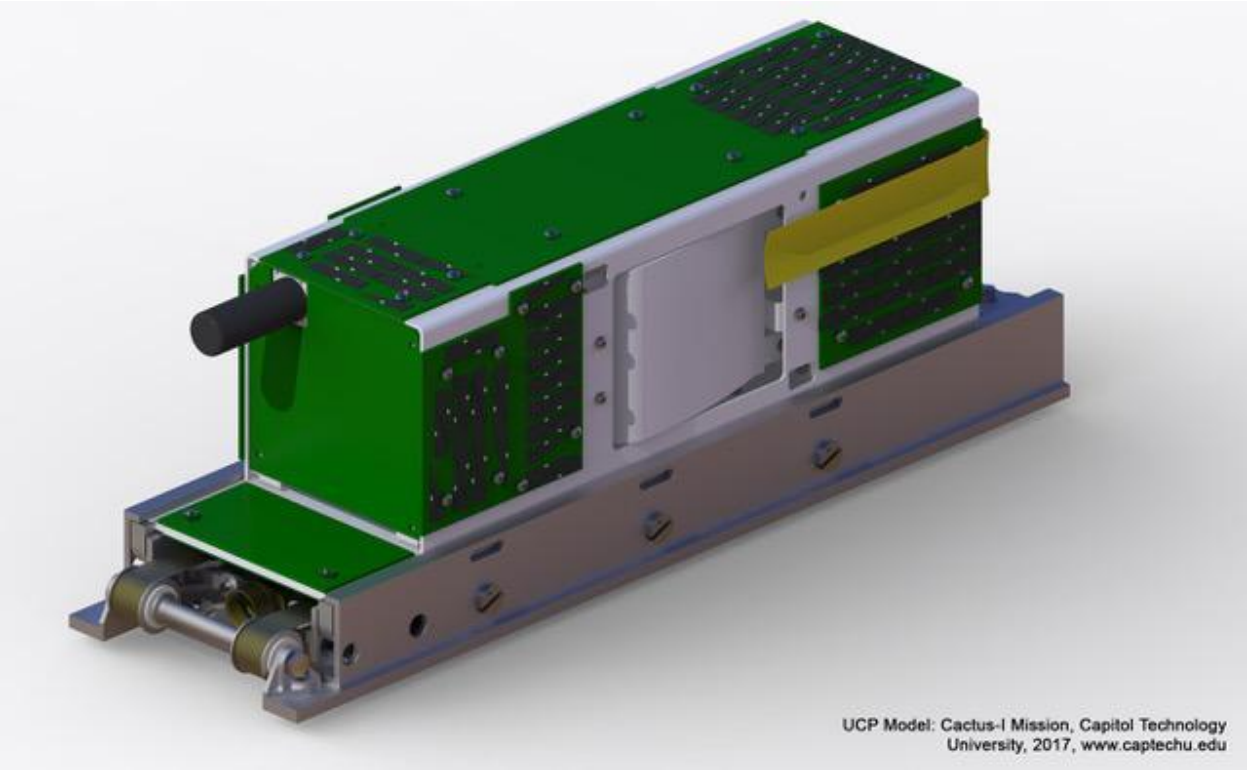
The CubeSat Design Handbook is a product by Robert Pierce Smith.

Acknowledgements: The Cactus-1 mission is Capitol Technology University's first CubeSat mission. Our launch opportunity was provided via the NASA CubeSat Launch Initiative. The Cactus-1 mission is supported by grants from the Maryland Space Grant Consortium (MDSGC).

CACTUS-I Design Documentation and Future Guidance

Pierce Smith

12/19/18



Credit to Xtenti

Contents

Purpose

The purpose of this document is to capture the design of the CACTUS-I CubeSat. The design as well as the designs behind the design will be explained. A ‘Lessons Learned’ will be provided for each section to define what went well and what did not go well. This information is specifically called out in hopes that a future group of student engineers may learn from them and reach higher goals.

Contents

This document will cover Solar, Power, Structure, and Systems design details. This document will not discuss the CACTUS-I ACS, Software, Communications, and ground system in detail, some topics will not be discussed at all. This document will not discuss the paperwork behind the mission; proposal, ODAR, FCC licensing, and MSPSP forms.

Note

Some sections of this document will speak negatively of certain aspects of the project. To clarify, CACTUS-I is a large success because it made it to the launch pad despite the constraints on the students and PI. The point of discussing the failures and negative aspects of CACTUS-I is to improve upon the program and strive for a better CACTUS-II, not to place blame or point fingers. Many faults discussed are ones I see in hindsight and they are often my own mistakes.

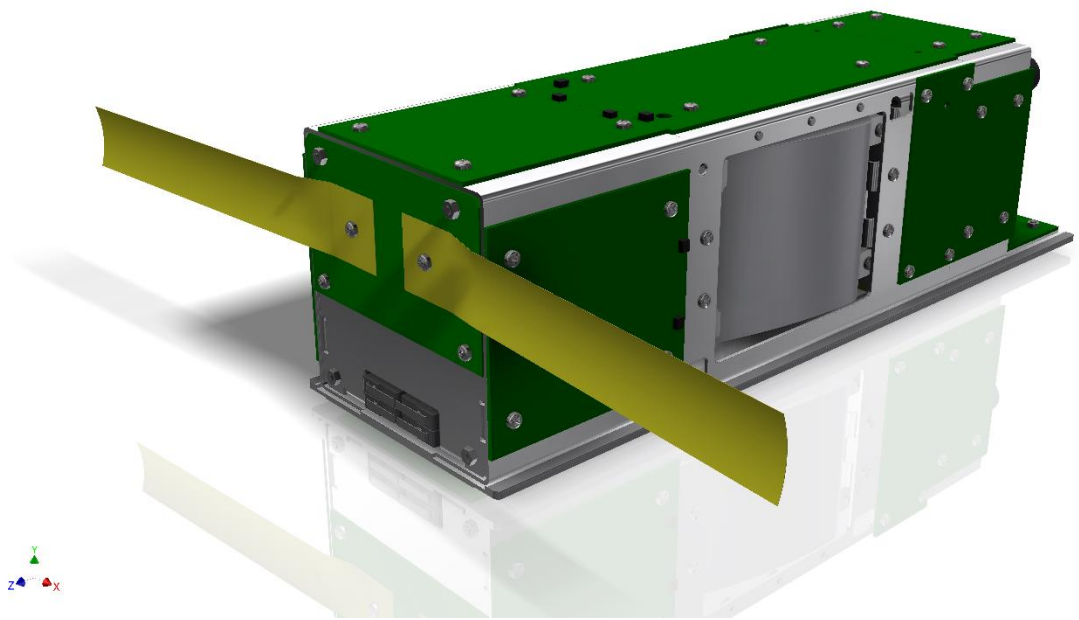


Figure 1- CADD Render of the CACTUS-I CubeSat *Credit to Pierce Smith*

CACTUS-I Overview

Capitol Technology University's CACTUS-I is a 3U++ Tabbed CubeSat, meaning it is 366 x 116 x 113 mm satellite using the new Tabbed launching system (interface details in the structure Section). The goal of Capitol's first CubeSat is to support two payloads that have been developed in the past 3 years; TRAPSat and HERMES. TRAPSat is a debris collection, imaging, and profiling subsystem with the goal to map out debris clouds in orbit. HERMES is an experimental communications payload using the Iridium constellation for uplink and downlink communications. The chosen orbit was a Polar orbit (Altitude undisclosed), driven mainly by TRAPSat's desire to collide with debris which is more common at the poles. The satellite has a planned lifetime of 3 months with extended missions possible as far as the space craft survives.

The CACTUS-I budget was under twenty thousand dollars while the Satellite itself cost about Ten Thousand dollars. No Students or Faculty were paid during the development. All funds went towards materials, tools, and supporting infrastructure built/bought at Capitol. The project was built almost entirely by students. The team size varied from 20 during research, profiling, and brainstorming phase (phase A) to just 5 during the integration and test phase (phase D). The development time started August 2016 with delivery in early 2019. CACTUS-I passed all launch requirement and testing requirement and is approved for launch.

Figure 2, below, is an exploded CADD model of the CACTUS-I CubeSat. From right to left are components for the card stack, TRAPSat Payloads, Frame and solar panels, CACTUS-I batteries, and the HERMES Payload. The card stack consists of the Di-pole antenna and mount, the Aerogel insulation, Comms, EPS, Sensor, CPU, and End mounts. The TRAPSat Payload components are the Mylar Cover, Aerogel payload, Camera, LEDs and Aerogel Capture bay (ACB). The CACTUS-I batteries on the left side are pointed out as the battery case and batteries.

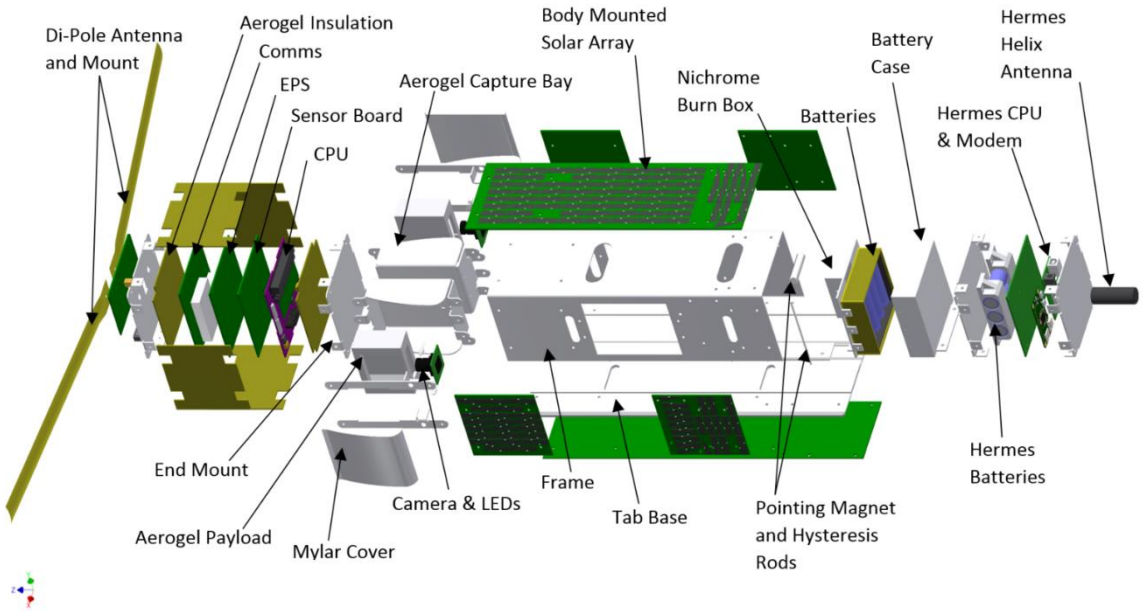


Figure 2 - CAD Explosion of CACTUS-I CubeSat

CACTUS-I System Design

Constraints

The CACTUS-I mission had many risks and constraints affecting Schedule, Cost, and Scope. These are all due to Capitol being a small school with little resources that has never launched a CubeSat before. This risk was well known and understood before starting the project. Additional constraints were set on the project before it began; the CubeSat was to be built for under 10000 dollars and built in 1 year.

It terms of cost, the overall project budget was low. The additional constraint of the CubeSat itself costing under 10000 only added to the challenge. The typical trade study determining buy or build was not effective because almost all CubeSat subsystem solutions cost $5,000 dollars. Buying solutions that were not specialized for CubeSats were also looked at but finding subsystems that met most of the needs was difficult because of the niche CubeSat industry. Much of the budget was spent on supporting resources like soldering stations, test equipment, software defined radios and other radio equipment. To show proportions, two pie charts have been created. Figure 3 below represents the total spending on the CACTUS-I mission. Figure 4 further below shows the spending on just the CubeSat, the total estimated cost of the CubeSat is $9,300, meeting the goal of building a CubeSat in under $10,000.

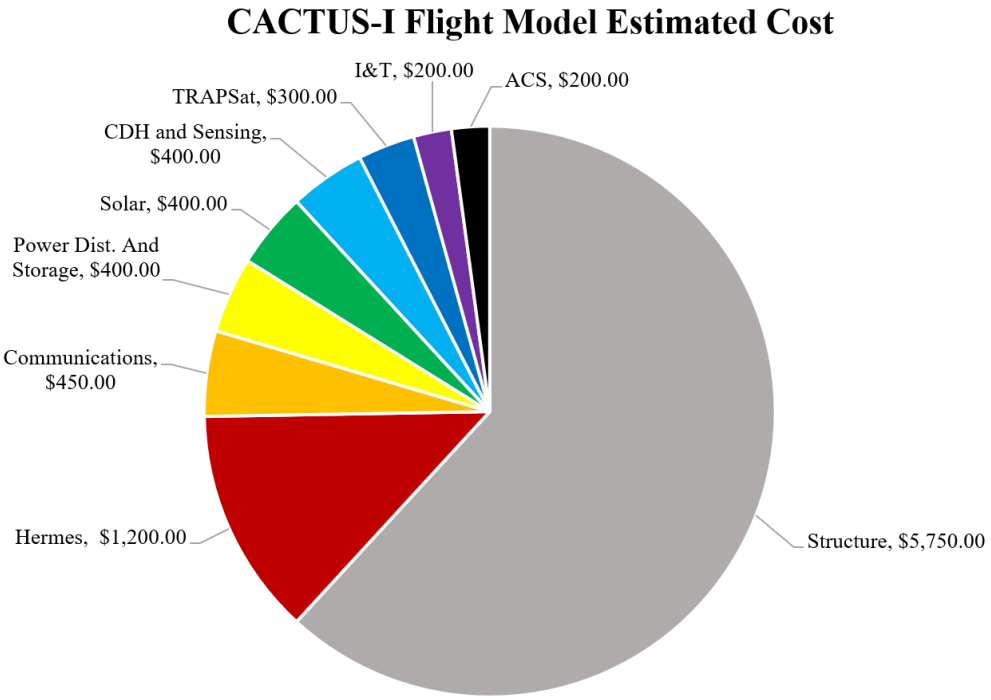


Figure 3 – Pie chart of the estimated cost of the CACTUS-I Flight model. Spending on the subsystems differ between this figure and figure 3 due to buying more components than needed to have back up hardware during development and testing. The total spending on this CubeSat is estimated to be $9,300.

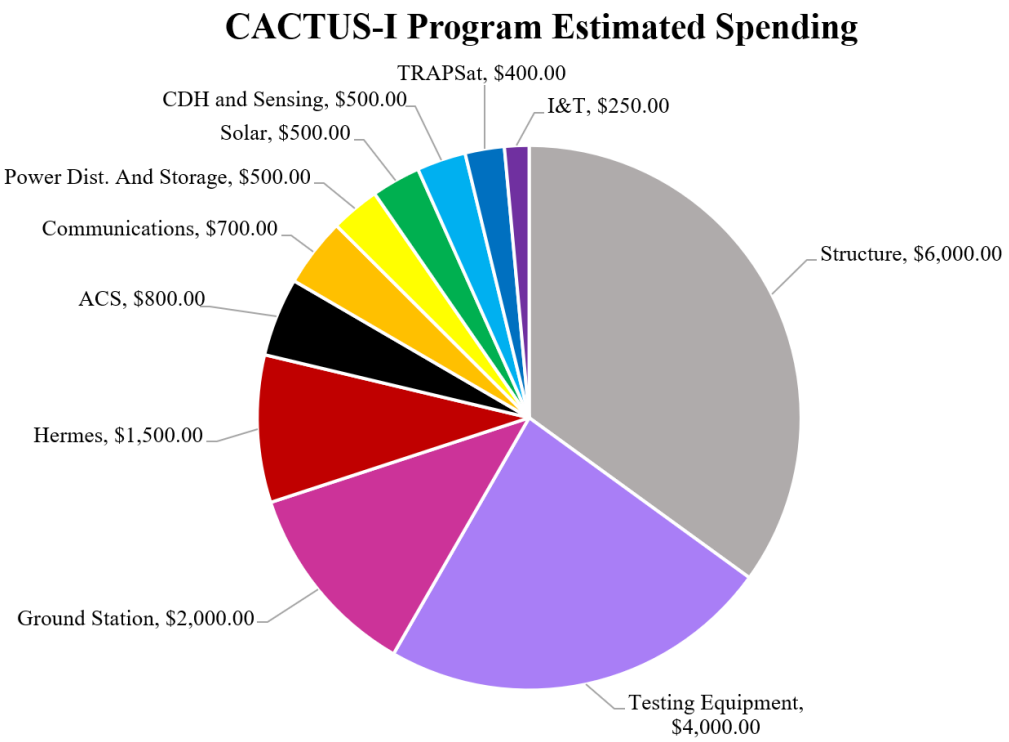


Figure 4 - Pie chart of the total estimated spending of CACTUS-I, accounted costs here estimate spending of $17,150. $150 accounts for some money that was contributed from those working on the project.

Time and Schedule

CACTUS-I Development started in August of 2016 and the delivery date at the time was set for August of 2017. This was an aggressive schedule driven by one of the goals: build a CubeSat in under a year. This goal was a large risk to the project because much of the time during that year would have been taken up by turnaround time from machine shops and PCB houses. Dates for mission delivery slipped and as they slipped, so did the project's end date. This worked well with our development as CACTUS would have been nowhere near done by the original deadline. Many risks that came to fruition contributed to the increase in development time. These risks included a lack of knowledge, the need to be flexible during development, and a decrease in student participation.

The lack of knowledge stems from the fact that the CACTUS-I team was led by sophomores and worked on by sophomores, there were very few upper classmen in the group. Those that led the project had worked on other sounding rocket payloads, giving them some experience in the space field, project lifecycle, and design. These skills were helpful but did not meet what was needed for CACTUS-I. For many students in the team, this was their first large project where there was design work to be done. Many students were new to large extracurricular projects which led to students learning as they went and experienced students spending time to teach new students rather than continue development. A lack of knowledge caused many subsystem designs being underdeveloped or containing mistakes, leading to rework. Mistakes created the need to be flexible in terms of what gets worked next, to cope with rework. The Gantt chart above shows work on many subsystems being dropped in favor for others and being picked

up again later. This was also done because no subsystem was fully defined from the start of development. Work needed to be halted in one subsystems and started in another in order to define the interfaces between to the two to continue design on both fronts.

As time progressed, students either lost interest in the project, felt that their involvement was no longer needed, or they had to stop working because of school work. As student labor began to dwindle for certain subsystems, development stopped all together. This can be seen by design items being worked in series rather than parallel. Those that remained on the team worked one subsystem at a time before moving to the next.

Scope

The scope of the CACTUS-I mission was one of the biggest hinderances. The problem with the scope of CACTUS-I was the goals that it attempted to achieve; built in one year and for under $10,000. These two goals set the stage for the rest of the project: rushed. CACTUS-I is capitol's first venture into the CubeSat space. Creating a functioning CubeSat is enough of a challenge for a first-time university, what added to the challenge was the very aggressive scope.

To keep with schedule, CACTUS-I needed to be quickly designed, fabricated, integrated, and tested to meet the launch date in one year. This goal was unachievable from the start but was only realized partway through the design process. The project got a much-needed break from the many schedule slips of the launch provider. This provided the project with needed time to complete the build. Without these schedule slips, CACTUS-I would not have been ready for launch.

The goal of completing the CACTUS-I build for under $10,000 was fitting given Capitol's reputation of delivering performing systems on a very low budget. The reputation that is being referred to is Capitol's students' ability to build low cost sounding rocket payloads that still achieve high levels of success (even in the event of a rocket failure). But as stated before, CubeSats are a new project space for Capitol. By holding the build budget to $10,000 it limited the project's ability to 'Buy or Build' solutions. The commercial CubeSat market is very niche, so finding solutions that are not expensive qualified flight hardware is challenging. Despite these challenges, the CACTUS-I CubeSat was built for just under $10,000, meeting its goal.

Design Choices

Attitude control system

The general requirements for the attitude control system were to keep the TRAPSat system pointed in the direction of the velocity vector and enable communications when desired. Other drivers included minimizing cost, complexity, and the SWaP properties of the subsystem. The type of subsystem chosen was a Passive Magnetic Attitude Control (PMAC) system. This type was chosen because it required no input power, it did not take up much space or mass, and it did not require any form of commanding or control. A PMAC system is operationally simple but very complex during development. Simulation (through MATLAB) is required to determine

exactly how much hysteresis mass to put in each axis and how strong the dipole of the pointing magnet should be. These parameters required many simulations to determine the proper amount. This increase in complexity during development was accepted because simulations could be run overnight, and students could work on other tasks while ACS was being simulated.

This PMAC system was able to meet the needs of the TRAPSat science payload by keeping the CubeSat aligned with the magnetic field lines of the earth, the satellite would flip 180 degrees when going over the magnetic poles, but this was accepted because of the cheap and elegant solution that PMAC was to the mission. This imposed another constraint of the CubeSat from the science payload; the TRAPSat payload needed to be mounted on both sides of the CubeSat so that one payload is facing the velocity vector at all times.

Power systems

The CACTUS-I Power subsystem requirements were very open ended because not many portions of the satellite were defined. The solution must provide power for a Raspberry Pi and the communications subsystem. The subsystem must follow the PC104 standard, physical is required, electrical is preferred. The solution must be low in complexity as not many students are experienced in electrical engineering and design.

The need for a PC104 size leads down three avenues, buy, build from another university, or create in house. Buy is out of the question as buying space craft subsystems is too costly. Building from another university was considered, many designed were looked at from other universities but the issue was that there were almost no solutions that were fully documented, allowing Capitol to replicate the design. This led eventually to building in house. Originally the design for the power board came from the company inter orbital CubeSats free of charge. This design was chosen because the communications solution came from the same company, meaning that two subsystems were more likely to work, making integration easier. The board was simple for teammates to understand, it supplied exactly what was needed to the communications system, and it could be replicated at about the same price for an in-house creation. The board did not meet the required 5V supply for a Raspberry Pi so the design was modified once received from the company. During development it was realized that the inter orbital design suffered from the same problem as the university designs, not enough documentation. The power board was changed heavily over time, making different functions more efficient and reliable and meet the missions needs exactly.

The batteries used in the power system were a simple choice. 18650 cells were purchased from Panasonic (part number NCR18650B), as recommended to the team from an experienced professional. Power storage most definitely had to be a buy solution for the power subsystem.

Mechanical and Physical

The Mechanical subsystem had major constraints relating to the deployment system as well as the launch provider. These constraints were mainly vibrational, physical size, and surface

characteristics. During development the structure subsystem was given priority as it would be the most expensive and have the longest turnaround time. During early concept design many CubeSat frames were found for sale. These frame costs were used as an estimation of cost for the custom structure to be built for CACTUS-I. It was understood that should the custom design exceed that cost estimation; a commercially available frame should be purchased. A design from Planetary Systems was used as inspiration; a single part was used to meet the mating requirements of the tabbed interface between the launcher and the CubeSat. Thus, vibrational and physical size requirements flowed to the rest of the CubeSat Structure parts. With this allocation, all parts needed to meet the physical size and vibrational requirements but only one part needed to meet the tabbed interface requirements as well. This reduced cost as only one part needed extremely high specifications while others could lack tolerances that were not needed.

The design of the mechanical system was also the design of the physical layout and location of all components. The TRAPSat payload required to be facing the velocity vector

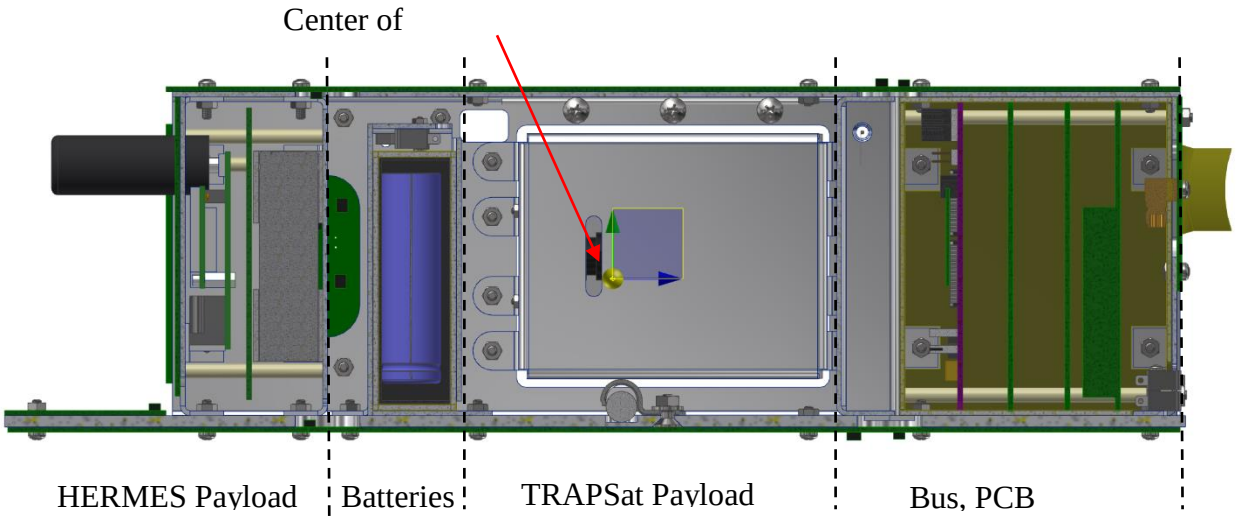


Figure 5 – Half Section view of CACTUS-I, revealing the distinct regions of the CubeSat

during orbit. The mechanical design was laid out such that the axis of the PMAC pointing magnet aligned with the TRAPSat Payload's. This meant that there was a TRAPSat payload on the front and the back of the CubeSat. With the HERMES on one end of the CubeSat the TRAPSat payloads were placed in the middle. The TRAPSat payloads are very light so placing them on the opposite end the HERMES Payload would shift the center of gravity towards the HERMES end. Placement was an effort to balance center of gravity for the space craft. The End opposite to the HERMES payload is where the PCB card stack was placed. As a final effort to balance the center of gravity the batteries for the PCB Card stack were placed next to the HERMES Payload.

Lessons Learned

What Went Well

Successful 'Final Push Efforts' by hard working students to complete milestones.

Last push efforts occurred when the team needed to complete a task by a certain time to meet an internally prescribed deadline or milestone. The team members that stayed on CACTUS-I were hardworking and would meet the challenge to come to the lab to work for the whole day and night with the rest of the team. These times were often the most productive and most fun, keeping teammates coming back. Final Push Efforts occurred often as this type of progress is common with University programs because students still have to attend class and complete homework. Students focusing their effort on one day synchronously is extremely beneficial. Each Final Push Effort had great results. Internal deadlines were often not broken.

It is critical to find the right type of students for a project. The types desired, and the ones that stuck around, were the students that showed up reliably and worked. Sometimes these students had very little experience and other times they had a lot. The experience didn't matter in the grand scheme. What was important was that the students showed up every time, stayed in the loop, and became knowledgeable on the CubeSat. These hardworking students are what make last push efforts and projects like CACTUS-I possible and successful.

Adaptation of designs and future proofing work helped keep the program rolling and keep schedule slip to a minimum.

Future proofing work is giving a design the flexibility to change configuration and adapt to problems, troubleshooting, or new designs. Consider two configurations, each has its tradeoffs and there has not been a conclusion as to which is better. To keep the program moving forward the design would be done in such a way that both configurations can be supported. In the case of structure and mechanical it's imperative to get the design correct the first time so that nothing physical needs to be reworked. Physical rework costs time and money. This is less apparent on the software side as it only costs time. Student labor (or PI labor) is cheap. Future proofing structure and PCB designs was critical to keeping those subsystems on track.

In typical engineering, a waterfall style of approach, it's more important to know exactly how everything will fit, form, and function together. A CubeSat will often have unexplored territory within its own design space, leading to discovery of work. This unknown can cause long holding patterns in a typical engineering process. Future proofing designs allows for the program to continue into those unknown spaces with a design that can adapt and support many configurations. This modular, adaptive approach is seen more in software development under the Agile design process although, it can be applied to more technical areas. CACTUS-I development fits a very loose Agile workflow. This workflow was necessary for keeping the program moving.

What Did Not go Well

Design choices involving heritage were not properly analyzed.

In class, students are taught that heritage is an important component of a space craft design, without heritage a design has no merit and no verification of performance besides ground testing. This of course is a bad thing, except in the CubeSat world. CubeSats are meant to be experimental, thus not many CubeSats will have heritage. Throughout development many decisions were derailed or put on hold as a lengthy discussion or civil argument over heritage took place. These discussions sometimes resulted in a good outcome and other times did nothing but slow down key decision making. Heritage can help a mission reduce the amount of work to be done to finish the build, but it can also hinder the project as well if there are better methods, product's ect. available. The key problem was that not enough analysis was done to make some of these key decisions. A heritage design would often win over another design simply because it already existed and worked once. Documentation of a past design was typically minimal and therefore cost the program time.

When heritage was involved in design choices, decisions were made fast because team members were led to believe that a heritage design was the best choice. This mentality led to a lengthier I&T process because old or bad documentation led design astray or did not provide the needed details. In the CubeSat space, it is important that a team challenges a heritage idea the same way it would challenge any other idea. In reflection, very little of the design was looked over from a heritage perspective. There were very little questions asked about 'What's inside?' Although, these questions may not have been asked due to program issues not on the CACTUS-I side. For CubeSats, a good idea, a decent design, decent testing, and documentation to back it up will be more than enough to fly.

CACTUS-I Structure Design

Major Design Features

The CACTUS-I structure has 4 primary components; The Tabbed Sled, the Bus Shell, the TRAPSat Shell, and the HERMES Shell. The Tabbed Sled received its name because it stretches the entire length of the CubeSat, serves as the mounting platform for all CubeSat components and is the interface to the launcher. Each shell represents 3 sides of a cube where the fourth face has small flanges that allow it to slide on the Sled, see figure 6 for a shell model. The Tabbed Sled has channels that are 0.06 inches deep, allowing the flanges of the bent metal shells to sit flush with the top surface. The shells are fastened to the sled with no less than 4 screws.

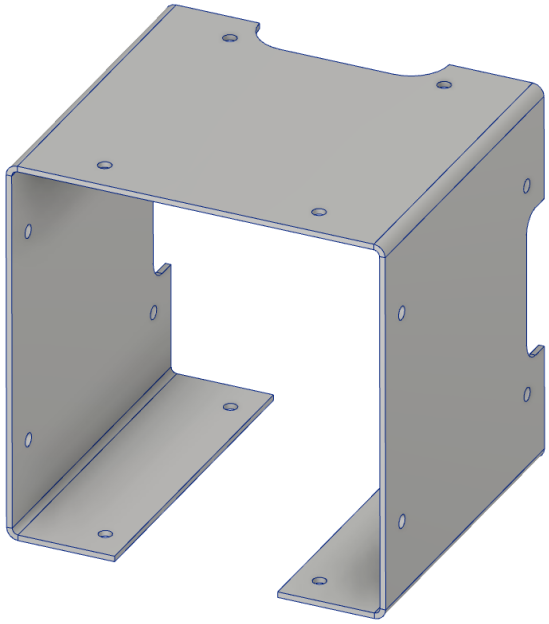


Figure 6 – the Tabbed sled CADD model from the CACTUS-I project. The two channels on either side of the mounting plate is how the main components, the Shells, are aligned and mounted.

The shells allow for modularization as each segment of the CubeSat can be constructed independently and integrated electrically on the bench, then mounted together physically. A shell only covers three faces of a cube with the fourth face containing flanges. This fourth face is properly covered when mated to the Tabbed Sled. The top and bottom (or front and back) of the shell will not be covered. This is left open in the case of the TRAPSat Shell to mount large components inside. The HERMES and BUS Shells are closed off by End Mounts, which allow for PCBs to be mounted safely. The shell is also used to mount solar panels, which cover most faces on the spacecraft.

Space is very tight within the CubeSat so one screw may be used to hold together many components. For example; A screw used in the BUS Segment is inserted from the outside of the space craft through a solar panel, through the Tabbed Sled, through the BUS Shell, and through a metal end mount where a press nut is attached, thus fastening all components to each other. This type of fastening is how solar panels and shells are fastened to the Tabbed sled. This is also how a solar panel, Shell, and End Mount are fastened together. This leads to less wasted space due to fasteners but increased integration complexity and time as three components are being fastened at a time.

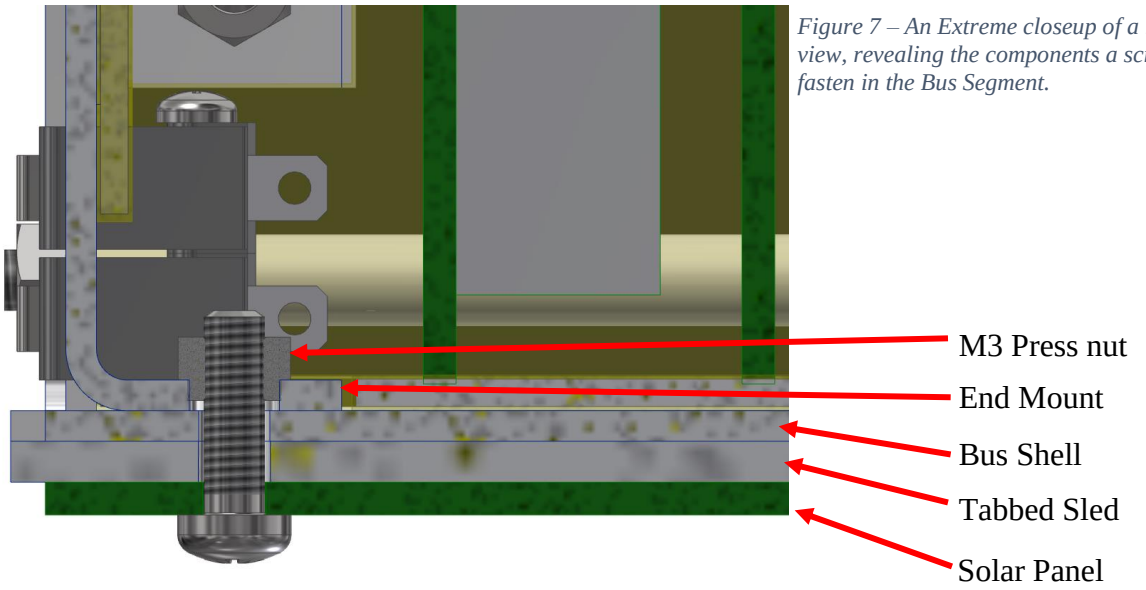


Figure 7 – An Extreme closeup of a half section view, revealing the components a screw is used to fasten in the Bus Segment.

Overview of Interfaces with Launch Provider

All references to X, Y, Z dimensions are based off the FANTM-RAiL™-Tabbed 3U Single (FRA-T3S) Attachment/Deployment Assembly Interface Description Document (IDD) provided to the team from Xtenti. The Tabbed deployment method is a new form of CubeSat deployment. CACTUS-I will be using the FANTAM-RAiL-Tabbed 3U Single (FRA-T3S) system developed by Xtenti. This system will hold the CubeSat by two hard anodized tabs and deploy by pushing with a constant force from a pusher bar located on the -Z Face.

The CACTUS-I Tab interface has extremely tight and specific tolerances as well as a hard-anodized surface. The nominal values of dimensions were used in CAD designs, these interface constraints were defined first before other design choices were made. The CubeSat was constrained to a maximum length of 113mm in the X direction and 116mm in the Y direction. To keep the design similar to CubeSat designs already existing, the CACTUS-I structure was chosen to be 100mm x 100mm in the X and Y directions, leaving space (6.5mm per face at least) for solar panels to be mounted to the surface. Performance parameters of other CubeSats can be related to CACTUS -1 with ease as less has changed between designs.

Many design choices were guided by Planetary Systems documentation because within the IDD, Xtenti directly references the Planetary Systems CubeSat specification as being the target satellite for deployment:

> "… designed for up to a tabbed 6.0 kg (13.2 lbm) 3U UCP generally adhering to the Planetary Systems Corporation (PSC) Canisterized Satellite Deployer (CSD) specification."

Following the CSD specification from Planetary Systems was the best course of action in order to keep interfacing issues to a minimum with the Xtenti FRA-T3S deployment system.

Material Choices

The Tabbed interface was chosen to be made of one machined plate of Aluminum 7075, 3mm thick, as recommended by Planetary Systems (Give Ref). The 3mm thickness was chosen to match the nominal dimension for the tabbed interface. The material was chosen because: 1) The majority of the FRA-T3S deployment system is made of Aluminum 7075, matching materials is desired for the same physical characteristics and behaviors (thermal expansion for example). 2) The harder Aluminum 7075 will hold up better than the standard Aluminum 6061 against any wear and tear from handling, fit checks, and testing. Reducing the chance for the Interface to fall out of tolerance over time.

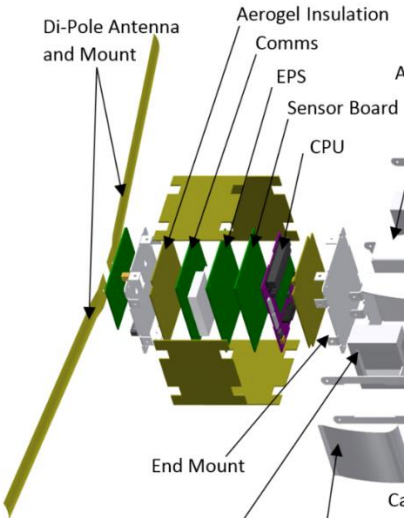


Figure 8 – A direct Copy and Crop of Figure 2, with a focus on the left-hand side of the graphic. The Card Stack.

The rest of the frame was constructed with bent metal of thickness .06" and material Aluminum 5052. The thickness was primarily based off the Pumpkin CubeSat bent metal 1U frame as well as other CubeSat frames. The material choice of Aluminum 5052 was recommended to the team by a professional experienced in manufacturing. 5052 is more pliable and easier to bend than the harder 6061 and 7075. This leads to less cracks from bends and more dimensional accuracy post bend. Bending will create stress within the metal, over time this stress can be released, moving drilled holes out of place. It was explained to the team that hole features on 7075 can 'walk' over time and drift in dimensional accuracy.

The material of fasteners were typically Passivated 18-8 Stainless Steel because keeping as many components nonmagnetic increased the accuracy of magnetic attitude control simulations by reducing the real world 'noise' that could be created. PCB spacers are another primary component, separating PCBs from one another and giving clearance. The Material of the spacers flown is Nylon 6/6. Material was not a main driver for spacers, Nylon was chosen because of how custom the solution needed to be. Spacers that were 52 mm long were purchased and cut to the proper length. This saved money as spacers can be very expensive and it provided the custom lengths needed to meet the needs of the Card Stack design.

BUS Segment

The BUS segment is comprised of the BUS shell, the Card Stack, the Antenna PCB, and the corresponding solar panels. This segment is located on the end of the CubeSat, the -Z side. The Card stack is a stack of PCBs with End Mounts on the top and bottom, the antenna PCB is mounted on the outside of the top End Mount as it holds the Tape Measure Antennas. The bottom end mount is unique because it has a small chamber where the Nichrome burn will occur to deploy antennas. The Antenna end mount faces the exterior of the Space craft while the Burn end mount faces the interior, towards TRAPSat. This chamber is sealed off from the inside of the

cord stack with Kapton tape and Mylar blanketing. The PCBs and End Mounts are separated and organized by long threaded rods running through the corners of the PCBs and spacers. Spacers give each PCB enough room top and bottom for soldered component clearance and wiring clearance. This stack is rotated sideways and inserted into the shell. With the End mounts and shell the card stack is covered on all faces except the bottom, which is where the segment is mounted to the Tabbed Sled.

TRAPSat Segment

TRAPSat is comprised of a the TRAPSat Shell, two Aerogel Capture Bays (ACB), the battery box, and corresponding solar panels. The TRAPSat segment is an open design where there are no end mounts on either side and there are modest openings in the Shell where the ACBs are mounted. The ACBs are mounted on either side of the TRAPSat Shell by 4 screws each. The Battery Box is only mounted to the flange portion of the TRAPSat shell via 4 screws as well. Because the box is only mounted on the flange of the shell, it is not truly fastened until the shell is also mounted to the Tabbed Sled.

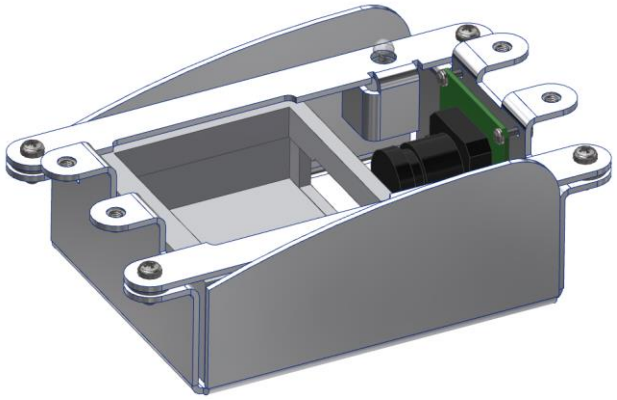


Figure 9 – A CADD Model of one of the two TRAPSat Payloads mounted on either side of CACTUS-I.

HERMES Segment

The HERMES segment is comprised of the HERMES card stack, HERMES Batteries, the HERMES Shell, and the corresponding solar panels. This design is very similar to the BUS Segment but shortened considerably to mount a static helix antenna. More detail on this design can be found in CADD models and other documentation from the HERMES Team.

Thermal

Thermal characteristics where not heavily considered because at the orbit CACTUS-I will be at, the temperature will stabilize between -10C and 10C. Mylar blanketing and Hybrid Aerogel insulation are the primary insulative materials used on CACTUS-I. Mylar Blanketing was used to cover the outside of the space craft to provide thermal insulation and good reflective properties. This blanketing was used underneath the solar panels as well because it is nonconductive, helping combat potential short circuits between a solar panel and shell, and because it could reflect heat shunted from the panels into the CubeSat. Hybrid Aerogel insulation packets were used to insulate the BUS segment of CACTUS-I on all faces. TRAPSat segment does not use insulation except for the battery box mounted within. The Battery Box uses the same insulation on all faces, protecting the sensitive batteries from temperature swings.

Both thermal materials were mounted with double sided Kapton tape. This tape was used sparingly because the adhesive had a high outgassing percentage, making it dirty and difficult to use in a clean vacuum chamber. Using too much of this material would have hindered the ability to test CACTUS-I in a vacuum chamber.

Vacuum

CACTUS-I holds no pressurized containers, therefore each closed volume within CACTUS-I must vent within a certain amount of time. Each segment with a closed volume has enough open surface area to meet the venting requirements. The BUS section has open areas facing the TRAPSat segment. This was done because the TRAPSat segment has more than enough open surface area to vent itself and other closed spaces. The HERMES Segment has a thin but wide opening along the bottom of its exterior end mount, venting air directly into space.

Lessons Learned

Lack of tolerance between end mounts and Bus Shell affected the procedure for assembly but did not have any lasting negative effects

The clearance needed between the end mounts for the card stack and the Bus Shell were not considered in design. During integration, the card stack assembly could not be inserted into and through the Bus Shell because the End mounts were slightly too large. The end mounts could be inserted to be flush with the edge of the shell (as designed) and not farther. The original procedure had the full card stack assembly inserted. The modified procedure used to complete integration was to take off one on the end mounts, insert the card stack into the shell such that the end mount was flush with the shell, then the other end mount was put back on. During testing and fit checks, the assembly had to be taken apart. Clearance between the end mount and the shell became more reasonable but still required a modified assembly procedure. Tolerance between the end mounts and the shell should be considered. The end mount sizes should be reduced to allow clearance for the card stack to be inserted.

Screw heads and Nuts that protruded from the antenna PCB on the -Z face needed to be shaved or sanded to meet the physical requirements.

The outside of the card stack is where the antenna board is mounted. Screw heads and nuts protruded from the surface of the PCB. The Card stack and bus shell were recessed from the edge of the tabbed sled to ensure the protruding component did not violate the physical specifications of the CubeSat. The shell was not recessed enough because after build, the screw heads and buts protruded into the keep out zone on the -Z face. A Dremel was used to sand down the items and bring the CubeSat back into spec.

To keep this from happening, a low-profile nut and screw should be used on the outside of the card stack. The recessed card stack may also need to be re-evaluated to determine if it

needs to be recessed further. A method of fastening the card stack together may also provide a more elegant solution to the problem of protruding components.

CACTUS-I Solar Design

The CACUTS-1 Solar panel solution consists of PCB's of varying size and small solar panel chips strung together to form a large panel. The output of these panels for the BUS and TRAPSat segment ranged from 10 to 13 volts. The size determined the amperage output, the smaller panels produced 40 mA at peak while the largest produced 200 mA at peak. The HERMES Segment uses a different voltage level, the output of these panels ranges from 8 to 11 volts. The amperage output of these panels ranges from 40 mA at the smallest and 100mA at the largest.

Materials

The chosen solar panels are small chip cells provided from TrisolX. These small cells were recommended because of high efficiency and dollar cost per area. These chips are the byproduct of cutting a large square panel out of a circular silicon wafer. See figure 10, right, for size.

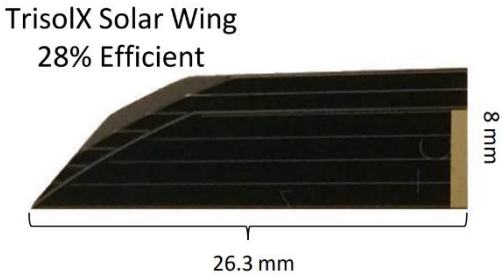


Figure 10 - TrisolX Solar Wing Chip product used to create solar panels. A total of 260 chips were used on CACTUS-I

CACTUS-I used leaded solder paste and solder (37 percent lead) to mitigate the risk of Tin Whiskers. Whiskering is not a well understood phenomenon that can be observed in most elemental metals and some alloys. Whiskering is more common with aged hardware and Tin Whiskers specifically are more common on hardware below 13 degrees Celsius. Figure 11 shows the potential of Tin Whiskers; the whisker pointed out is 18mm long and electrically connects one area to another. The mitigation of using leaded solder will drastically reduce the chances of whiskering to occur and whiskers to grow long enough to connect to another contact on a PCB. Figure 12 shows the difference leaded solder can make. The component has two leads that are tin plated, the lower portion of the lead was dipped in a leaded solder.

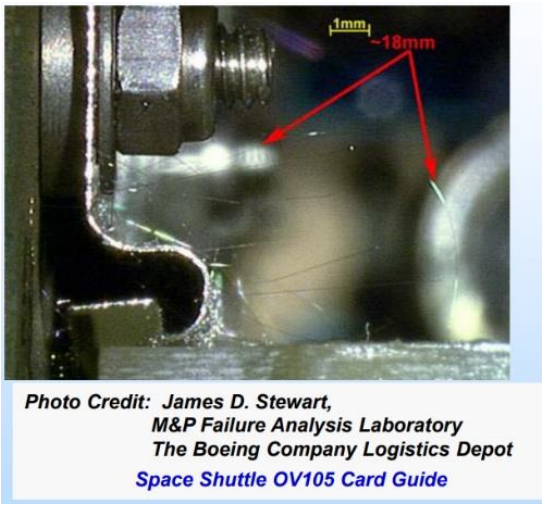


Figure 11 - This image shows long Tin whiskers that have grown long enough to contact another surface, 18mm long. This example shows that Tin whiskers have the potential to erroneously connect circuitry.

Another mitigation used was conformal coating of solder joints. Dow Corning 732 RTV Silicon Sealant: Clear was used for the conformal coating. A coat of less than 1mm was used on exposed solder joints.

Each solar panel also had a set of low drop diodes on each panel. These diodes prevented any forms of feedback into shaded panels. The power board that CACTUS-I used also had diodes for each panel input so the diodes on each solar panel ended up being a redundancy. A low drop diode is preferred to keep voltage losses to a minimum.

Figure 12 - The crystal oscillator component above has leads that are Tin plated. These leads were dipped in a Sn/Pb based solder. Over time the Tin-plated section of the lead developed whiskers while the Sn/Pb dipped section did not. This shows the importance of using Sn/Pb based solder to prevent shorts and chances of failure. Credit to Michael J. Sampson

Direction on Manufacturing

PCBs were created in Eagle, a PCB creation tool owned by the Autodesk Company. This tool was chosen because it is free, easy to understand, and members of the team were familiar with this tool. The physical PCB was manufactured by a professional company.

To the right is an image of the Eagle layout of one of the solar panels. A gray-Red color represents exposed solder pad, this exposed pad shape almost matches the contact surface of the solar chips used. There is one corner of the solder pad that is removed, this was done to reduce the number of erroneous contacts from the bottom solder pad to the top contact of the solar panel. The chip itself is very thin and in testing it was very easy for exposed solder to connect to the top contact. The goal was to reduce the number of erroneous connections as fixing them took time and there was a high number of solar chips that needed to be soldered. Board traces are kept at a 16 mil width because of the relatively low power the solar chips will provide. Because trace space on the PCB is not a rare commodity thicker traces could have been used and is recommended.

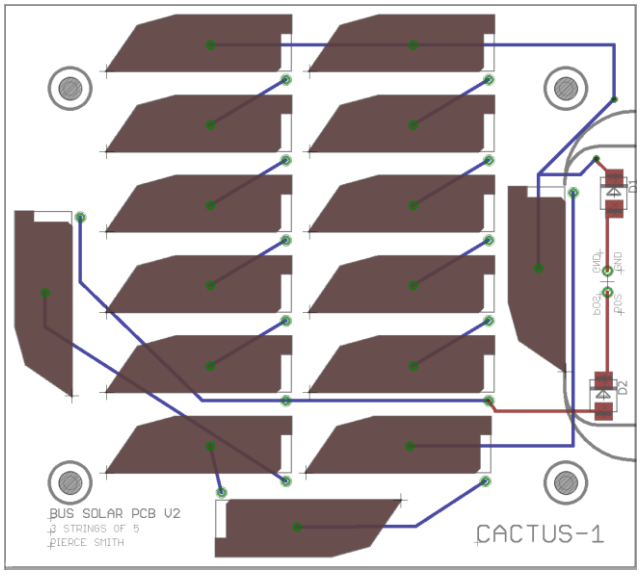


Figure 13 – Eagle board layout of the Bus Solar Panel V2. Top copper is red, bottom copper is blue, vias are green and silkscreen is grey.

The Process for creating a solar panel will be explained below.

1. With the boards in hand they were cleaned with isopropyl alcohol, front and back. The pads especially were cleaned as they were dirty due to the manufacturing processes.
2. Solder paste was applied to each solder pad. About a centimeter or more of solder paste was applied to the pad. Excess solder will be removed later.
3. A heat gun, on high, was lightly waved over the solder paste to liquify most of it. Heating continued until the paste fell from mostly solid to mostly liquid. This took about 5 seconds for the paste and heat gun used.
4. Solar chips were dropped onto each pad. Dropping from a centimeter off the PCB was the best strategy found as our fingers would not touch the solder paste and dirty the top of the solar chip.
5. The reflow oven was preheated and prepared with the heating profile used for the 37 percent leaded solder paste being used. If repeating this, use the manual that came with your reflow oven to see what heating profile should be used with your solder paste.
6. The PCB was placed inside the reflow oven when ready and the oven was started.
7. After reflowing has been completed the board was given time to cool off. Then the board was flipped over to wick away solder bubbles on any Vias. Isopropyl alcohol was used to remove the flux around each chip on the front and remove flux from each via on the back. Solder paste contains flux and as the paste is baked the flux flows out and away. This step should be performed within 8 hours after reflowing to reduce the chance of flux staining the PCB color (looks are super important of course).
8. Each chip was then heated with a heat gun to be flowed into the correct position. This is where the downfall of the PCB design is realized. The corner of the solder pad removed affected the surface tension of the solder, making the panel flow into a different spot on the pad. Each panel needed to be readjusted. This readjustment was done as part of removing excess solder. Extra solder would sit under the solar chip and raise it off the surface of the PCB. By using tweezers and gently pressing down the panel excess solder is pushed out. A wick can be used to remove the excess solder on the side. This process was easily accomplished with 2 people. One heating the chip and another adjusting the chip's position.
9. The board was cleaned again, especially the tops of the solar chips
10. Wire jumpers were bent into an L shape to be soldered to the top contact of the Solar chip and the via placed next to the solar chip. The top contact was soldered first. The small portion of the L was placed on the solar chip top contact with the long leg placed in the via. The soldering iron was used to heat the wire while solder was fed onto the top contact pad. Solder tends not to grab the top contact pad right away, so practice is recommended to understand how to apply solder to this contact. This contact is a very thin layer of metal which can ablate off the solar chip if heat is held too long. When the top pad is removed, solder will no longer hold to the pad and the pad color will look silvery black. The chip will need to be replaced if this happens. The board was flipped over and the wire was soldered to the via. Heat was not applied for long to prevent heat creeping to the top contact and de-soldering. This process was repeated for each of the solar chips on the board.
11. The panels were cleaned again with isopropyl to remove solder material from the surface of the solar chips.

12. Low drop diodes were installed on either the front or back of the PCB, depending on the design. Flux and other material were cleaned off the diodes

Efficiencies

Each Solar chip had to be separated from each other to prevent short circuits, this leads to wasted space around each Chip. While these solar chips have a relatively high efficiency of 28 percent, the low packing efficiency of the PCB most likely offset this. The table below details the expected performance and efficiencies of each panel design. The Packing efficiency of the CACTUS-I solar panels is quite low, averaging around 32 percent. The total wattage potential of CACTUS-I is not calculated because it would be impossible to realize in operation. The efficiency of the cells used in calculations is 28 percent and the wattage per area used is 1390W/m^2. From these numbers is can be estimated that with full sun on one side, CACTUS-I can experience a solar power of 1.2 W (Bus panel plus the Pin/Blank Side panel) or 2.7 W (Bus panel plus Large Panel). The large difference in performance is due to the total area valuable for solar cells. The TRAPSAT payload took about 110 cm2 of usable surface area on two sides. With the proper orientation of the satellite, most direct sun will hit the higher performing sides of the CubeSat.

PCB Name	Bus (x4)	Large (x2)	Pin Side (x1)	Blank Side (x1)	Total
PCB Count	4	2	1	1	8
PCB Total Area per Panel (cm^2)	72.45	148.94	36.00	36.00	659.69
Solar Chip Count per Panel	15	40	10	10	160
Total Active Chip Area per Panel (cm^2)	19.50	52.00	13.00	13.00	208.00
Packing Efficiency (%)	26.92	34.91	36.11	36.11	0.32
Predicted Power Output per Panel (W)	0.76	2.02	0.51	0.51	

Lessons Learned

Pad geometry led to manually rework of each cell, costing a lot of development time.

During the construction of the solar panels, the largest drawback to the design of the PCBs was the geometry of the Pad. As mentioned before, the corner of the pad was covered by solder mask in hopes to reduce the chances of a short circuit between the jumper wire and the pad, see figure 14. This design choice ended up being a large time sink because after placing solar chips and reflowing them in an oven, the chips would be offset from the desired positions due to the surface tension of the solder. Because the corner of the pad was removed there was lack of surface tension in that location, causing each solar chip to shift away from the corner. The Pad of the solar chip used in the PCB designs should be edited to include the corner

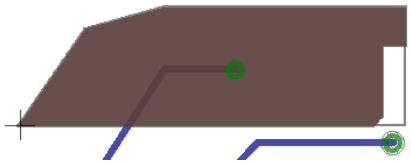


Figure 14 – PCB design view of a solar chip pad. Notice the bottom right corner of the pad does not have solder, dark red. Because solder could not grab at the corner of the pad, the solar cell would come to rest at a crooked position. This required manual rework to fix each cell.

as copper once again. By doing so, solar chips reflowed will come out sitting in the right spots, ready for the next step of assembly.

The solar chip product used to create the solar panels led to a long and tedious build process.

There are a total of 260 solar chips used on the CACTUS-I mission. Each chip required manual rework and jumper soldering to function properly. A lot of development time went toward constructing these solar panels. These chips are expensive, small, and efficient. The small size meant that many would be needed to create one full solar panel. The small size also meant that the area available for solar panels had a lot of wasted space between cells. The high efficiently of the cells was nullified by the amount of wasted space between cells. The design of the solar panels should be reworked to use a different solar panel product. One that is physically large and consequentially more expensive. Seeking solar panels with a lower efficiency would be an excellent way to reduce costs. The outcome of this modification would most likely be a small increase in the yield of each solar panel due to better packing area efficiency despite a lower conversion efficiency. This would also reduce the amount of work and time needed to build the solar panels, allowing effort to be focused in other areas.

CACTUS-I Power Design

CACTUS one power board was a solution reworked many times. This subsystem was heavily affected by the lack of knowledge and support. The power design originated from the inter orbital CubeSat kit. This board was chosen as a baseline because it came from the same system as the communications board, theoretically making integration easier. This was chosen because after many weeks of research, this seemed to be the easiest design to understand, build, and improve upon. The design had three main sections to it: Power input and cleaning, charging, and power distribution. Of the pieces reworked, the charging section was modified to fit the battery design of cactus 1 and the power distribution section was also changed. The power input and cleaning stayed the same, although, 2 inputs were added to the chain to match the number of solar panels on CACTUS-I.

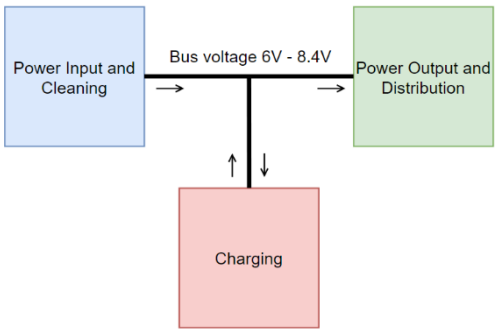


Figure 15 – simplified view of the electrical system design.

Design Overview

The power design is very simple. It relies on three sections that are each interconnected. The bus voltage of this design is driven by the current battery voltage. This means that all inputs and outputs must be regulated to account for the lack of control in the central power distribution.

The graphic above is a greatly simplified form of this design. Input voltage can go to either the battery for charging or it can flow directly to power distribution. This is a partially regulated system where bus voltage changes over time and all inputs/outputs must be regulated. Originally the design used li-ion batteries in parallel leading to a bus voltage of 3V to 4.2V. This lower voltage will create higher average amperages to meet the same power requirements. A higher amperage can increase the failure rate of small components. To keep the design reliable and cheap, the bus voltage was increased by changing the battery configuration.

Below is a schematic for the power board with sections previously mentioned marked with bounding boxes. Blue represents the power input and cleaning section, red represents the charging section, and green represents the power distribution section. Notice the red and blue bounding boxes both hold the LT3021 IC. This is because the LT3021 serves two purposes; cleaning the input power to some constant number and charging the batteries.

Power Input and Cleaning

The input power section is very repetitive. It uses the same circuit block 8 times, once for each solar panel input. Each block contains a current sensing IC and a diode to prevent energy flowing back to the solar panels. Power can flow back into panels when they are in shade, leading to loss. These current sensing ICs are part of the original design of the Inter Orbital board. They interface with a larger chip that was removed from the board. This chip was removed because software drivers could not be found to support it. The team decided that while it would have been beneficial for engineering data on the performance of the solar panels, it

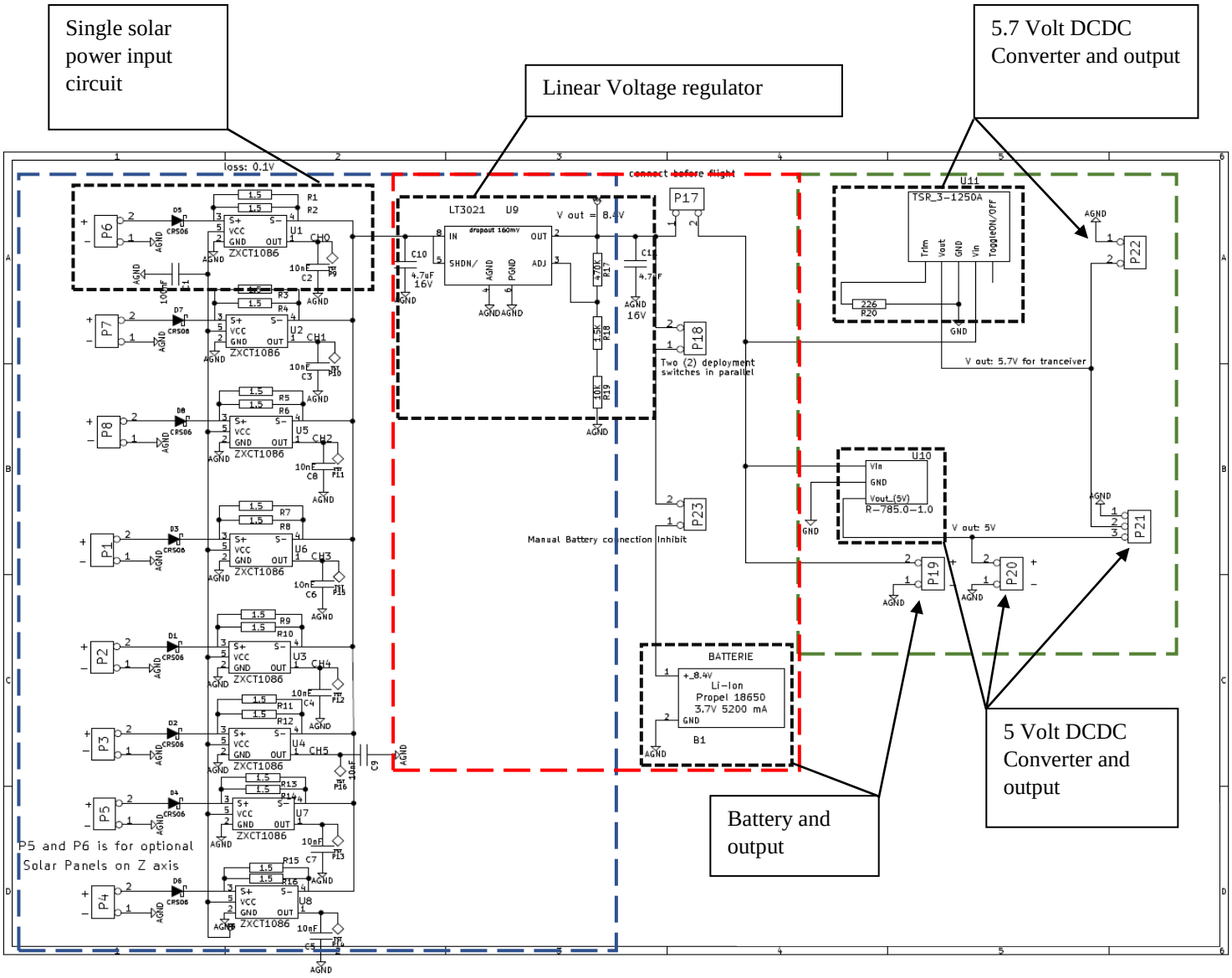


Figure 16 – Schematic view of the CACTSU-I power board. Regions of the board are indicated, and circuit functions are identified.

would not help the team or CubeSat make decisions during operation. There was no form of control over the solar panel inputs or the power distribution outputs.

The LT3021 IC is a voltage regulator and will now be referred to as the voltage regulator. The regulator is configured to regulate down to just under 8.4 volts, the final tuning was about 8.35 Volts but will be referred to as 8.4 volts. The reason this voltage regulator was configured to this voltage was to meet the max voltage of the Li-ion batteries used in CATUS-1. The solar panel voltage is nominally 13 volts, this ensures that the input voltage will always be regulated down to the max battery voltage. If the input voltage was lower than the regulator target voltage, the regulator would simply output that input voltage. This is the case with all linear voltage regulators, they only go from high voltages to lower voltages. Solar panels were designed with a higher peak voltage to combat degradation over time and imperfect pointing towards the sun.

Charging

The charging section is simply a connection to the batteries as the voltage regulator has already cleaned the input voltage to a stable 8.4 volts. The battery configuration for CACTUS-I is 2s2p. Two batteries in series, two sets in parallel. This configuration doubled the maximum and minimum voltage of the batteries and also doubled the potential current output. The battery voltage can change dramatically, especially in eclipse, because the configuration uses two batteries in series. The battery minimum voltage is 6 volts. This gives a total range of 2.4 volts. As the battery cycles between 25% and 75% DoD the voltage supply can change by upwards of a volt. This should not affect any components as the DCDC converters can accept this lower voltage and the voltage regulator will always regulate to 8.4 volts as it tries to charge the battery. Charging is done by holding a higher voltage potential to the batteries via the LT3021 voltage regulator so that charge always flow into the batteries. This flow will diminish as the difference between the current battery voltage and the max battery voltage decreases.

Power Distribution

The power distribution section was one of the section completely changed from the original design. While the original design did have a voltage boost circuit used to deliver the 5.7 volts needed for the communications board, during testing it was found to be unreliable. The IC used in the boost circuit would often overheat and burn out. This led to the removal of the boost circuit block and the addition of a simple DCDC converter. A DCDC converter was purchased instead of reworking the boost circuit to avoid more risk. The team was not comfortable with redesigning the boost circuit due to lack of experience and knowledge on the subject. The TSR 3-1250A DCDC Converter replaced the voltage boost circuit to supply the communication board. This converter was adjustable, so a trim resistor was used to supply the correct voltage to the communications board. The second DCDC converter, the R-785.0-1.0 was used to supply the 5 volts and 1 amp max to the Raspberry Pi 0. Both converters had lockout voltages below the minimum battery voltage. A lockout voltage is the lowest voltage a chip, DCDC converter, or other circuit can function at. Below the lockout voltage, the device will turn off. Having very low

lockout voltages ensured that the DCDC converters would not suddenly turn off from the varying supply voltage.

Lessons Learned

Solar energy conversion inefficiencies will lead to more low power situations.

A linear regulator is used to convert the incoming solar energy to the proper bus voltage. Converting voltage will lead to some loss, though it can be small. In the case of a linear regulator the incoming voltage must be higher than the regulated voltage. The greater the difference between the incoming and regulated voltage the greater the inefficiency. The Solar panel voltage is estimated as 12.5 volts and the regulated voltage is 8.4 volts. To estimate the efficiency of the regulator a simple ratio can be used:

$$eff = \frac{V_{out}}{V_{in}} = \frac{8.4}{12.5} = 67.2\%$$

An efficiency rating of 67.2 percent is poor compared to other converters with typical ratings between 85 and 95 percent. There are two ways to improve this efficiency, each with tradeoffs:

1. Remove one solar chip from a string to lower the overall voltage output of a solar panel by 2.5 Volts. Using the same equation above, this will result in an estimated efficiency of 84 percent, comparable to other DCDC converters. The benefits of this method are that it is low cost and the satellite will experience good efficiencies at beginning of life. The added risks with this method are a shorter satellite life time, and harder punishments from off pointing. The regulator will convert energy in a more efficient manner and this fix will not change any parts or increase costs. However, off pointing will cause the panel voltage to drop below the regulated voltage faster, making pointing errors more punishing. Panel degradation over time can reduce panel yield even further, worsening off pointing punishments. Recall that once the input voltage falls below the regulated the regulator will not work; it will simply pass the input voltage into the circuit.

2. Use a DCDC Converter in place of the voltage regulator. The added benefits are that voltages will be converted more efficiently and low voltages from off pointing can still be up converted, making for less loss. The downsides to this method is DCDC converters can be expensive and hard to find for the output voltage required. Voltages can be converted to the target voltage with efficiencies of 85 to 95 percent. Lower voltages can be up converted to reduce loss in a low yield situation, which is something a regulator cannot do. However, a voltage regulator with an output voltage target of 8.4 volts or 4.2 volts can be hard to find. This may be why the original design used a voltage regulator. Also, if a DCDC converter was found with the proper target voltage it could be very expensive.

Reduce risk of DCDC converter failure by adding input and output filters as well as protection diodes.

The DCDC converters used in the second rework of the power design worked during the many tests and Day in the Life tests ran. To ensure a long life add protection components to DCDC converters. These protections components will often be called out in part data sheets. The R-785.0-1.0 DCDC Converter will be used as an example. Below are two circuits with the R-785.0-1.0 converter and a form of protection. Figure 17 shows an optional diode that is used to prevent feedback current when a device is powered down. Feedback current could come from the device due to inductors storing current. The Raspberry Pi 0 used on CACTSU-I has a power inductor used to smoothen voltage transitions between 0 and 5 volts. This power conductors can be a source of current feedback. Option one can be used if the powered circuit (Raspberry Pi 0) is low in impedance, otherwise, option two should be used. To reduce electromagnetic noise a set of filters can be added to the input of the DCDC converter, shown in figure 18. While this is more important in lab applications with sensitive equipment, it of course can be argued that a CubeSat antenna operating near the noise floor is sensitive equipment. This is one way to reduce noise coming from the CubeSat itself.

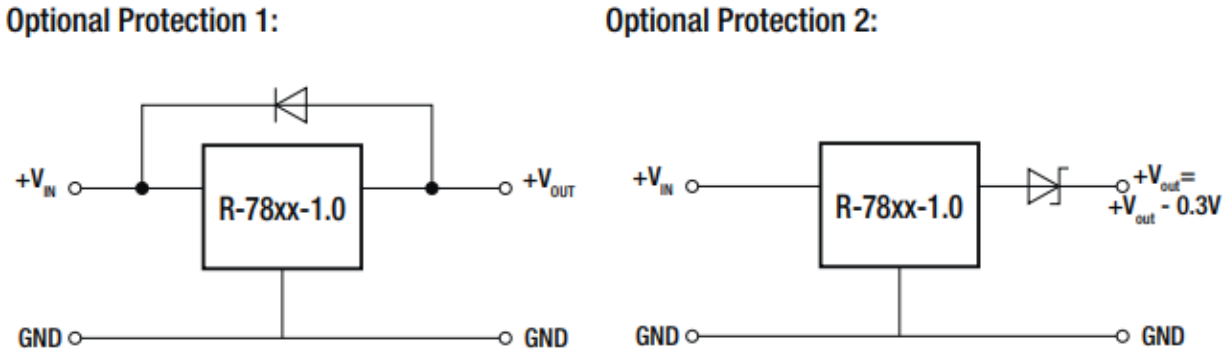


Figure 17 – Optional protection diodes used to prevent damage to the DCDC converter from feedback current. A feedback can be experiences if a device is powered down and has inductors storing energy. Option 1 is a configuration to be used in the powered circuit is low in impedance, otherwise, option 2 should be used. Note that a output voltage reduction will be experienced if using option two.

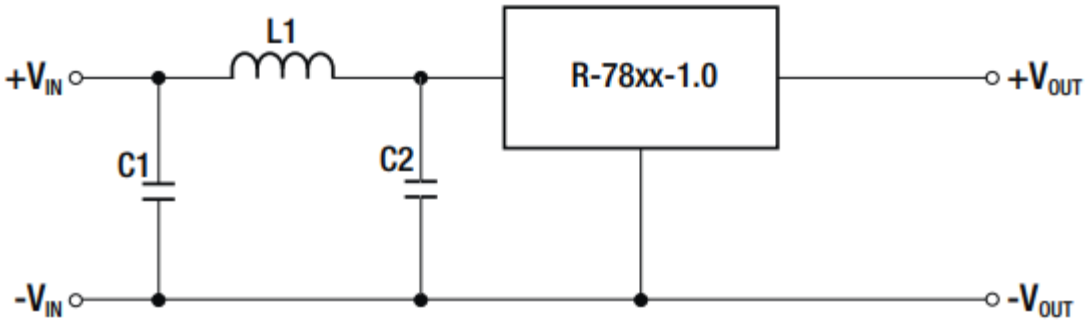


Figure 18 – Filters inserted at the input of the DCDC converter to reduce the electromagnetic noise. This may be an important method of noise reduction to keep communications signals clear.

Initial fixation on finding a heritage design led to delays in the power board design being ready, leading to a rushed product.

During design, teams were guided to find an existing power board and adapt it to fit the needs of the CACTUS-I mission. Many power designs that were found did not have complete documentation or were far too complex for what was needed. Three main power board designs were looked at intently before arriving at the design that was used and modified. The reasoning behind not designing a power board in house was to make for an easier time defending the design in review. A heritage design that has flown before makes a much better stance than an unflown in-house design. This was done to also reduce risk to the system but unfortunately the design chosen was heavily modified to the point that creating a new design in-house would have been easier, cleaner, and have an equivalent outcome. Another part of the issue comes from the student body. No student on the CACTUS-I mission and not many students at Capitol were prepared to design a power board from scratch. This was another major factor that led to the decision of modifying an existing design and was extremely justified.

With the knowledge learned from this mission, a design should be created from scratch or a stricter set of requirements should be made and used to search for an existing design so that very little modification is needed.

Future Guidance

Assumptions

The future guidance that will be discussed below will recommend designs and processes aimed at a CubeSat with a similar mission and payload to CACTUS-I. There will be some recommendation and designs that can apply to CubeSats of other missions; these generalized designs will be identified in each of their sections.

The future CubeSat is a Tabbed 3U++ CubeSat. It contains two payloads on board, one payload is a completely independent system residing in the last U of the Satellite, HERMES. The other payload is connected to the Satellite bus, TRAPSat. TRAPSat is depending on the bus to provide power, tasking, data storage, and data transmission. Both payloads depend on the BUS

for structural support, power generation through solar panels, and external thermal protection. The TRAPSat payload requires surface area of the CubeSat to operate, reducing the amount of space available for solar panels. The HERMES independent payload will require power generation and thus, the surface area making up its U is designated to be HERMES only.

The assumed budget is one that is similar if not equivalent to the CACTUS-I budget. It is also assumed that supporting tools and infrastructure are now present at Capitol Technology University (soldering irons and SRD equipment) and at the testing facility (tabbed vibration mount).

Advice

Do not assume heritage is better.

Just because a design has been used before and printed on paper does not make it better that one that can be created by the current team. Heritage requires documentation, something that is typically nonexistent or not complete. When working on heritage systems, students are often spending most of the time learning and troubleshooting because of bad documentation. Because the CubeSat space is very experimental, it is acceptable to have mostly new systems on board.

Do not be afraid to design something in house.

Designing a system or subsystem in house leads to better understanding for the students involved and gained knowledge and experience that the university can hold on to. Designing in-house also allows for easier trouble shooting and integration because students will be more familiar with the ‘under the hood’ functions of the system. Design files will also be available since it was created in the university, making modifications also very easy for future missions. If buying something from a vendor look for: good documentation, ease of understanding and good technical support services if applicable. The product purchased should solve or assist in solving a requirement or needed resource. If it does not meet a requirement it must be modifiable, many vendor products are not. This argument does not hold a candle when dealing with Comms and Data processing and handling. Theses subsystems are the two that are purchased most often and as long as it can be found cheap there is no reason not to purchase it. The University will probably not want to support the design of a processor or a communications system as it is too costly to research and develop.

If Capitol plans to continue space bound projects, this is a point to focus on. Even programs like RockSat-X end up re-making the wheel because there is no central location at Capitol where information can be easily stored and accessed by students.

Recommendations for Design

Ensure that the team is using and maintaining power and link budgets. One of the issues with the power system on CACTUS-I was the lack of power profiling. Because the power design took an incredibly long time to develop no attention was paid to the power budget of CACTUS-I.

This led to a modification of the Con-Ops, making tasking less frequent and sleep more frequent. Keeping track of the power profile will assist student engineers in constraining the system design's power usage.

Systems

Con ops

The general assumption that is used for most CubeSats is 'Build it first, then determine the operations.' In most cases, designing a CubeSat to meet a cadence rate or operational goal is not always possible. It's often better to simply have an idea of what needs to happen in orbit, then design the CubeSat to the best of the team's ability. Once the built system is tested and profiled, a cadence for science capture can be determined. In short, the concept of operations for this CubeSat will be 'Do science, sleep for X amount of time, repeat.' When dealing with communications, Cube Satellite acquisition will almost always be blind, interrupting the CubeSat of whatever it is doing to begin dumping data to the ground. This means the CubeSat will always need to be listening for any command to begin transmitting data.

General design constraints

On CACTUS-I the PC/104 mechanical specification was used to easily mount and organize multiple PCBs at once. What was not used was the Electrical Specification of PC/104. The electrical specification takes many forms, the ISA version is what will be used as it is simple and the number of electrical connections should be plenty for a mission like CACTUS-I. The electrical specification will define the location and number of pins that each PC/104 compliant board will use. It also defines the type of data buses (8 bit, 16 bit) that can be used and the pin locations for other types of information or power delivery. This standard is held so commercial off the shelf (COTS) parts that are PC/104 ISA compliant can be connected easily. In the case of a mission like CACTUS-I the data bus specification will be ignored because no COTS equipment will be purchased as it is far too expensive. Thus, the PC104 Mechanical Specification and the PC/104 ISA electrical connector specifications will be used.

Information on this standard can be found in the document "PC/104 Specification; Version 2.6" published by the PC/104 Embedded Consortium.

Systems Synthesis

System synthesis first starts with an understanding of the needed level of complexity and control. Many simple systems, like most CubeSats, have very little control. Understand the requirements of the science payload and determine the typical bus subsystems that would be needed. For each subsystem, define what type and what kind of behavior would be needed to then meet those requirements. For example, if a Satellite needs minimal pointing, something like Passive Magnetic Attitude Control may be perfect, like in the case of CACTUS-I. On the other hand, accurate pointing may need 3 axis control with reaction wheels and if in Low Earth Orbit,

magnetic torquer rods could be used in conjunction. With, hopefully, many types of subsystems to choose from, full systems can be built and evaluated for potential system performance.

Typical Subsystems within a space craft are:

1. Data Processing and Handling (CPU and storage)
2. Communications
3. Attitude control systems
4. Power generation, cleaning, and distribution
5. Mechanical
6. Science (the purpose of the satellite)

It is important to define the CPU and Communications first because there are fewer options and less flexibility with these systems. These systems are also heavily integrated in terms of data flow so it's important to find the best match for these subsystems. Added flexibility can come from creating something in house, but Capitol lacks the knowledge base, student labor, time, and money to design a CPU or communication board. Testing such a system would also be too risky to any mission. Finding a COTS solution that can be integrated onto a PC/104 board would be optimal. For example, a Raspberry Pi 0 or an Arduino would serve as a simple CPU that can be mounted to a PC/104 PCB via header pins and standoffs. Rad Hardening would need to be considered of course. Good matches for these systems then need to go through a sanity check. Many of these questions come from lessons learned from CACTUS-I, there may be other questions to ask and it's up to the team to stop and think critically about this.

1. Can these subsystems fit into a PC104 Form factor (ACS Excluded)?
2. Are these systems too power hungry?
3. Is there documentation/support available to work through the COTS subsystem's problems?
4. Is it outrageously expensive?
5. Are there any other quirks about the subsystems? Thermal issues? Instability? Very picky or strange power requirements?
    a. Active heating or cooling would be a no go.
    b. Instability related to General function or performance
    c. Common voltages are 3.3 and 5 volts. These are easy to supply via a custom power board because many components are made specifically to support 5 Volt boosting/bucking
6. With the chosen Comms and CPU, can the Science payload integrate and function well?

The Attitude Control System is one of the next items to consider in synthesis. Many ACS systems are complicated enough that a University like Capitol would want to buy some form of solution. Again, if buying something (if possible) it is best to try and integrate something COTS onto a PC/104 board made in house. ACS is also one of the subsystems that create interesting volume and use of space issues. Most times, ACS is not something that can fit in a PC/104 card stack. It needs to be properly mounted in specific locations to work. Working through how to

physically integrate the chosen ACS subsystem should be prioritized. If the ACS system cannot be placed in its optimal location, it will not perform as desired.

One of the last subsystems, power, can be crafted as a flexible, custom solution because it requires only basic PCB creation knowledge and circuit design. The circuit design within a simple power supply board is something that can be learned by looking through Texas Instruments documentation. Texas Instruments provide fantastic Integrated Circuit documentation like how the IC works, common circuits created using the IC, and the math behind it all. The reason sanity check question 5 is asked is because if the power supply needs to supply strange or uncommon voltage levels it will be much harder to find information and support when designing. However, there are many supporting resources online that can explain how to create a 5 Volt boost/buck circuit for a Raspberry Pi.

Solar is often considered part of the power subsystem as it fulfills the power generation portion. Small solar panels can be found for purchase and be sued to create large solar panel arrays. As found with the CACTUS-I mission, this wasted a lot of time due to the quantity and man hours needed. Finding large panels for sale would be ideal. Prioritizing panels of large size and lower efficiency would see a small, if any, change in performance compared to the SACTUS-1 panels. This will, however, save time that can be used to develop other items. In any case, the Solar and power design can often flex, therefore it is low on the totem pole.

The last subsystem is the Mechanical. The mechanical, assuming nothing dynamic will be happening is space is just a large box to hold things and mount solar panels to. The mechanics need to focus on meeting the launch environment requirements. Because the mechanical design for CACTUS-I worked so well and the tabbed platform is still very new, it is recommended that the CACTUS-I mechanical design be used for inspiration or a starting point, then modified to meet the new mission needs.

To summarize, from the list of acceptable subsystems that could work for the Science mission follow this general path:

1. Select Comms and CPU together, look for compatibility and support. Go through a Sanity check.
2. Select ACS, prioritize ACS when considering physical space and location. Go through a sanity check.
3. Select or profile a design for a power board. This will most likely be the subsystem that bends and fits around the other three, four is counting the science payload. Do a sanity check to make sure that
4. See how each decision fits into the mechanical subsystem.
5. Evaluate the outcomes of the system, the physical layout, subsystem elements, and feasibility.
6. Repeat the process, choosing some or all different subsystems. Think differently about solving the problem each time. This is an iterative process and should be repeated multiple times over the span of many days, not many hours.

During this process also take inspiration from other missions that have similar qualities.

Interfaces

The graphic below, figure 19, shows the four basic types of interfaces. These types each describe an element to a real interface. A wire, for example, will have physical, energy, and data interfaces that define it. A thruster fuel line will have a physical and mass interface associated with it.

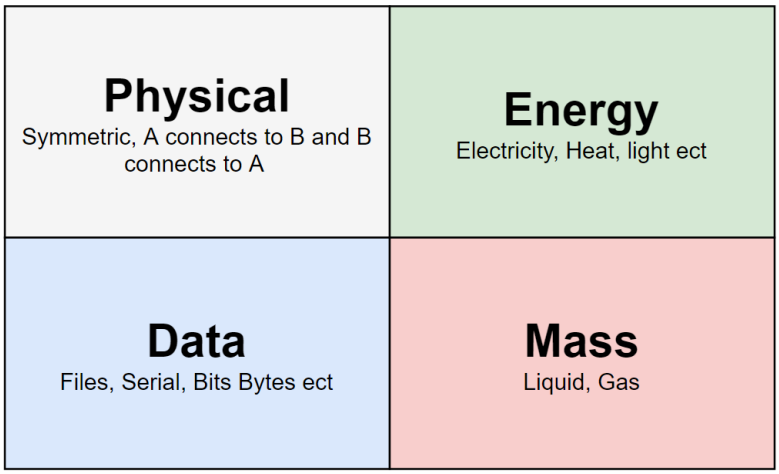


Figure 19 – The four elements that can make up an interface. These are the most granular types used to describe interfaces

Interfaces between subsystems should be clearly defined. This is the best location to improve a design and it is also the easiest place to screw it up (Akins 15th law of space craft design). The Design Structure Matrix (DSM), known as an N^2 diagram at Capitol, is a matrix used to examine the interfaces of a proposed system design. It lays out each subsystem in a diagonal fashion and identifies the inputs and outputs between the environment and each other. This helps engineers identify what subsystems may need in terms of added capability to simplify the interface. Sometimes this is small like adding an extra power regulator on a PCB that represents a subsystem. Other times it can be more complicated like adding a small microcontroller to a subsystem to free up the processor. Complicated interface simplification should be avoided as the solutions are often more complex that needed for a CubeSat. Each type of interface can be described in an N^2 diagram. A simple example of an N^2 diagram is shown to the right, figure 20.

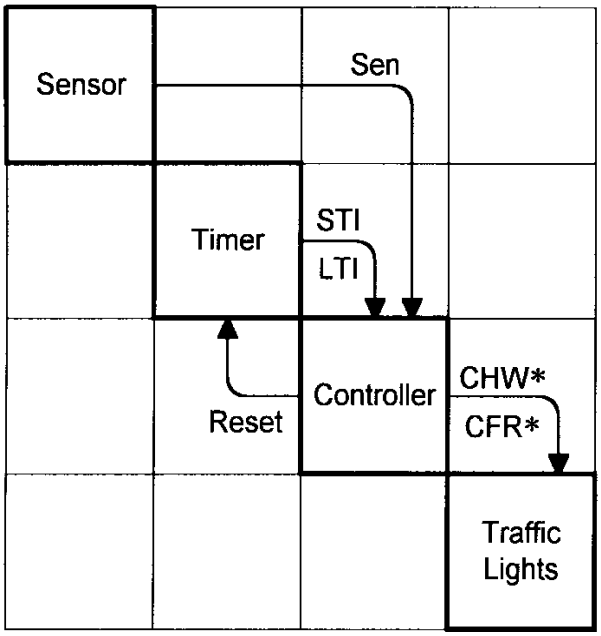


Figure 20 - Extremely simple N^2 diagram showing how inputs and output flow into other 'subsystems'

To dive deeper, material is pulled from a course presentation: “Fundamentals of systems Engineering; Session 8; Systems integration; Interface Management” by Prof. Oliver L, de Weck at Massachusetts Institute of Technology. Below, figure 21, depicts an example system that has many types of interfaces, notice that the interface colors match to one of the 4 granular types. Figure 22, further below, is a detailed DSM breaking down the interactions from figure 21 into a matrix. The numbers contained in many cells can represent specific specifications or documents although, in this case they are meaningless.

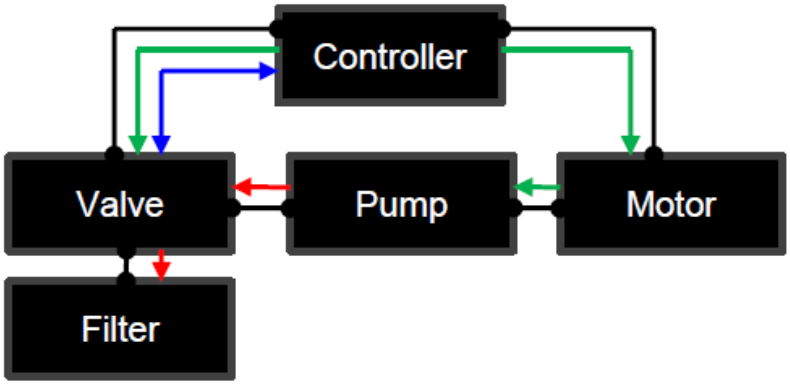


Figure 21 - Sample system that uses each type of interface type. Credit to Oliver L. de Weck

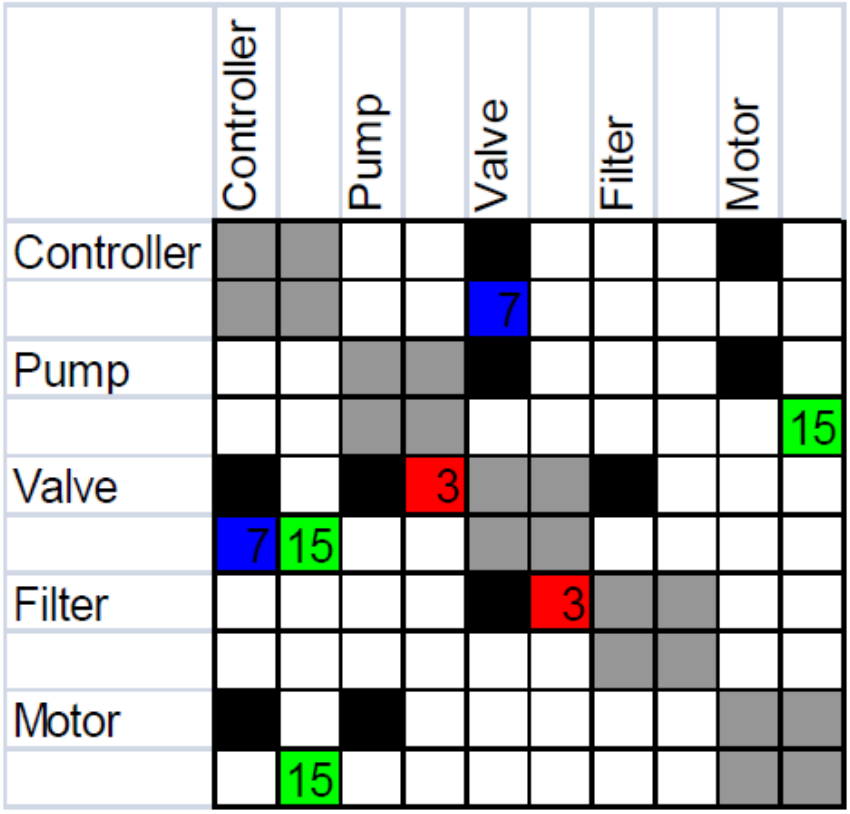


Figure 22 - a DSM of the example systems shown in figure 21. Notice that each type of interface has a designated location in the chart to be represented if there is one. Credit to: Oliver L. de Weck

The DSM presented above, figure 22, can be expanded to become a very in depth technical document. To reiterate on some messages previously stated: Following the exact process is not going to help build a CubeSat faster, cheaper, or better. CubeSats have a lot of unexplored technical challenges that are discovered during design and test. To sit down and properly document and work through each element of the design would defeat the purpose of a CubeSat at a university level. CubeSats are meant to have a looser path to success compared to other much more expensive projects. What is important is to understand the concepts and apply them as necessary during CubeSat development. In this case, managing a DSM document may not be the best course of action during the development because of how rapidly CubeSat designs can change. More time could be spent editing the DSM then time spent on design and build.

Another way to improve system design is not by decreasing the number of elements that need to be transferred between subsystems but instead improving the interface itself. The PC/104 ISA standard is a perfect example of this and is highly recommended for use on a mission like CACTUS-I.

The PC/104 specification defines a mechanical size and hole location. The ISA portion will define a location and type of electrical connection as well as a data bus. For our custom applications the data bus is ignored however, the electrical connection location and parts are useful. The ISA standard will allow for multiple PC/104 compliant PCBs to be stacked and all interconnected with 104 pins. Figure 3 and 4 from "PC/104 Specification; Version 2.6" will show the PC/104 Mechanical and ISA interface specification. For ease of reading, these diagrams have been included as figures 23 and 24. The parts used to make the ISA connections can be easily found from SAMTEC.

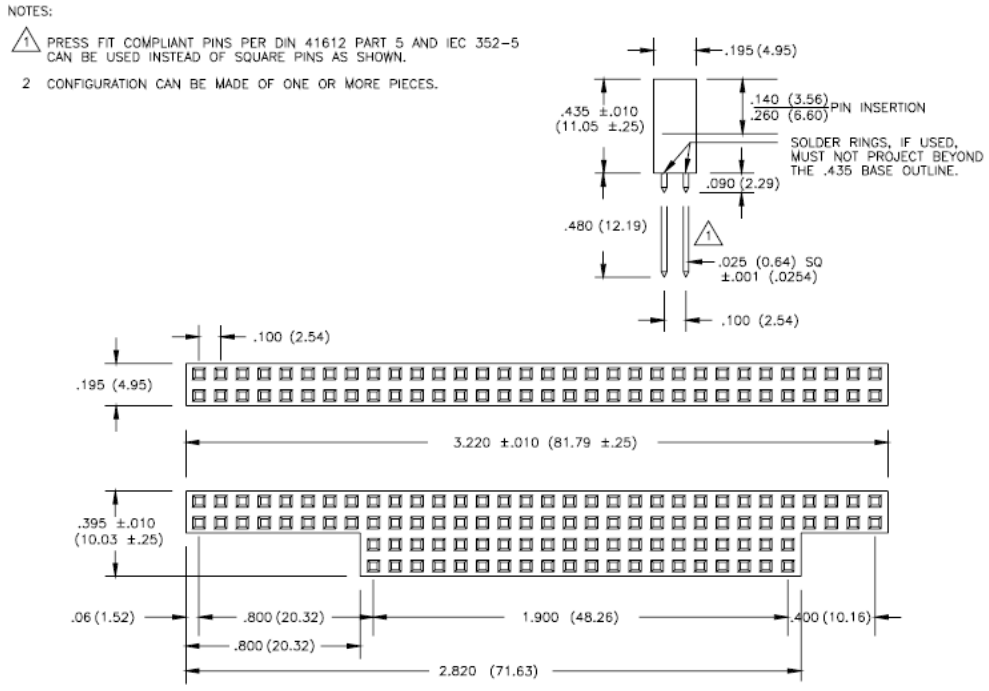


Figure 23 – ISA Interface definition, this include the size and number of pins. The connector height and pin length can be ignored because This will be implemented in a custom Bus for a space craft. The pin header height can be reduced to save room if needed.

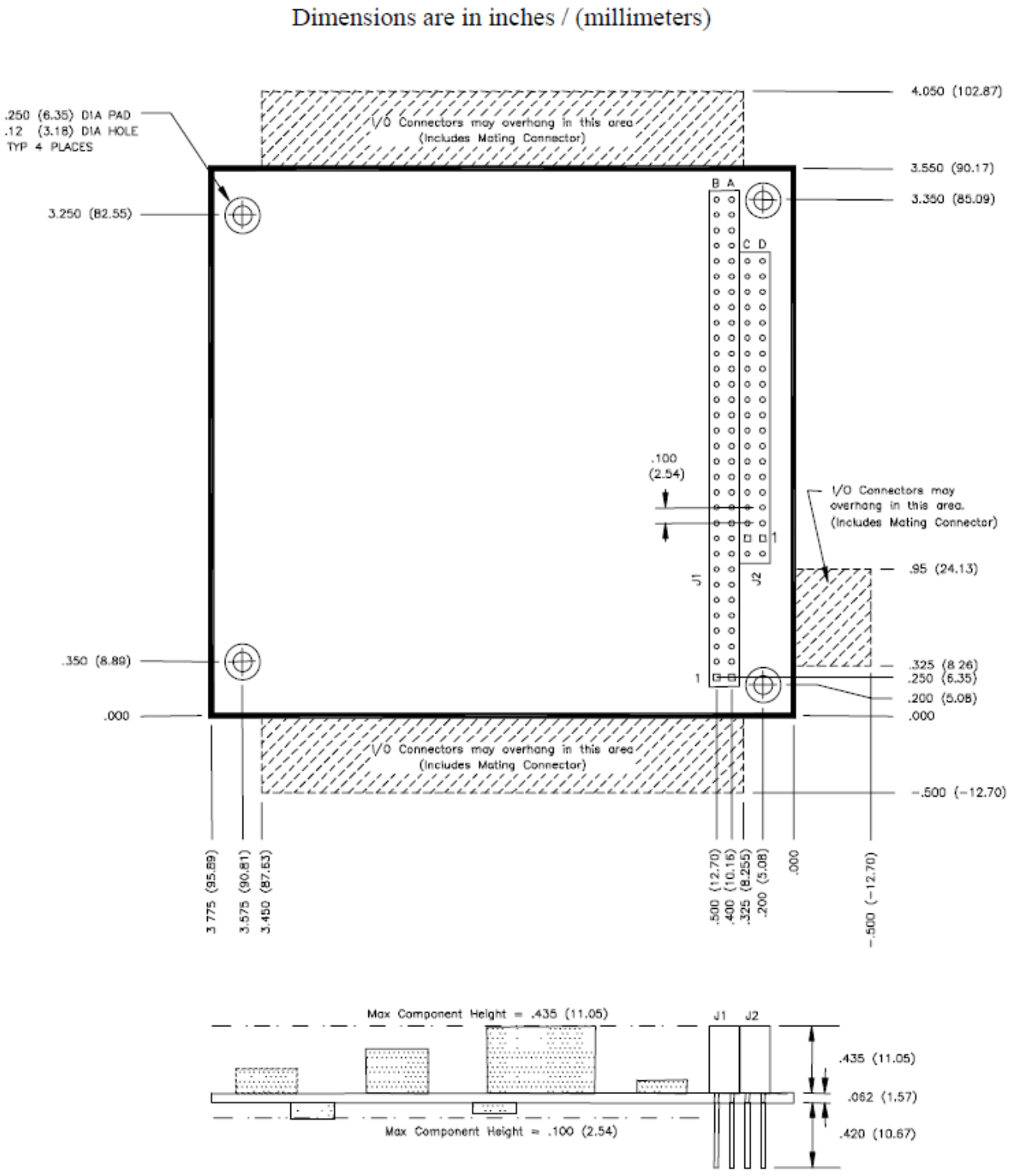


Figure 24 - Excerpt of Figure 3 from "PC/104 Specification; Version 2.6". depicts the size constraints of the compliant PCB and components. Also depicted are the connector locations for the ISA standard. Note that the additional area given outside of the PC/104 PCB bounds will probably not be able to be supported on a cubesat given the size contraints.

Power budgeting

A power budget is used to see the balance between incoming and outgoing power. It can be used to identify over active subsystems or provide a target performance metric for solar power generation. Multiple budgets for different situations, configurations, and events should be maintained at all times. Consider budgets for:

1. Nominal operations with minimal science with a constant solar input from the lowest producing side (consider only the area that could have cells on it). Include eclipse time of course
2. During antenna deployment if a nichrome burn is used because it can use a lot of power. Even if the draw seems low, profiling the system during deployment is important. Consider no solar input.
3. Operations during data transmission, this will be useful for seeing how long a pass could last. Consider no solar input.

As design continues the power budget should become more defined. A proper cadence for science activities can be established.

With an orbit time of 90 minutes, eclipse time of half an orbit, and based on suggested hardware, a sample power budget can be created:

Part	Add/Sub	Time on per 90 min orbit (decimal)	Current (mA)	Voltage (V)	Average Power over 90 min (W)
Raspberry pi	-1	1	120	5	-0.6
Comms Board A (Rx)	-1	1	75	6.2	-0.465
Payload 1	-1	0.01111	150	5	-0.0083325
Payload 2	-1	0.01111	150	5	-0.0083325
Solar Input	1	0.5	180	12	1.08
ACS	-1	0	0	0	0
Sensors	-1	0.5	1	5	-0.0025
				Total	-0.004165

The ‘Add/Sub’ column is used as an easy way to manipulate numbers in excel, it makes the value add or subtract from the total; Solar input is positive as it adds energy. This power budget assumes a timeline of a 90 minute orbit with 45 minutes in eclipse, hence the ‘Time on…’ column were a decimal value is sued to represent the fraction of time a component is drawing power. Payload 1 and Payload 2 were assumed to be active for 1 minute each orbit, during that minute they each draw 150 mA at 5 volts. This power usage is offset by its time on, shown in ‘Average Power over 90 min’. This power budget tells us that the space craft will lose about 4 mW of power every 90 minute orbit, a power negative situation. Easy ways to avoided power negative situations are to set the CubeSat into a sleep mode or lower power mode. Often the CubeSat receiver will stay on, listening for any commands that may come across. Some

operations may have the receiver turn off for small amounts of time to save even more power, but this is not recommended; anything can happen in orbit, it may not turn back on. Notice that will this power budget there is no input or column for efficiency. Power conversion and storage is not perfect, there are different levels of losses accolated with each method. DCDC converters range from 75% to 95% efficient, depending on the voltage difference between input and output as well as the current draw on the output (higher is usually more efficient). Linear regulators will only shift voltages down, done at a loss that increases as the difference in voltage increases. Power storage with batteries is assumed to be about 85% for modern technology, considering this is a CubeSat, 80% is a better number to assume until testing with hardware can be conducted. This power budget example is a high level, where hardware is not yet in house. An easy assumption to make is to assume that the general CubeSat efficiency is 80%.

This budget should be modified to include efficiencies for different components when hardware is house and tested. Power profiling of components/subsystems will be very important to accurately predict power consumption in orbit.

Mechanical

As mentioned in system synthesis, the mechanical structure needs to primarily survive the launch. This is assuming that no dynamic or kinetic operations are occurring while in orbit. Because CACTUS-I passed GEVS vibration testing, the same Sled and shell design should be used for CACTUS-II. Other options should be explored of course but given the past success of a design made in house, it could be considered a subsystems solution. An improved structure design will be presented and reviewed in this section. Many references to CADD files will be made, these files will be referred to with an underlined name correlating to the file name. All which will be included in the package delivered with this document.

End Mount Improvements

The end mount is a part used to close off Segment Shells and PC/104 Card Stacks. During the build process, the end mount had a hard time sliding into a shell due to a lack of tolerancing. What is recommended, and what has already been done in the design files, is to reduce the length and width of the end mount by .5 mm. While small, this reduction will provide enough room for a completed card stack to slide through a segment shell without too much resistance. Once a card stack is complete it should not have to be partially disassembled to be inserted into the segment shell.

Card Stack Improvements

As suggested in the Interfaces section, PC/104 ISA compliant PCBs should be used to build a card stack. The ISA interface is an excellent way to reduce time spent wiring as well as making the card stack integration a much cleaner process. Refer to figure 23 to see the ISA interface. The Electrical Section will cover implementation of the ISA interface on PCBs. This

section will assume a complete PCB model. Standard board spacing for PC/104 boards is .6 inches. Metal stand offs are not available at this Hight, the closest is .625 inches. There are three obvious solutions to the Card stack spacing design.

1. Use threaded rods like before, find nylon spacers at .6 inches or cut nylon spacers for the correct board spacing.
2. Use stand offs with 0.625 inch separation. Adding an extra .025 inches should only be a concern of total stack height. Pin contact will still be made between boards.
3. Use threaded rods and metal spacers with 0.625 inch separation. The same concerns from solution 2 exist here. This spacing is still not a concern because pin contact will still be made.

Below is a table for a single weighted trade study between the 3 collusions. This assumes the card stack height is below 4 inches or 100 mm. There are 5 boards total and an end mount is used on the top and bottom, for 6 sets of spacers total. Nuts are not considered because of hoe cheap they are. Cost is not considered because of how low cost each solution was. It was calculated to be 5 to 15 dollars for any of these solutions. Cost determined using parts from McMaster Carr. 4-40 threaded rods/screws, aluminum spacers and stand offs. Custom spacers were found using nylon spacers (large sizes can be purchased and cut down to reduce prices).

TABLE 1	Solution 1	Solution 2	Solution 3
Spacing efficiency	Custom Spacing, (10)	Preset sizes, about a 5% to 15% loss of space from longer lengths. (7)	Preset sizes, about a 5% to 15% loss of space from longer lengths. (7)
Time to build or implement	Custom spacing takes a longer time to size and cut properly. Risks are the Nuts needed to use on each end of the threaded rods. Rods must be cut to size (6)	Very easy assemble, add stand offs per boards (10)	Threaded rods can get in the way during board addition, risks are the Nuts needed to use on each end of the threaded rods, causing variability in length. Rods must be cut to size. (8)
Stability	Custom cutting leads to variability, can also cause cracking and failure. This method passed the GEVS Vibration testing although. (8)	All metal, all machine made. Very stable. (10)	Large rods extend the entire length of the card stack, ridged machine cut metal spacers are used. Very stable. (9)
Totals	24	**27**	24

From this short trade study, we see that solution 2, using stand offs, is the optimal choice. This is not documented in the trade study but, multiple spacer/standoff sizes can be purchased, giving the designer many options in board spacing. This board spacing is also determine by the

size of ISA interface compliant connector used on the board. Low profile connectors can be used to space boards around .5 inches.

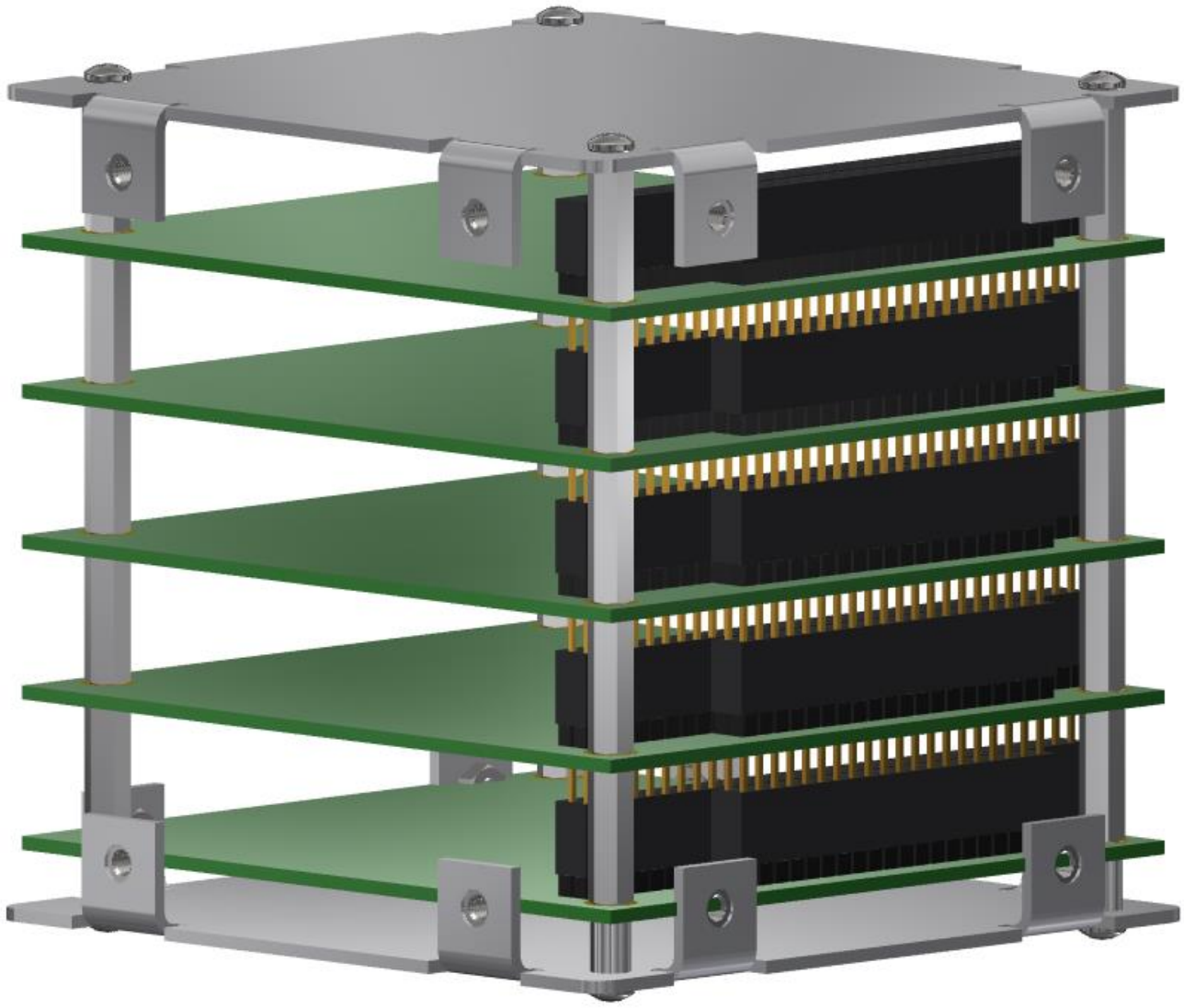


Figure 25 - A PC/104 Card Stack using the ISA Interface as well as threaded stand offs with Screws. The total Hight is about 101mm including the screw heads on either end. Using a 'low profile' ISA header and a shorter threaded standoff will a lot more space within a stack. Based on the PCBs from CACTUS-I and modifying the separation amount between each card, 5 boards could easily be included in a Stack less than 100 mm tall.

Another useful interface that could be added to a Card Stack is an externally accessible USB 2.0 connector. This can be located on one end of the card stack so that it mounts to the end mounts. Looking at the CACTUS-I model, this USB interface would reside somewhere below the antenna mount PCB. For implementation, this USB plug can be vertically mounted on the bottom PCB board. This could be an issue in terms of space if the comms board continues to be the bottom board. Other options are to mount a USB header to an end mount and solder wires from some other PCB to the USB header.

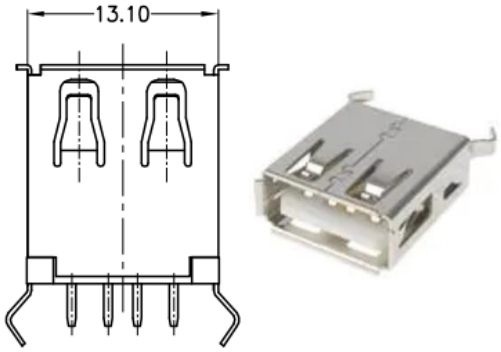


Figure 26 – Standard Size Vertical mounted USB 2.0. This is a 4-pin device with 2 chassis ground connections. A horizontal mounted version of this was used on CACTUS-I. NOT SHOWN: the height of this connector is 15 mm.

Part: 614004135023 from Wurth Electronics

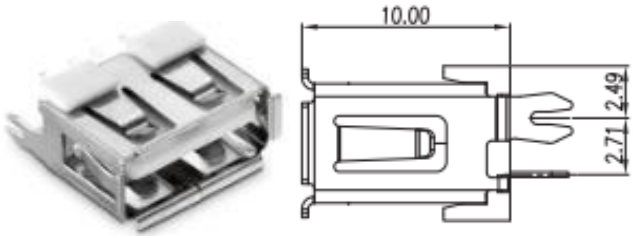


Figure 27 – This is a shortened vertical mount USB 2.0 connector. This is a 4-pin deice with 2 chassis grounds. If space is an issue, this connector could be used and is probably the better option in general for efficient use of space.

Part: 614004185023 from Wurth Electronics

The figure to the right is an implementation of a vertical USB on a PC/104 Card stack. The spacing between boards, .625 inches, is about 1/8 inch too long for the USB header to be flush with the end mount. Bringing the standoff length down to .5 inches would allow for the USB header to sit properly relative to the end mount and allow users to plug in USB devices when needed.

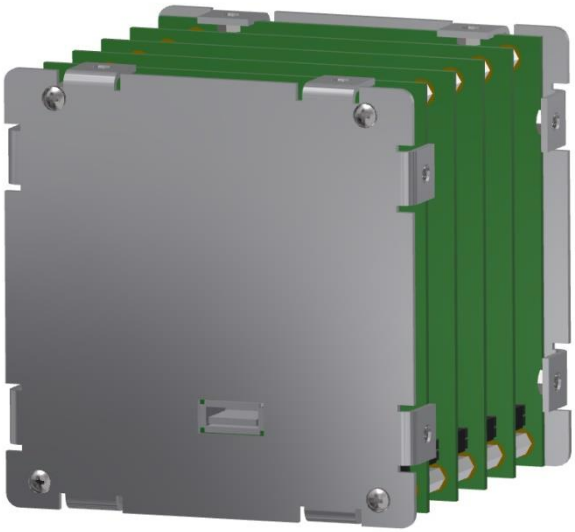


Figure 28 – A view of the top of a PC/104 card stack with a USB 2.0 port. This ideally would be located somewhere externally accessible. On CACTUS-1, if this was implemented the port location would be just below the antenna board.

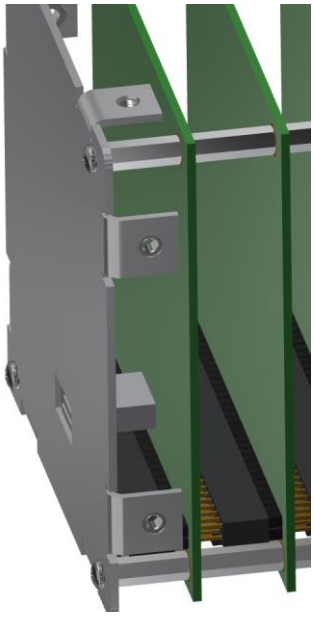


Figure 29 - A vertical mounted USB on a PC/104 Board. The vertical mounted USB chosen is modeled from figure 26. The USB gives a common, familiar interface with the CubeSat.

Tabbed Sled and Shell Improvements

The tabbed sled and Shell method worked very well on CACTUS-I and should continue to be used. The hole placement that mounts each shell should be standardized such that the holes all line up in the Z axis but vary in the X, see figure 30 for the Tabbed sled and coordinate system. This tabbed sled could be further standardized by setting locations for holes, but this is not recommended. The end mounts have been standardized and the shells can vary in length to fit various payloads. This gives the structure enough flexibility to adapt and enough rules to define a standard. On CACTUS-I, the slotted holes in the tabbed sled were used to run wires from solar panels into the rest of the CubeSat. This feature may also be needed on a future mission, to reduce the number of slots needed to run wires, larger solar panels than span the length of multiple shells could be made.

The materials to continue using are as described in the CACTUS-I mechanical Section. The Tabbed Sled made from Aluminum 7075 to keep a ridged platform. The Bent metal shells will be made from Aluminum 5052 because it is easier to bend than 7075 or 6061.

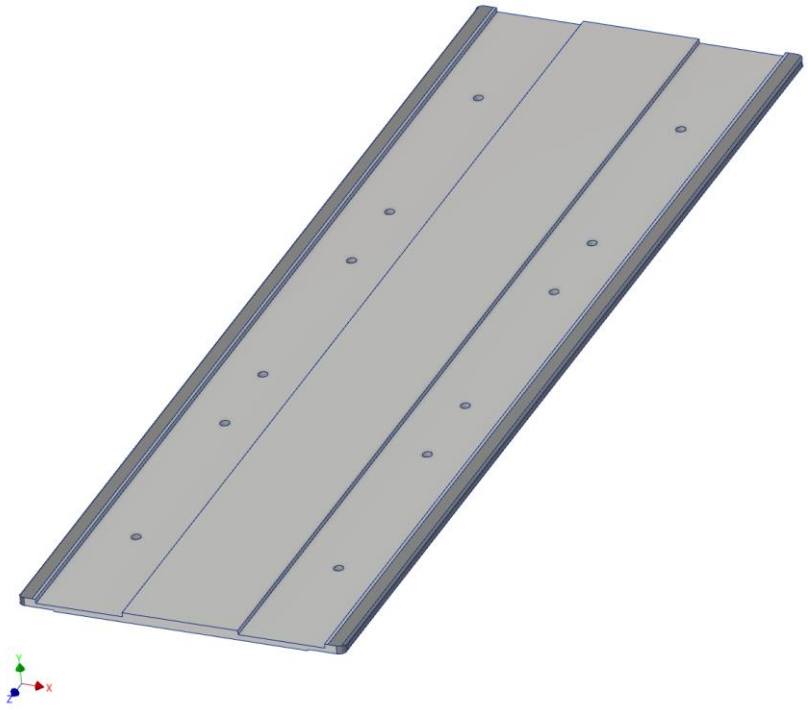


Figure 30 - The Tabbed Sled with aligned Holes

Interfaces and Connections between Segments

There are multiple types of connections that could be made as well as multiple methods of doing so. This section will cover three primary methods, each serving different combinations of segments (Card stack, unique payload or something in between)

1. Connection between two Card Stack segments, each PC/104 ISA compliant
    a. A specific and easy to implement solution

2. Connection between a PC/104 ISA complaint card stack and unique payload (think TRAPSat)
    a. This is a solution that could be easily implemented on something like CACTUS-I, a connection between the Bus and TRAPSat segments
3. Connection between any combination of payloads
    a. A very generalized interface that could be used on anything, this would use more space and sometime set more complicated than needed

Interface 1

When connecting two card stacks, a very simple interface could be made using the already existing ISA interface. This requires some prerequisites in the configuration between the two shells.

1. The position of the ISA pins must be the same between card stacks.
2. The end mounts are close to the edge of the shell, close enough that a spacer pin connector can be connected between the shells and connect them.

In many cases, there is no reason to make an interface like this. If the two card stacks must be in the same position for ISA mating, then the interfacing segments could be merged to form one large shell and one PC/104 stack. A separation where this interface would be acceptable is if a PC/104 stack is becoming so long that support is needed in the middle.

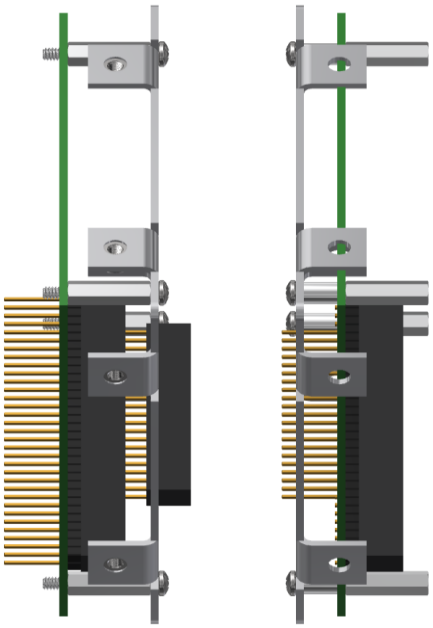


Figure 31 - Two ends of separate PC/104 stacks in different Shells. The interface connecting them is a 20x2 pin header, extending a set of 40 pins into the next card stack. depending on spacing, one of these header pins could be used of multiple.

The figure to the right is a model depicting both ends of the interface. The interface would use the same 20x2 header pin part to extend a set of pins to the next board. Only 40 pins are extended because cutting the end mount any thinner would be a risk to its mechanical strength.

The figure to the right is a wire frame view of the interface when the shells are mated together. The arrows show how far the male pins are extending into the female socket. The pins have extended far enough to make contact however, testing should be done with parts in hard to ensure connections. The pin extends about 4 millimeters into the socket.

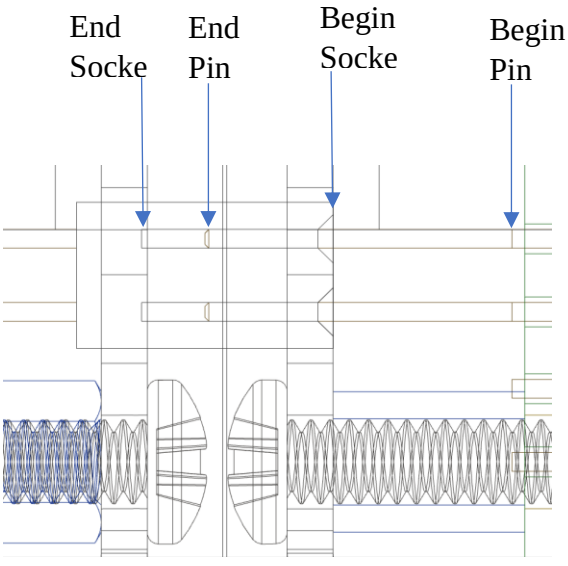


Figure 32 – A Wire frame display of the Interface type 1, extending the PC/104 ISA pins into the next shell.

Interface 2

A unique payload could contain complex objects like the TRAPSat Segment of CACTUS-I. If there is no PCB included anywhere in the unique payload segment, a D-Sub connector could be mounted to the end mount rather than Interface 1 described above.

Within the Card Stack Segment, this D-Sub connector could be through hole soldered to a PCB and mounted to an end mount, thus combining the end mount and PCB into one part. Or the D-Sub connector can use solder cups for wires and mount to an End mount. Either option works, which is chosen depends on the segment space and complexity.

These types of connectors would require extra space in both segments. This is easier to do in the unique payload because of the non-uniform consumption of space. The PC/104 payload would need to have a cut out on a board to make efficient use of space or take out an entire board to make room. This connection type is flexible because the mounting location can be anywhere on the end mount if both connectors line up.

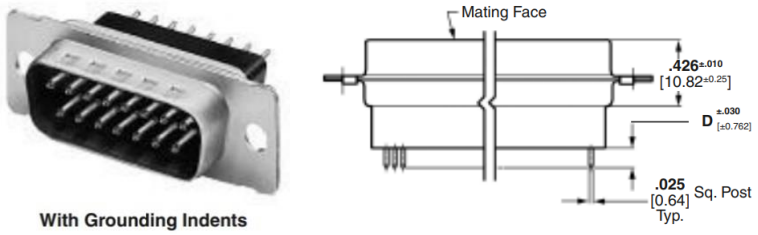


Figure 33 – a D-Sub 15 connector with a straight through hole connection. If a PC/104 PCB can be close enough to an end mount this component may be a space saving option.

Part: 5745072-2 from TE Connectivity

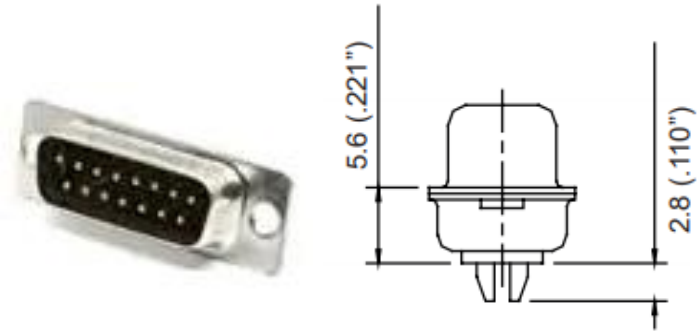


Figure 34 – A D-Sub 15 connector with solder cups for wires. This component would be used in a unique payload if it had no PCB to connect to. It can be mounted to and end mount with wires connecting to payload components.

Part: L77DA15P from Amphenol Commercial Products

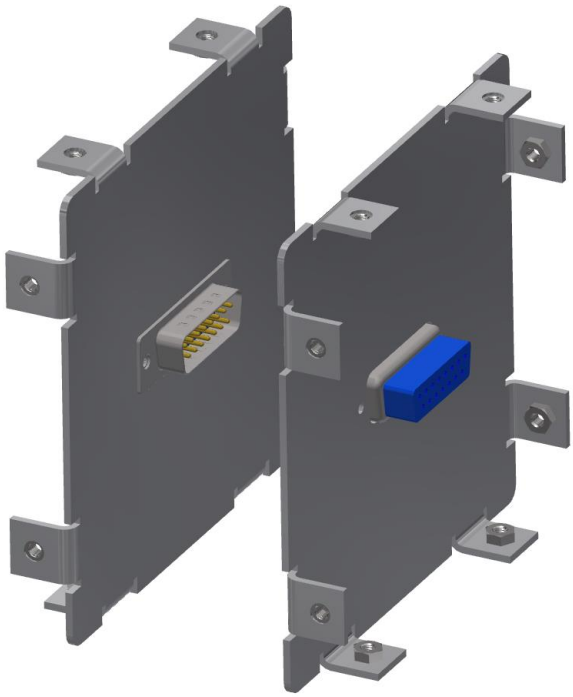


Figure 35 - CADD models of the D-Sub connector interface. In this model, the connector is mounting to the End mount and uses wires to connect to pins. It is possible to mount the connector to the end mount and solder through hole pins to a PCB.

In the figure to the right, the Two shells with D-Dub interfaces were brought together to see the mating of the connectors. The total distance between one End mount to the other is 8mm. This means that at least one of the end mount will need to be receded 8 mm into its shell. In this case, both end mounts are recessed 4 mm each. In application, the connection will not be this perfect, 9 mm or 10 mm may be needed to give the connector space. This 8 mm of room may be the perfect amount to fit hysteresis rods and a pointing magnet for a slim PMAC system. At least two of the PMAC axis would fit within this 8 to 10 mm space.

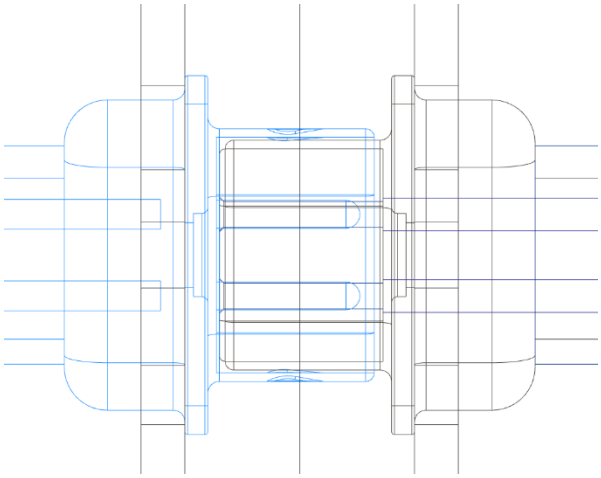


Figure 36 - a wireframe close up view of the mating D-Sub connector. The male connector is highlighted blue. Arrows will be used to point out the beginning and end of the connectors and sockets.

Solar

Larger Solar Cells

A larger solar cell should be used for the next CubeSat. A Larger solar panel at the same efficiency will cost much more money so it would be acceptable to find cells with a lower efficiency. Ideally, these two parameters will balance each other out when looking at output power, low efficiency with more area can produce the same power as high efficiency with low area. The reason area is being compared is because the small solar cells used on the CACTUS-I payload led to a very low packing efficiency. Using larger cells will cover more area for a high packing efficiency. If these two parameters balance out, the main benefit from larger cells will be a reduction in time spent build the solar panels. Building solar panels was one of the most time-consuming parts of the CACTUS-I build.

Many solar products that are readily available and easy to find are located on Mouser or Digi-key however; these products may not be suitable for space. Below are solar panel chips from the company IXYS. These products were found on Digi-key and all of these parts were used in the table above, match product numbers to see the performance. These solar solutions are small cells placed onto a thin PCB covered with a glass. The cells are about 22% efficient and the packing efficiency tends to be about 70% (IXYS calls this the Fill Factor).

For the sake of example on how to determine what is a better trade off, various products from Digi-key will be evaluated in terms of performance and cost. To reiterate, it's unknown how fragile these cells are.

Figure 37 - The smallest solar component offered by IXYS, this is a single cell device that generates .5 volts and 44.6 mA. Many of these would need to be connected in series to get a usable voltage level. Size: 22mm x 7mm

Part: KXOB22-12X1F from IXYS

Product	Product No.	Length (mm)	Width (mm)	P_{max} Voltage (V)	P_{max} Current (mA)	Power Output Per Cell/Chip/Unit (mW)	Wattage Per Area (mW/mm2)	Price	Break Price	Price Per mW
TrisolX Cells	N/A	26.3	8	2.33	14.6	34.02	0.1617	2	N/A	0.05879
IXYS Cell 22x7	KXOB22-12X1F	22	7	0.5	44.6	22.30	0.1448	1.435	100	0.06435
IXYS Cell 62x21	SLMD121H09L	62	21	4.5	44.6	200.70	0.1541	9.1	60	0.04534
IXYS Cell 43x14	SLMD121H04L	43	14	2	44.6	89.20	0.1482	4.72	80	0.05291
IXYS Cell 86x14	SLMD121H08L	86	14	4	44.6	178.40	0.1482	8.18	60	0.04585
IXYS Cell 89x55	SLMD481H08L	89	55	4	178	712.00	0.1455	28.36	10	0.03983
IXYS Cell 89x67	SLMD481H10L	89	67	5	178	890.00	0.1493	32.36	10	0.03636
IXYS Cell 90x79	SLMD481H12L	90	79	6.06	178	1078.68	0.1517	36.36	10	0.03371

Figure 38 - this is a 9-solar cell device from IXYS. This represents one of the largest components from IXYS with the edge solder pad connection method.

Part: SLMD121H09L from IXYS

Figure 39 – The largest product from IXYS. This unfortunately, will not be very useful for a CubeSat simply because it would be hard to mount and connect the panels efficiently.

The table above breaks down the price and performance of various solar panels. The TrisolX panels used on CACTUS-I were set at an estimated price since the data sheet did not list similar parameters. For repeatability, the Price Break used at Digi-Key has been listed as well. The Price Break is a discount when buying items in bulk. Digi-Key lists the minimum quantity to needed to receive the listed price break. The Packing efficiency (or Fill Factor) listed on data sheets was not very specific so a wattage per area metric was calculated to compare the different sizes and performances. This metric reveals which parts have the best use of space and as expected, the TrisolX cells are the most efficient (higher is better). This is expected because the efficiency rating of the cells is 28% while the IXYS cells are only 22%. The Price Per Wattage metric will determine what cells have the best value, lower is better. A product that has good scores in both metric will be desired but other factors will also affect the decision. Factors like the connection method (see figures 37, 38, and 39), time to build, quantity available, and ease of implementation should also be considered. Some of these factors can only be properly evaluated with parts in hand.

Based on the metrics presented and the factors mentioned, the SLMD121H09L was chosen to be the main comparison to the existing Solar Design. Reasoning is below:

1. The part is mid-range in terms of Wattage Per Area and Price per Wattage.

2. With a larger sized panel, the time to build should be faster than the very small TrisolX cells.
3. At the time of writing, there are plenty of parts available to purchase and support a CubeSat build.
4. The part uses the edge solder method (see figure 38 for the exact part). This method seems like it will be easier to work with. This is based on past experience, I have never used this part before.
5. The part is not incredibly large, making implementation easier as more can be fit onto a PCB.
6. The voltage output at max power is 4.5 volts, this is ideal for a low voltage bus where one 18650 cell is being used.

	TrisolX Cells	IXYS Cell 62x21
Number in Series	5	1
String in Parallel	3	3
Voltage (V)	11.65	4.5
Current (mA)	43.8	133.8
Power (mW)	510.27	602.1
Active Area (mm2)	130	1080
Total Active Area (mm2)	1950	3240
Packing Efficiency	26.92%	44.72%

The chosen part, SLMD121H09L, was used in a solar panel design. For comparison, the Bus PCB solar panel geometry from CACTUS-I was used. The figures below represent the original Bus PCB Solar panel with TrisolX cells and the Bus PCB Solar Panel with the new chosen part. The table to the right summarizes each panel's information for an easy comparison. The TrisolX Cells have an efficiency of 28% while the IXYS cells are 22% efficient. While the solar efficiency has gone down, the packing efficiency has almost doubled. Comparing 510 mW and 602 mW, the total solar output for this implementation should theoretically be 20% higher.

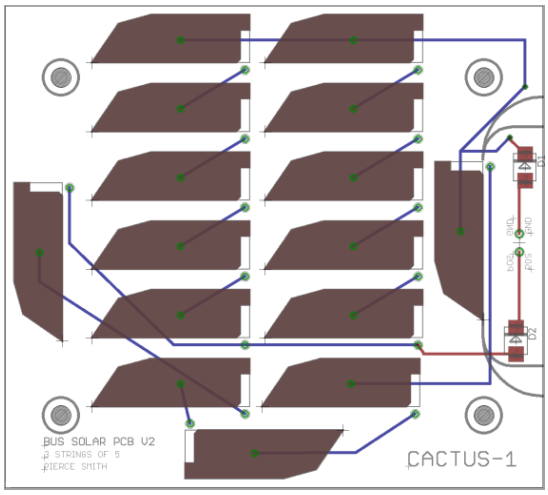


Figure 40 - The Bus PCB Solar Panel V2 that is mounted on CACTUS-I using the TrisolX solar chips. The power output of this panel is 510.27 mW.

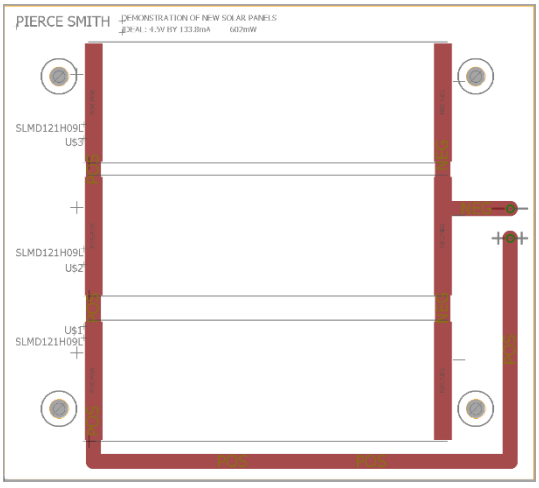


Figure 41 – The DEMO Bus Panel. A new PCB with the same dimensions and Hole locations as the Bus PCB Solar Panel V2 on CACTUS-I. This panel has a pwoer output of 602.1 mW.

Notice on this implementation of the DEMO Bus Panel the traces are very large, almost as large as the pads used to mount the SLMD121H09L panels. This was done because the DEMO PCB outputs a lower voltage and a higher amperage. A wider trace will reduce the chances of trace damage due to high current. These traces have been made extra wide because there is plenty of room on the board to do so. In terms of stability, these new cells have never been worked with in hand. Some form of epoxy may be needed at the edges to hold them in place. The TrisolX panels were mounted via solder across its entire footprint, a very secure mounting strategy.

Larger Solar PCBs

On CACTUS-I each solar panel mounted to its own shell. This made integration easy as some Segments already had solar panels installed. This also could theoretically make some Segments stand-alone like the Bus segment. The added benefit of some segments being stand-alone is not useful to Capitol because each satellite is a one-off, unique build. Because this feature is not needed, the solar panel size can be increased to span multiple shells. This would interconnect multiple shells to each other via the solar panel, making for two shell supporting connections; the solar panel and the Tabbed Sled.

To the Right are two images of the Bus PCB and Large PCB installed on CACTUS-I. These images have been aligned by the drill holes due to the limitations of the free version of EAGLE, the PCB software used. Boards must be below a certain area within the free version, so without paying it was impossible to work with a merged board. On a future project, if larger panels are desired, a 15 dollar monthly subscription or 100 yearly subscription to EAGLE Standard would be needed.

Aligning the M3 holes will assure that the board sizes are correct relative to each other. With the open space between the two boards and with some rearrangement, three more panels can easily fit. That brings the total from 55 to 58, a 5.5% increase in solar area. With further rearrangement of the cells on the Bus PCB another 5 could be added, totaling 60, a 9.25% increase. This may see a large benefit if moving to new cells presented in the previous section.

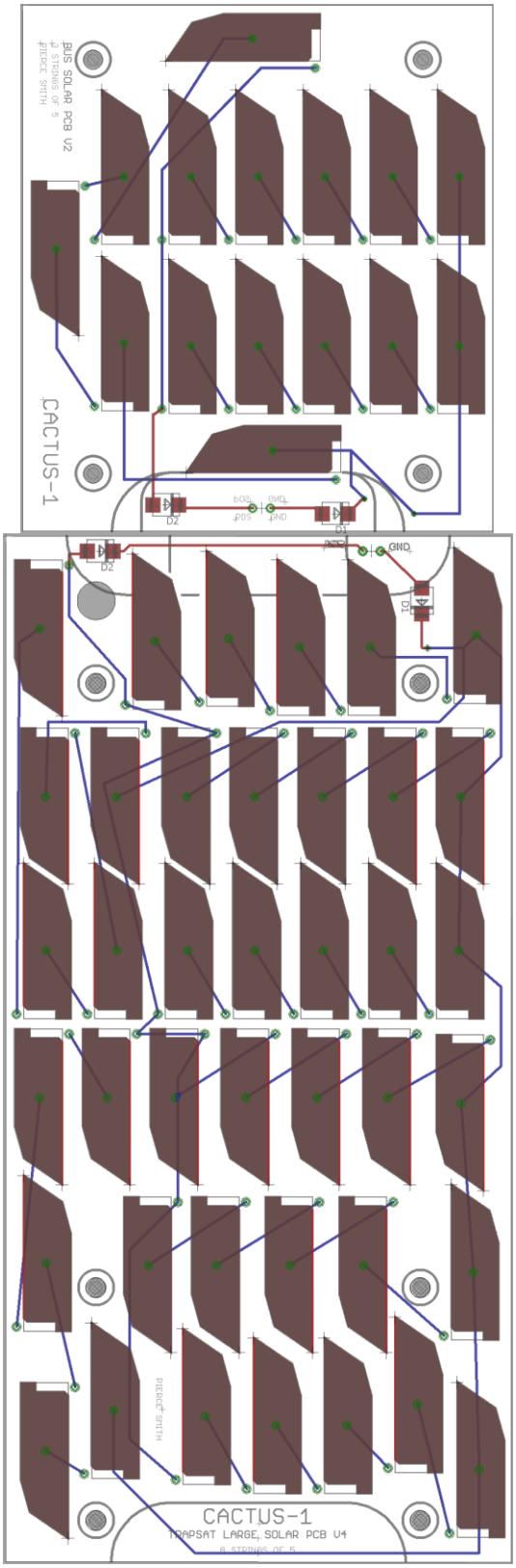


Figure 42 – The images to the right are the Bus PCB and the Large PCB from the CACTUS-I project aligned within this document. This was done due to the limitations of the PCB software EAGLE in its free version. Aligning these images shows how the boards would have been joined together. The free space between the board could be used to add more cells. With rearrangement, 5 new cells could be added, a 9.25% increase in performance.

The Fallback, using the Same Cells

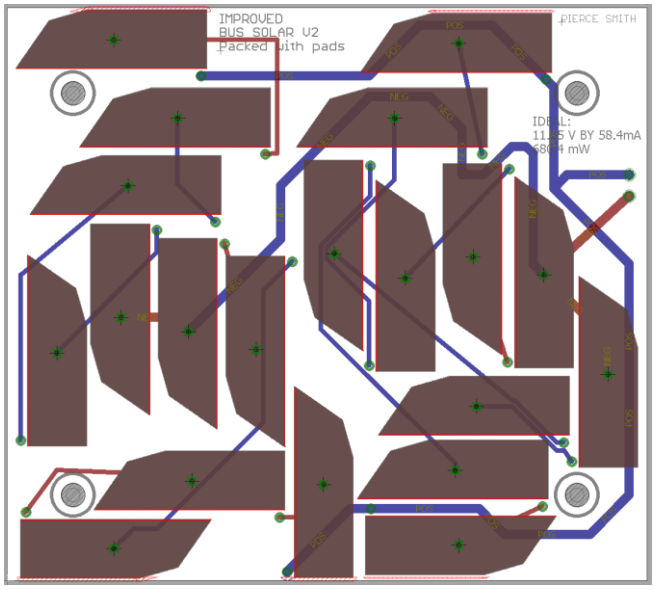


Figure 43 - An improved version of CACTUS-I's Bus PCB Solar Panel V2. This version also has had its pads fixed so that assembly will be easier. While it is very tight, an additional string has been added to the board, this increases yield by 33%. The traces that are carrying the most current from the parallel branches have been thickened to keep them healthy.

If no other viable solar products can be used and the older cells must be used, the packing efficiency must be improved enough to include new strings of cells. Firstly, the pads used to connect the solar cells need to be changed. As described in the solar section of the CACTUS-I documentation, the corner of the pad was removed to reduce the number of short circuits. This corner needs to be filled back in so that when panels are reflowed they fall into the correct positions. To further reduce the amount of work needed to make these panels, less solder paste should be used for each cell. Finally, the packing efficiency needs to be increased by placing solar panels closer together. How close each cell can be to each other will be determined from real world experience, it is best to give students solar panels and a board and have them build one. By building one, the students will see how close they can manage to get the solar cells and then plan accordingly in design. The picture above, figure 43, is an attempt at improving the packing efficiency. The panels are never closer than 1 mm to each other. The diodes were also removed from the solar panels because the power board already has diodes. The redundancy was sacrificed to fit the addition cells. If more work is put in, the traces and routing could also be improved.

Electrical

The power subsystem for CACTUS-I was always a struggle. This system should be designed and built in house because it is the easiest of the subsystems to create. The future power subsystem should use the PC/104 standard with ISA compliant interfaces. This will make for easy wiring within the Card stack. This design should clearly have 3 sections to it: Solar input and cleaning; Power storage, charging, and discharging; and Power distribution with conditioning. A full design will not be presented however, concepts of power storage efficiencies as well as power conversion efficiencies will be discussed here.

Special note

A full power board design will not be discussed in this section. This is because Erik Schroen will be doing a senior project on a power board design for a CubeSat using the PC/104 ISA standard in the spring of 2019. Erik has 3 years of experience designing power supplies with the Army. He is more than capable of designing a small power board for a CubeSat. Any design I

cover would simply not be as trustworthy or reliable as Erik Schroen's. I will, however, cover Power System Block Diagrams and controls that would be used within a CubeSat Power bus. Erik may take this as a suggestion on what type of systems he should design. Also given are the parameters for minimums and maximums.

PC/104 ISA

The ISA interface adds two pin headers to the PC/104 board. This pin headers have female pins on the top, spaced .1" from each other, and male pins sticking out of the bottom. This allows boards to be stacked on top of each other, see figure 44, to the right, for an example.

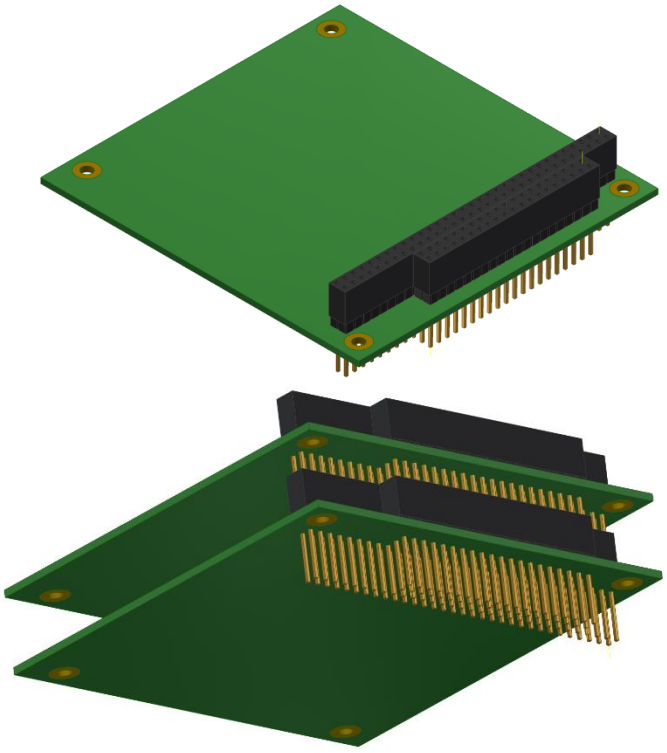


Figure 44- a PC/104 ISA complaint PCB stand-alone and mating with another board. The long pin headers are made to interconnect boards vertically, the standard spacing between boards if .6 inches. for custom needs, connectors that are low profile can be purchased to save vertical space.

The two pin headers needed are readily available from SAMTEC under the ESQ product line and they can be purchased through Mouser Electronics online. A 32x2 header and a 20x2 header will be needed, the products at SAMTEC are called ESQ-132-14-G-D and ESQ-120-14-G-D respectively. The 32 or the 20 in the name represents the number of pins across the header. The 14 correlates to the insertion force, the female header height, and the male pin length. The number 14 itself does not correlate to any measurement. The G indicates that the pins themselves have gold contacts. The D in the name indicates the header has dual rows, making for a 32x2 and a 20x2 header. A helpful resource to understand the naming break down is SAMTEC's Elevated Socket document, which is included with the package delivered with this document.

The standard height for the female header on top is .435 inches. This can be decreased by getting a header model without the breakaway spacers on the bottom. These can be removed manually. There are additional models from SAMTEC that do not include the spacers, these would be SSQ-132-23-G-D for a 32x2 pin header and SSQ-120-23-G-D for a 20x2 pin header. Another document called 'Through-Hole .025" SQ Post Socket' from SAMTEC will break down the naming behind the SSQ product line. If using the SSQ product line, be aware that the vias the header is soldered in to may need to be reduced in diameter. The Square male tails may be smaller size. A smaller, well fitting, via insures a good connection.

A EAGLE Board and schematic file that acts as a template for the PC/104 ISA standard has been attached, see figure 28 to the right for the board layout. Because all pins are interconnected between all boards on the stack, if one board applies 5 volts to J1 Pin1, all boards can connect to that pin to receive 5 volts. This also means that the total connections available between boards is 104 (2 x 32 + 2 x 20). If this is a limiting factor, J2 can be expanded to a larger header. This would break the ISA interface standard but if no COTS boards are included, the interface can be modified as needed. Also know that the ISA interface standard does not allow for more than 1 amp to flow through a single pin. While the ESQ and SSQ products can take more than 1 amp, it is recommended to allocate two pins for power supply, especially if it can go above 1 amp.

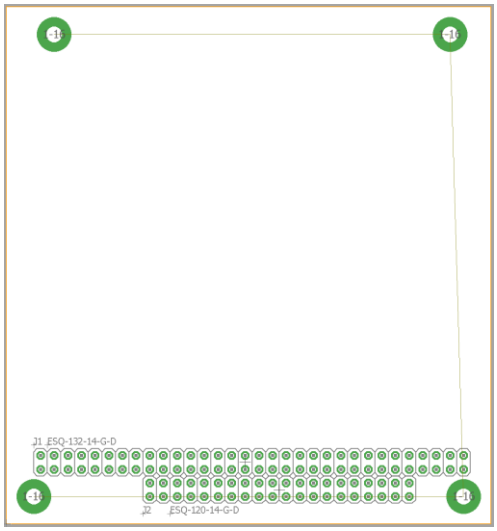


Figure 45 - A template PCB of the PC/104 ISA standard. This PCB can be copied along with its schematic to make new PC/.104 boards for some future CubeSat or other application.

A screen shot of an example pin allocation chart is included below, this chart can be used to identify the sources and users of all the pins. Additional information can be added as needed. The ISA Standard states that no pin can have more than 1 amp of current at any time. If there is a high amperage process that needs to occur, either use wire or split the current between pins. To split current between pins, small 1-ohm power resistors would be needed to equally load each pin out with a relatively equal amount of current. The file, Example Pin chart.xlsx, will be included with the package delivered with this document. In this example there is a PC 104 board within the TRAPSat payload so that easy connections can be made. A wiring chart will be needed to manage any connections with actual wires. This would cover the break out of connections between an imaginary TRAPSat PC/104 board and the TRAPSat Payloads.

Pin	Function Name	Source Board	User Boards	Description
1	5 Volt Supply	Power Board	CPU, Sensor	Supply 5 volts, 500 mA max
2	Ground	Power Board	CPU, Sensor	Ground connection
3	6.5 volt Supply	Power Board	Comms	Supply 6.5 volts to the comms board, 150mA max
4				
5	Solar input 1	Solar Panel 1	Power Board	Supply 600 mW at 4.5 volts
6	Solar input 2	Solar Panel 2	Power Board	Supply 600 mW at 4.5 volts
7	Solar input 3	Solar Panel 3	Power Board	Supply 600 mW at 4.5 volts
8	Solar input 4	Solar Panel 4	Power Board	Supply 600 mW at 4.5 volts
9	Solar input 5	Solar Panel 5	Power Board	Supply 600 mW at 4.5 volts
10	Solar input 6	Solar Panel 6	Power Board	Supply 600 mW at 4.5 volts
11	Solar input 7	Solar Panel 7	Power Board	Supply 600 mW at 4.5 volts
12	Solar input 8	Solar Panel 8	Power Board	Supply 600 mW at 4.5 volts
13				
14	I2C SDA	CPU	Sensor, Comms	I2C communicaiton between CPU, Sensor, and Comms
15	I2C SCL	CPU	Sensor, Comms	I2C communicaiton between CPU, Sensor, and Comms
16				
17				
18	5 volt Supply	Power Board	TRAPSat Cam0	Supply 5 volts to the TRAPSat Cammera
19	5 volt Supply	Power Board	TRAPSat LED Set0	Supply 5 volts to the TRAPSat LEDs
20	Serial Tx1	CPU	TRAPSat Cam0	Serial comms between CPU and TRAPSat Cam0
21	Serial Rx1	TRAPSat Cam0	CPU	Serial comms between CPU and TRAPSat Cam0
22	Ground	Power Board	TRAPSat Cam0	Supply ground to the TRAPSat Cammera
23				
24	5 volt Supply	Power Board	TRAPSat Cam1	Supply 5 volts to the TRAPSat Cammera
25	5 volt Supply	Power Board	TRAPSat LED Set1	Supply 5 volts to the TRAPSat LEDs

Figure 46 - An example pin chart using the ISA pin layout. Because all boards can see what is on any pins, there is listed a user and a source. The source is more applicable for power applications or serial connections. A second pin chart may be needed to manage any connections with wires involved. This will only cover the ISA interface.

Power Conversion Methods and Applications

There are 5 main power conversions that will be discussed in this section: Linear Regulators, Boost Converters, Buck Converters, DCDC COTS Converters, and Power Storage with batteries. Each serve a different purpose and have trade offs. Each can be very useful depending on the application and how dynamic the environment may be. Each will be reviewed for function and application in a CubeSat.

Linear Regulators

Linear regulators, in general, can only bring high voltages down to low voltages. This is done by shunting excess current to ground through another component, like a Zener diode. The efficiency of linear regulators will vary depending on the difference of voltage between the source and target voltage. The greater the difference, the more energy that is shunted to ground and the hotter they can get. Other features of linear regulators is that they do not use a switching frequency to raise of lower voltage, this means that the DC voltage coming out of the regulator should be fairly constant with little ripple. Some sensitive electronics may really care about a small ripple but for most electronics to be used by Capitol for a CubeSat, this ripple protection is not needed. These regulators can also react quickly to a change in the source voltage, meaning the output voltage is not interrupted by a changing input voltage. There are not many applications within a CubeSat bus where there is a relatively sudden change in the input voltage, so this feature would also not be useful. Many linear regulators can adjust the voltage output by changing a feedback voltage with a resistor divider bias.

The power dissipated, and thus power wasted, from a linear regulator is equal to:

$$P = (V_{in} - V_{out}) * I_{Load}$$

This means that the efficiency is linearly dependent on the difference between the input and output voltage. It is roughly equal to:

$$eff = \frac{V_{in} - V_{out}}{V_{in}} * 100$$

Linear Regulators, while not extremely power efficient, are very useful components when power efficiency isn't always necessary. These devices are extremely cheap, which is nice to hear when dealing with tight budgets however, CubeSats are one off, unique systems operating in a power-starved environment. A wasteful converter is not something needed on board. With that said, linear regulators provide a very low noise output, which is ideal for noise sensitive equipment. An application of this device would be for supplying voltage to a communication subsystems, where a stable DC reference may be needed. Using a DCDC converter to increase the voltage to appropriate levels and then using a Low-Drop-Out (LDO) linear regulator to remove the noise from the DC source would be an excellent way to provide low noise power to an amplifier.

Boost Converters

The boost converter is called a Switch Mode Power Supply and it is used to generate high voltage outputs from low voltage inputs. High frequency switching is used in combination with inductors, capacitors, and diodes to create a steady, high voltage (high relative to the input voltage). There are many boost circuits that can be used but a rather simple boost converter will be covered to understand the concepts. See the figure below for a simple Boost circuit.

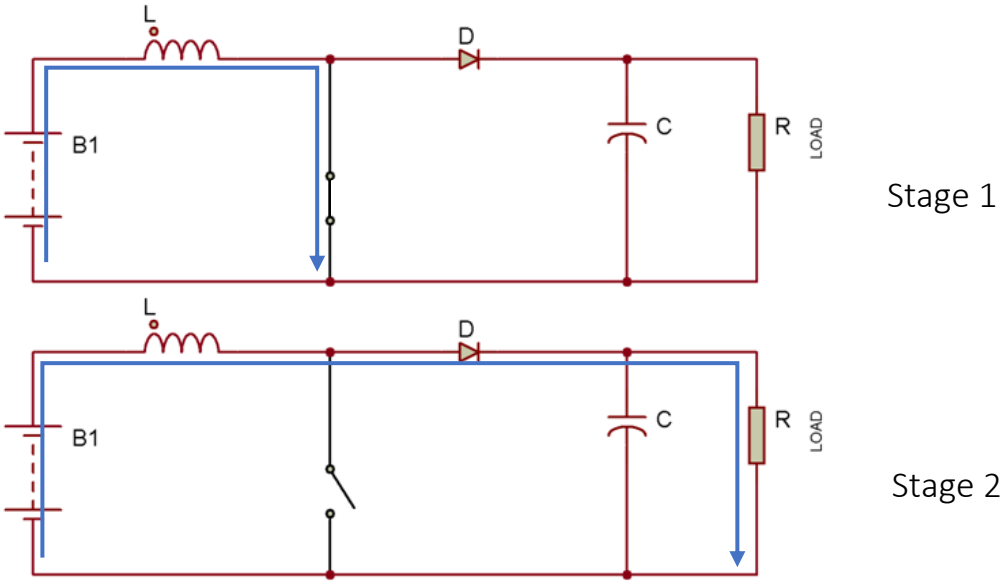


Figure 47 - The two stages of a simple boost circuit. Stage 1 is where current from the Voltage source, B1, is used to build up the magnetic field in the inductor, L. Stage 2 is where the voltage from the battery as well as the voltage from the collapsing magnetic field of the inductor is sent past the diode and into the capacitor as well as the load. When this circuit flips back to stage 1 again, the capacitor can discharge energy to keep the high voltage on the load. From the load's perspective, there is a small ripple in was is essentially high voltage DC power.

The Boost circuit has an active switch component, which would be the only switch seen in figure 47. This switch will turn on and off at very high frequencies. There are two stages to consider for the boost circuit above but, to consider this we must first make a couple of assumptions. One, the circuit is in Continuous Conduction Mode (CCM) and two, the circuit has already reached Steady State (SS). CCM means that the current within the conductor will never go to 0 and SS indicates that the circuit is already providing the expected power to the load.

In stage 1, the switch is closed, this ties the inductor, L, to ground and completes a circuit between the battery, B1, and the inductor. Current will flow from the battery to the inductor and then to ground which will then generate a magnetic field within the inductor. The reason current will never flow through the diode in this stage is because the node before the diode is at 0 volts because it is tied to ground. Remember that this is SS, so the part of the circuit to the right is already experiencing a high voltage. The capacitor, C, will be discharging energy to the load to maintain a high voltage. From the load's perspective, there is a slight ripple in the high voltage.

Stage 2 will occur shortly after, where the switch will be opened, and a new circuit will be formed. The new circuit will run from the battery to the inductor, to the diode, and then to the Capacitor and load in parallel. The inductor's magnetic field, generated in stage 1, will now begin to collapse, the only direction the current can go is towards the diode. The voltage from the battery and inductor will flow through the diode and charge up the capacitor and supply energy to the load.

This high frequency switching will allow low voltage to be stepped up to a high voltage, this can be a rather efficient and consistent process. The efficiency for these devices range from 60% to 95% and all depends on the amount of current being pulled from the device compared to its max current. The figure below, 48, is a table from a Texas instruments Boost converter. This converter can take various inputs from .9 to 5.5 volts and convert it to 5 volts. The efficiency of the device will change depending on the input voltage, current draw, and temperature. From the graph we see that at the extremes of current draw, the minimum and maximum, the efficiency starts to decrease. Keep the operating conditions in mind when looking for a voltage conversion solution. Also know that some devices can be sensitive to having the load shut down or be disconnected. The data sheet graph shown does not directly reflect the performance of the simple boost converter covered above. The point of this expert is to become familiar with boost converters and how the converters tend to behave.

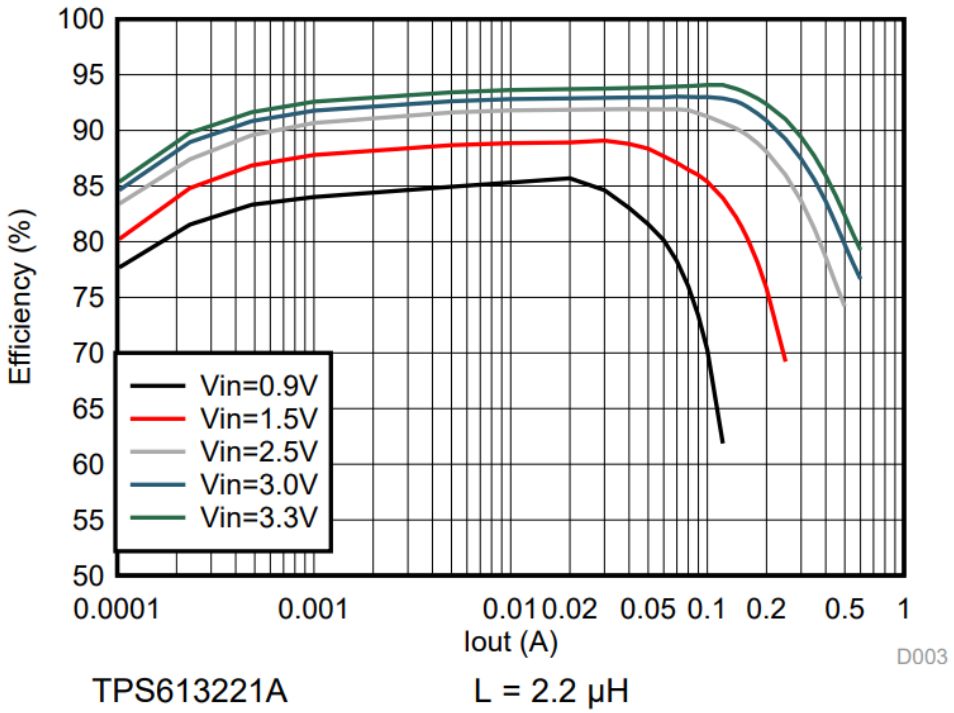


Figure 48 - Example plot of boost converter efficiency with respect to the current draw. We see that when converting voltages close to each other, the device is more efficient as we see that on either extreme, the device efficiency falls off. This performance does not reflect the performance of the simple boost converter covered above. The intent of this expert is for the reader to become familiar with general boost converter behaviors.

Boost converters are very useful to step up voltages and do so efficiently. A boost converter can be used to shift a 3.6 to 4.2 Volt dynamic bus up to 5 Volts for a Raspberry Pi 0 to operate on. The noise that the boost converter adds to the output signals may not be ideal for communications circuitry if a very steady DC reference is needed. A noisy DC reference could make for a noisy signal.

Buck Converter

A Buck converter is another Switch Mode Power Supply and is very similar to a Boost Converter except the components used are in a different configuration. This converter will generate low voltage outputs from high voltage inputs and do so very efficiently. The simple buck circuit that will be covered is the boost circuit previously reviewed but with the inductor, switch, and diode moved around. The figure below shows the two stages of the converter, all dictated by the switch next to the battery.

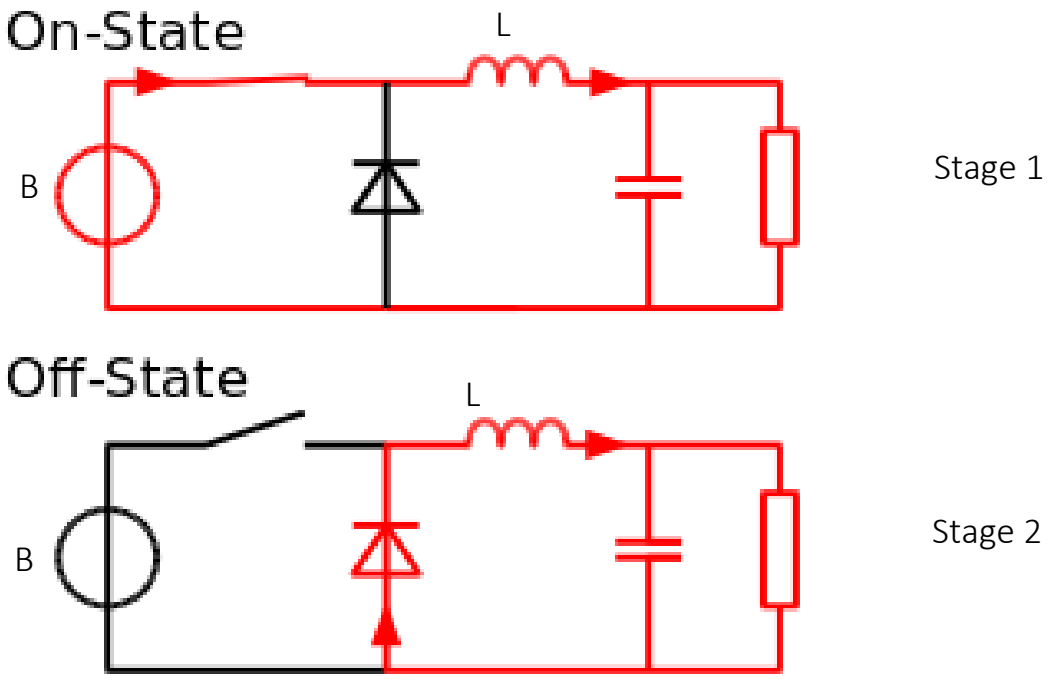


Figure 49 – the circuit for a simple buck converter. Shown are two stages. In stage 1 the inductor resists the flow of energy, reducing the experienced voltage at the load. In the second stage, the inductor will provide some power as well as the capacitor to the load.

The figure above shows the two circuits created by the active switch component in the converter. The only assumption to be made for this circuit is that the circuit has reached a SS. In the first stage, the circuit created runs from the battery, B, to the inductor, L, to the capacitor and load in parallel. During this phase, the inductor will resist the flow of current and start to generate a magnetic field. A lower voltage will be experienced at the load because the inductor is

taking some of the voltage from the source, a simple series circuit example. The capacitor will be discharging or charging, depending on the related voltages. The load will experience a lower voltage consistently because if the inductor is not supplying the voltage, the capacitor will and vis versa. The balance between these components supplying power to the load is determined by the duty cycle and it will determine the resulting voltage.

When moving into stage 2, the switch will open, and the inductor will function as a current source. In stage two, the inductor will begin to force current through the system as the magnetic field is collapsed. The inductor current can either charge the capacitor or serve the load or both, whichever is needed. At this point, two things could happen, either the inductor runs out of current and all that is left is the capacitor to provide power or the switch reconnects, turning the circuit back to stage 1, before the inductor runs out of power. If the inductor dose not run out of power, the circuit is in CCM. If the inductor does run out of power, the circuit is in Discontinuous Power Mode (DCM).

The efficiency of these devices can vary wildly, from 30% to 95%, which greatly depends on the current draw from the device. It is especially important with buck converters to consider the range of operating conditions the converter will see so that the right device is picked. Below is a buck converter with very different specifications from the boost converter shown previously. To provide background, this converter can provide an output 3.3 or 5 Volts at 300 mA and it can do so with an input voltage ranging from 4.5 to 42 Volts. Below is a figure from a Maxim Integrated Data sheet that shows the efficiency curves for this device. The device that this data was pulled from does not reflect the performance of the simple buck converter discussed above. Again, there are many circuits that exist that can perform voltage step down.

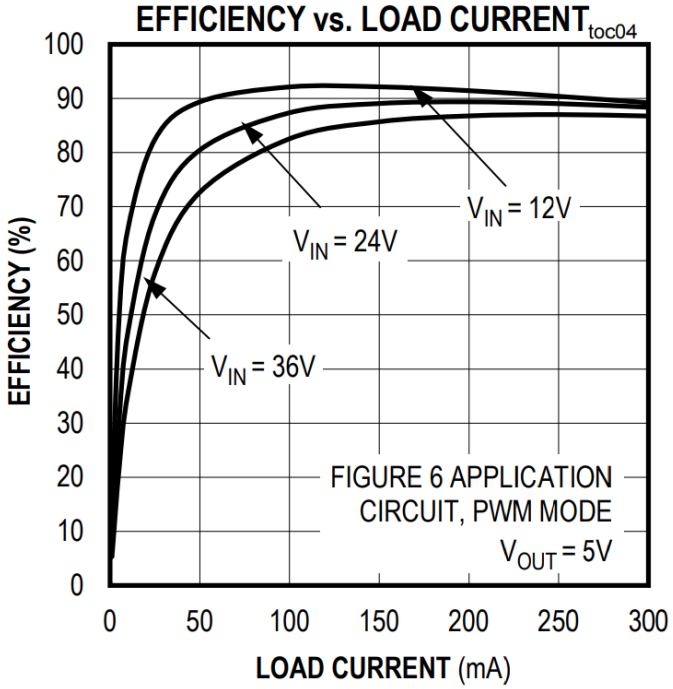


Figure 50 - Efficiency curves of a Maxim Integrated buck converter. The efficiency is mostly consistent except for very low current draws.

Many circuits now include intelligence and circuit protection. The point of the data sheet excerpt is for the reader to become familiar with buck converters and their behavior.

Buck converts are ideal for of course, stepping voltages down. If a 3.3 Volt device needed to be powered from a 3.6 to 4.2 Volt dynamic bus, a Buck converter could be implemented to do so with ease. This solution would be low noise and as long as nominal operating condition are met, it would be very efficient. Again, good operating conditions depends on the device and the voltages used. But aim to get the efficiency of these converters to stay in the 90% range.

DCDC COTS Converters

There are many types of DCDC converters and some have already been covered. Boost and buck circuits are considered a DCDC converter because they are circuits that raise of lower voltage levels. The circuits being considered in this section are COTS converters that use transformers to change voltages. There are two basic types, the Forward converter and the Push pull converter. The review on how these converters work will be short because they are readily available from manufacturers are generally plug and play. There will be a greater focus on protection circuits and the effects of using DCDC converters with Transformers in them.

In the forward converter, a MOSFET switch is used to connect and disconnect the source voltage from the transformer. This creates a square wave which is then boosted by the transformer. On the other side of the transformer, the diodes protect and direct the flow of current while the inductor and capacitor smoothen out the boosted square wave. This results in a higher or lower DC voltage with a ripple. The figure to the right, 51, will show the direction of energy during the active stage, which is when the switch is connected.

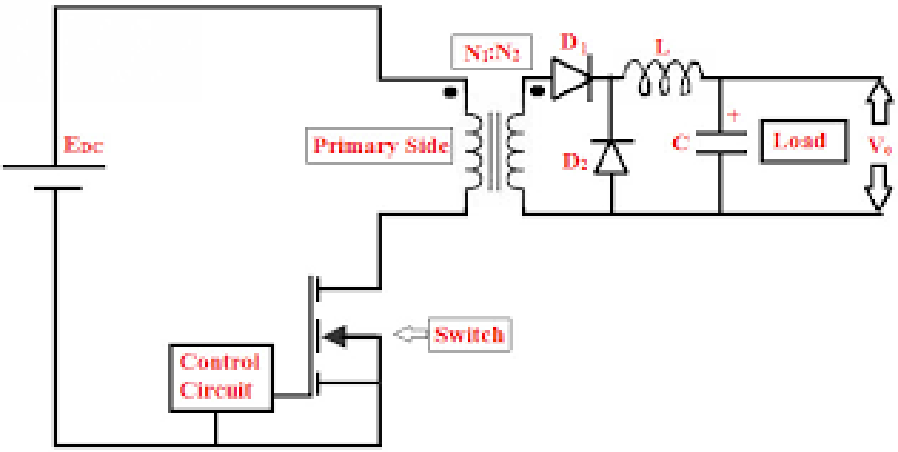


Figure 51 – A simple circuit containing the important component of a forward DCDC converter. These converters use one switch to connect and disconnect a source voltage. The duty cycle is usually 50%. These converters create square waves and then boost/buck them with a transformer, then rectify and smoothen. This process can add noise to the output power, more noise than a boost or buck converter and certainly more noise than a linear regulator.

A Push-Pull converter functions similarly to the forward converter but switches twice as much due to a center tapped transformer and two MOSFET switches. With a center tapped transformer, the duty cycle can be increased above 50%, making for less noise on the output after smoothening. The figure below, 52, shows a basic Push-Pull converter, the arrows that current will take when switch 1, Q1, is closed.

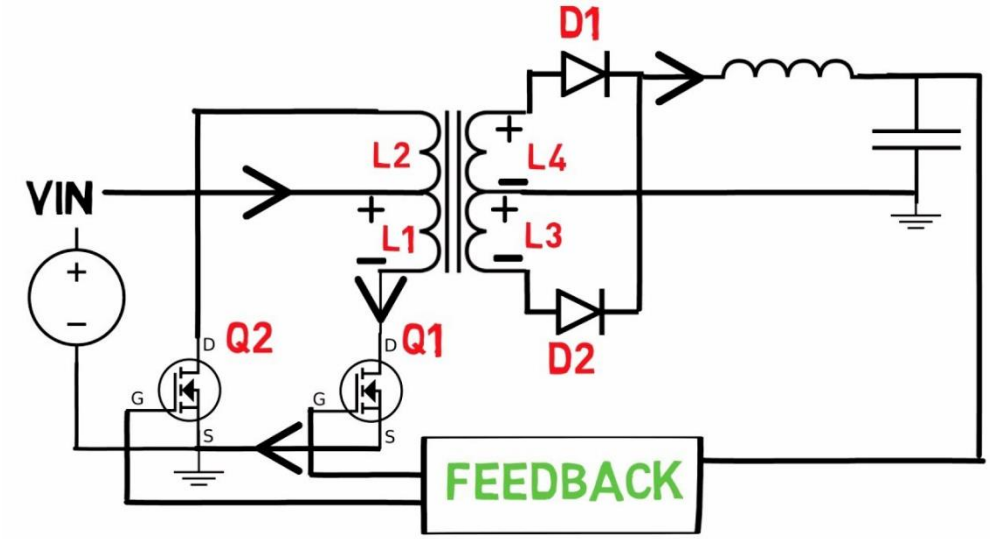


Figure 52 - A simple circuit of a Push-Pull DCDC converter with only necessary components present. This circuit center taps the transformer, allowing for higher duty cycles when using two switches. This makes for less noise on the output DC signal after the rectifying diodes and the smoothening filters.

Because transformers are used to increase or decrease voltages, there is added noise on the input lines of the DCDC converter due to transformer reflections. Many data sheets for DCDC converters will recommend adding a filter to the input of the DCDC converter to reduce the Electromagnetic Interference (EMI). See figure 17 from the CACTUS-I Power documentation to see EMI reduction. Data sheets from trusted large manufacturers will list not only an EMI reduction filter but also an output protection circuit. From experience this is typically a low drop diode connected in series with the output. See figure 18 from the CACTUS-I Power documentation for diode protection.

DCDC Converters are efficient (usually) devices that users can buy from vendors. They are fairly plug and play although, because of the transformer making noise and reflections, filters on the input of the DCDC converter will be needed to keep the circuitry clean. The transformer is not without benefits however; it provides isolation between the input and output. There is no physical connection between the source and load, so converter failure will not cause a critical failure for the load. DCDC converters can be useful on CubeSats where there is not enough space on a PCB to create a boost or buck circuit, building a boost of buck circuit is too tedious, or when the load does not care about a slightly noisy power source. A great place to use DCDC converters would be when paired with LDO linear Regulators. The DCDC will provide the large boost in voltage and the LDO will then remove the noise from the signal as well as reducing the voltage slightly. This type of combination would be very useful for a lower noise supply for a Communications system.

In Summary

Type	Use	Efficiency	Noise	Cost	Complexity
Linear Regulator	Lower voltage	Depends on voltage difference, usually not great	Low	Low	Low
Boost	Raise voltage	In nominal conditions, 80% to 95%	Medium	Low to Medium	Medium
Buck	Lower voltage	In nominal conditions, 85% to 95%	Medium	Low to Medium	Medium
DCDC (Forward)	Raise or lower voltage	In nominal conditions, 80% to 95%	High	Medium to high	Low
DCDC (Push-Pull)	Raise or lower voltage	In nominal conditions, 80% to 95%	Medium-high	Medium to high	Low

Good applications (assuming a voltage bus of 3.6 to 4.2 volts):

- Communications high voltage source – use a DCDC converter followed by an LDO Linear regulator for high, low noise, voltage.
- General 5V power source – use boost converters to make a very efficient voltage source for 5-volt devices.
- Solar input – depending on the voltages, a buck converter may be possible. Many times, the voltage needed for a Bus driven by battery voltage is hard to find. In which case a custom circuit could be created but, it will probably have low efficiency. Do the math and do the research to find if a linear regulator would work. Each case is different.

Bus Voltage

The bus voltage is the central voltage that the power distribution system will run from. Input voltages are converted to a bus voltage before being converted to an acceptable voltage for power distribution. Battery power is converted to the bus voltage before being converted again etc. Part selection and cost will be heavily affected by how the bus voltage is defined.

Unregulated bus voltages are just a power source. The components that draw power from an unregulated bus need to be very robust to handle varying voltages. For a CubeSat, an unregulated bus would be a design where the battery is directly connected, meaning the battery voltage defines the bus voltage. The solar input voltage is set at the maximum battery voltage, allowing for battery charging to occur when receiving solar energy. When not receiving any solar energy, the bus will deliver whatever the battery voltage happens to be, this is the unregulated portion. Because of this variability, it is important that power distribution circuitry can handle the range of input voltages expected. For a simple example, we will use the new solar cells suggested in a previous section to serve as our solar input and we will use the components listed in the example power bus to serve as our subsystems.

The bus voltage is set to be a range between 4.2 volts and 3.4 volts, which is the range of voltages the battery could be depending on it's charge level. The solar input must be set at 4.2 volts to allow charging to occur at any point in orbit. If the battery is below 4.2 volts, some current from the solar input will flow into the battery to charge. Any of the power distribution outputs must be able to take 3.4 to 4.2 volts and convert to the required output. The block system below shows the required voltage compatibilities to create a dynamic voltage bus. The way this diagram was created makes it more akin to a system block diagram. By adding additional circuit elements such as switches and monitoring ICs, this diagram can become a full system block diagram for a CubeSat power system. Redundancies may also be needed to cover failures of any kind. The design below is an interconnected power system with distributed regulation. Each power user has a component that will regulate voltage for itself. Each regulator is user specific that connects to a general bus.

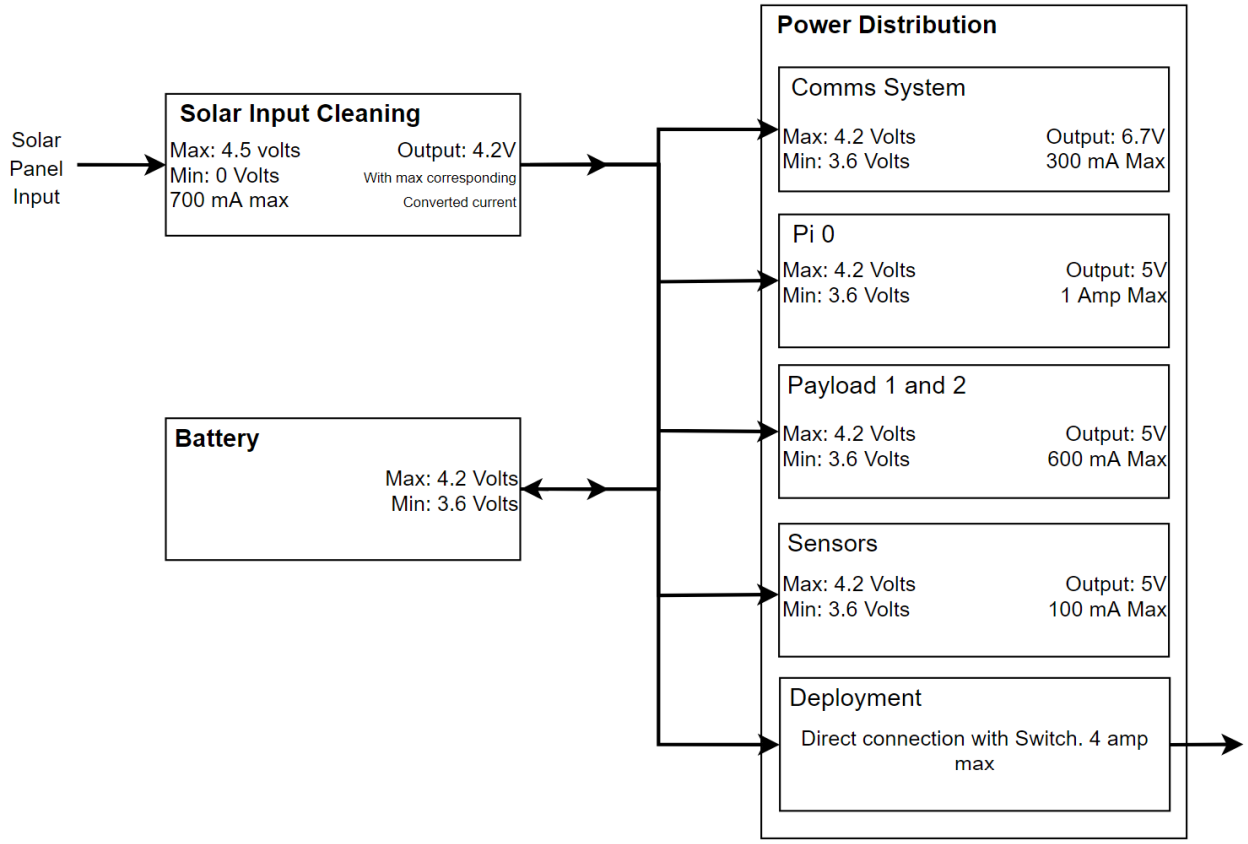


Figure 53 – A basic block diagram/interface combo that describes the needed voltage compatibilities of the circuit elements. The elements supply the 3 roles of a power board, solar input and cleaning, power storage, and Power distribution.

In the design above, batteries could be put in series to effectively double the Bus voltage. This will also increase the range of voltages that the bus can be, creating the need for more dynamic components. An increase in bus voltage will also improve the health of the power design's parts due to there being a lower current flowing through them. This design also uses a completely interconnected system where the Battery and components act as users for the solar input block when in sunlight. In eclipse, the components act like users for the Battery. The bus

itself is very dynamic and allows current to go where it needs to go, whether it be charge the battery or power the Pi 0, in this example.

A second example is provided below. This also uses an interconnected power system with distributed power delivery. This example is more in depth in terms of block types, controls, and activities. The system below runs on a 5 Volt bus that is centralized, meaning all activity happens through this bus. The Batteries are configured with 2 in series to raise the voltage of the power storage system. Included in this design are also switches to control the state of subsystems as well as a deployment port, used to perform actions like nichrome burns. Because the bus is fully regulated and regulated at 5 volts, many of the systems that exist on a CACTUS-like CubeSat can be serviced. The main point of failure would be the charging and discharging circuity. This circuitry will have to be able to output upwards of 1.5 Amps of current at 5 volts with all systems running at max power. This diagram is also detailed enough to include an I2C chip that can switch on and off subsystems when needed and monitor battery charge level and charging rate. This device would communicate with the Pi 0 over the PC/104 ISA interface on the power board.

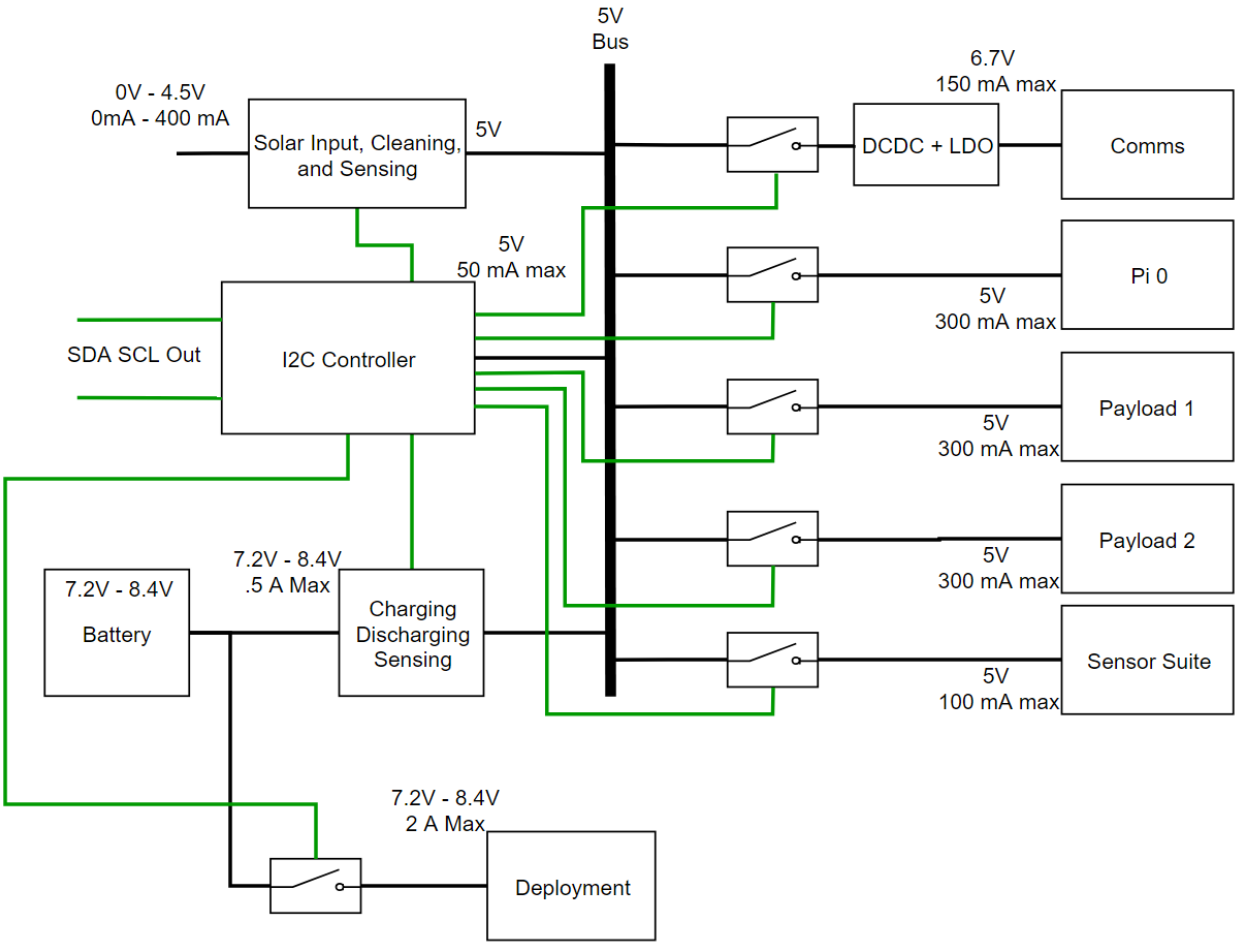


Figure 54 – A more detailed bus design using a centralized, fully regulated bus. This diagram also includes Sensing and switching capabilities using some small chip with I2C protocols.

With the design above, another power budget could be created; As was said in the power budgeting section, another column can be added for efficiency. By estimating the efficiency of each type of voltage converter, the actual power usage can be found and accounted for each subsystem in the budget. This will make the power budget much more accurate and predict the real behaviors more accurately.

Modeling Files

CADD Models

- All files are created using Autodesk Inventor Professional 2018.
- CADD Models are contained within the CADD folder.
- The directory structure within the CADD folder should remain untouched. Part sourcing will be affected otherwise.
- Custom parts are given custom names.
- Parts from vendors use the given part number as the name.
- Parts from vendors are typically in folders from where they were found, ex Mouser, Didi-Key, or McMaster
- If copying an assembly file (.iam) to a new location be sure to copy the parts as well. If this becomes confusing, follow this procedure:
    1. With the assembly file open in Inventor, Clock on File in the top left-hand corner
    2. Hover mouse over the Save As button
    3. Select the Pack and Go option that comes up in the next menu
    4. A popup may appear, simply hit ok until a very large dialogue window comes up
    5. In the destination folder, pick the folder where the assembly file needs to go.
    6. For the project file, the Default.ipj should be fine for now, ignore it.
    7. Hit the search now button, this will return all the files that are used in the assembly
    8. Hit the start button, this will export the files to the desired location
    9. Once the green bar has filled and the Done button is clickable, hit done
    10. Done!

CADD File Descriptions

Inventor Assembly Files will be identified here.

INTERFACE 1

This is interface 1 covered in the systems guidance section. Using PC104 ISA connections and extended them past one shell into another.

INTERFACE 2

This is interface 2 covered in the systems guidance sections. Using a D-sub connector between shells to allow proper interfaces for Shells that do not contain PC104 Boards, meant for payload interfaces.

PC104 ISA BOARD LOW PROFILE

This is the PC104 board with a low-profile header installed. This Header is part of the SSQ product line from SAMTEC. Use this header to shorten the PC1-4 stack if needed.

PC104 ISA BOARD VERY LOW PROFILE

This is a PC104 board with a very low-profile header from SAMTEC installed. This header has the same socket height as the Low profile, but it has smaller male pins, allowing boards to mate as close as possible.

PC104 ISA BOARD

This is the Standard PC 104 board with an ESQ Header from SAMTEC installed. Most models are using this board assembly because it is standard.

PC104 ISA CUT END

This is a Copy of the PC104 ISA assembly except the male pins are cut off, this is used as the bottom board is a PC104 stack.

PC104 ISA CUT INTERFACE 1

This board has all but 40 Male pins cute, the 40 male pins not cut are used as the mating interface for the INTERFACE 1.

PC104 STACK USB INTERFACE

This is a Copy of the PC104 STACK assembly but a small USB model is included. This USB model is to represent a veritably mounted USB on one of the boards. This USB can be accessed by one of the end mounts, which has s hole in it. The point of this Model is to show how easy it is to put a proper USB interface into a Bus.

PC104 STACK VERY LOW PROFILE

This is a PC104 Stack of 5 boards using the lowest profile ISA interface connectors. This demonstrates how small a stack of boards can be. Using a mix of low profile and standard profile is expected on a future CubeSat.

PC104 STACK

The PC104 Stack uses standard height PC104 boards to create a 5-board stack. End mount are used on either end to close off the stack. The stack uses threaded stand offs and screws as decided upon from the short trade study performed in the mechanical section.

SOALR PACKING

A very basic 100 x 95 mm solar panel with Panels mounted from the Solar guidance section. This was a test does to see what could be feasible using these panels. If a shell was 100 mm long (The CACTUS Bus was 86 mm long) then the solar panel that could fit to it would generate about 800 mW of power.

EAGLE PCB Files

- All files were created using the latest version of EAGLE: 8.5.0 Free
- All PCB Files are Contained in the EAGLE PCBs folder
- PCB Files come in pairs, the schematic (.sch) and board (.brd) files are linked together via the file name. Do not separate these files or they will not be compatible after editing
    - Edits in the board files will be reflected in the schematic file, if both files are open when working on one or the other.
- All files are contained under the 'Future CubeSat Demos' folder. For EAGLE to detect this project, the project and its contents will need to be moved to the default eagle project directory, this is a folder labeled 'Eagle' typically located in My Documents on windows. Move the entire folder 'Future CubeSat Demos' to this default Eagle directory, that will move the project file along with the contents and keep things organized.
- Eagle will hopefully detect this project, if not, follow this procedure:
    1. With the EAGLE Control Panel open, hit file
    2. Select open
    3. Select Project
    4. Select Eagle (this is the default folder that you have moved files to)
    5. Select the project, it should be listed as the directory; 'Future CubeSat Demos'
- The library file (.lib) holds information on the parts, custom made or otherwise, that are used in the boards and schematics, it's important that this library also stay with the board and schematic files. So when copying board and schematic files, copy the library file as well.
- To create PCBs many companies will take Eagle board files, like PCB Cart for example. If they do not and require Gerber files, more research will be needed to create a CAM job that can generate the Gerber files for you.

PCB File Descriptions

Bus Solar V2 Packed with pads (.brd and .sch)

This is the same board geometry of the Bus panel from CACTUS-I. What has changed is the Pad geometry has been improved and the cells have been packed closer together for better performance. The cells were packed together as close as they are based on experience from building the PCBs. Better pads reduce the work needed to build and more cells improved the yield of the panels.

DEMO Bus Panel (.brd and .sch)

This board is a 90 x 80 mm PCB with new solar panels mounted on it. The panels used are the same panels suggested in the Solar panel guidance section. With this design, the panel will generate 800 mW of power.

PC104 ISA TEMPLATE

These are Template PC104 design files. Copy both the board and schematic files, then rename them TO THE SAME NAME and begin designing a new PC104 board!