Block diagram – GCM_V5 – Revision 1

Main connector
MOM1_SPS1
standard

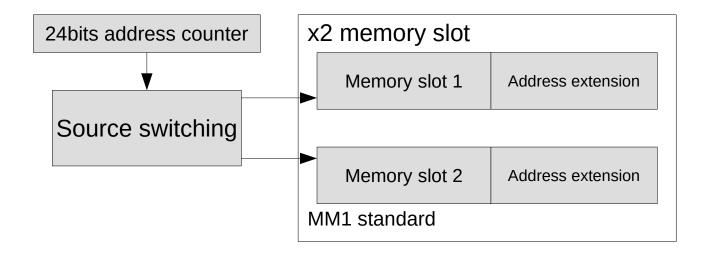
Peripheral communication
4 peripherals
2Byte writable bus
2Byte readable bus

24Bits address/jump bus
50Mhz controlable

External clock
50Mhz controlable

Clock generation 50Mhz divisible by 65536 max

SPI Connector



x4 peripherals slot

P0

P1

P2

P3

PP1 standard

Features depend of the processor