

Block diagram – GCM_V4 – Revision 1

Main connector

Peripheral communication
5Bits peripheral selection

24Bits address/jump bus

50Mhz max theoretical

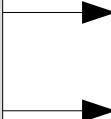
Clock generation
1kHz to 50Mhz (68Mhz max)

SPI Connector

24bits timer



Source switching



x2 memory slot

Memory slot 1 Address expansion

Memory slot 2 Address expansion

16bits address + 8bits expendable

x4 peripherals slot

P0
P1
P2
P3