1. Introduction

The report for the Amplifier Design Project is presented herein. In order to meet the project's objectives, a single-supply, multistage, inverted transistor amplifier had to be designed, simulated, analyzed, implemented, and tested using Multisim. All manual calculations can be found in the appendix and all simulations were done on Multisim.

2. Objectives

The objective of this experiment was to design a transistor amplifier that met certain conditions.
These specifications are:

- Power supply: $+\mathbf{10}\boldsymbol{V}$ relative to the ground;
- Quiescent current drawn from the power supply: no larger than $\mathbf{10}\ \boldsymbol{mA}$;
- No-load voltage gain (at 1 kHz): $|\boldsymbol{Avo}|$ = $\mathbf{50}$ (± $\mathbf{10}$%);
- Maximum no-load output voltage swing (at 1 kHz): no smaller than 8 V peak to peak;
- Loaded voltage gain (at 1 kHz and with RL = 1 $k\Omega$): no smaller than $\mathbf{90}$% of the no-load voltage gain;
- Maximum loaded output voltage swing (at 1 kHz and RL = 1 $k\Omega$): no smaller than 4 V peak to peak;
- Input resistance (at 1 kHz): no smaller than $\mathbf{20}\ \boldsymbol{k\Omega}$;
- Amplifier type: inverting or non-inverting;
- Frequency response: 20 Hz to 50 kHz ($\mathbf{-3}\boldsymbol{dB}$ response);
- Type of transistors: BJT;
- Number of transistors (stages): no more than 3;
- Resistances permitted: values smaller than $\mathbf{220}\ \boldsymbol{k\Omega}$ from the E24 series;
- Capacitors permitted: $\mathbf{0.1}\ \boldsymbol{\mu F}$, $\mathbf{1.0}\ \boldsymbol{\mu F}$, $\mathbf{2.2}\ \boldsymbol{\mu F}$, $\mathbf{4.7}\ \boldsymbol{\mu F}$, $\mathbf{10}\ \boldsymbol{\mu F}$, $\mathbf{47}\ \boldsymbol{\mu F}$, $\mathbf{100}\ \boldsymbol{\mu F}$, $\mathbf{220}\ \boldsymbol{\mu F}$;
- Other components (BJTs, diodes, Zener diodes, etc.): only from your ELE404 lab kit.

3. Circuit under Test

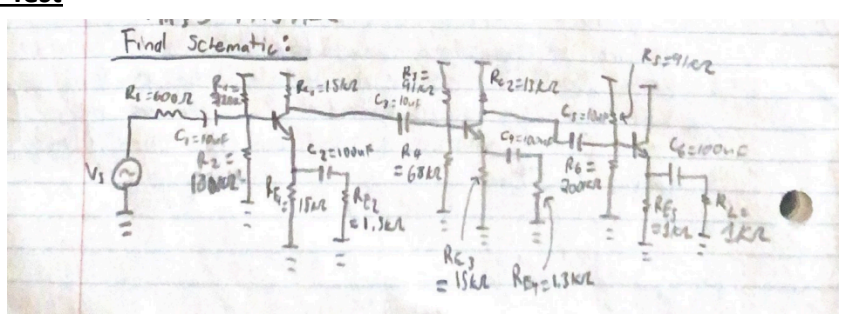


Figure 1. CE-CE-CC Designed Circuit schematic

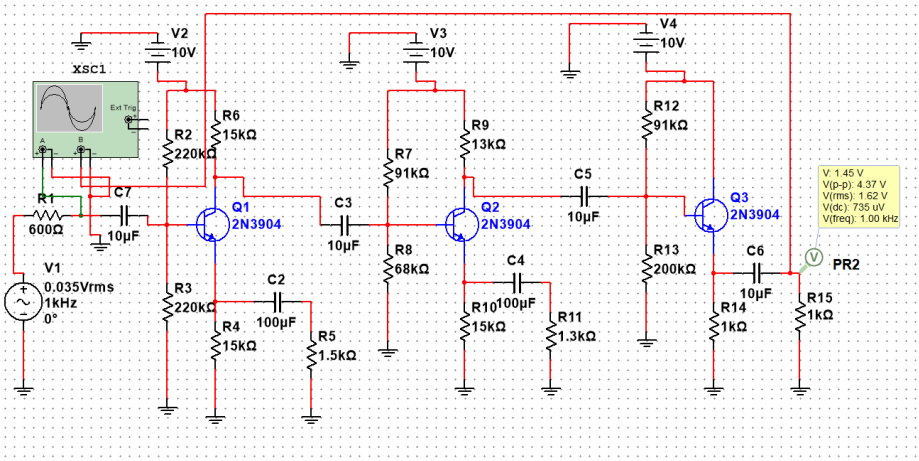


Figure 2. Constructed Circuit of **Figure 1** on Multisim with load resistance

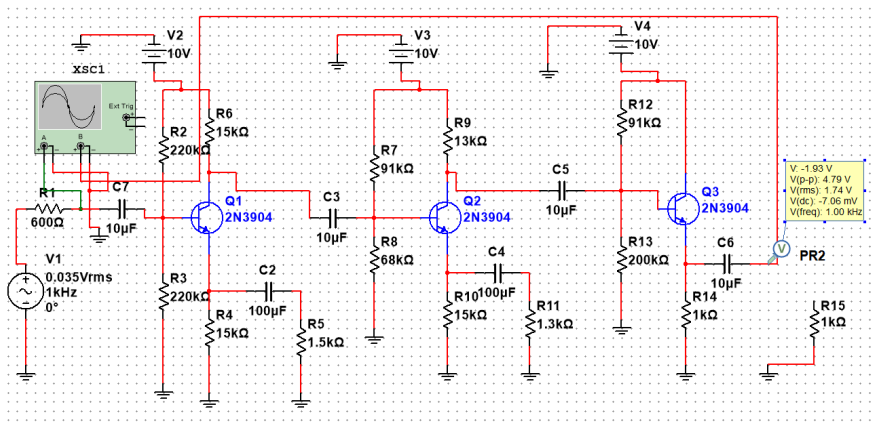


Figure 3. Constructed Circuit of **Figure 1** on Multisim without load resistance

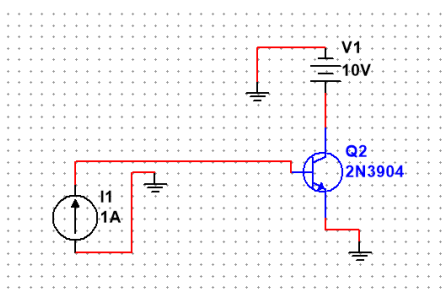


Figure 4. Circuit used to determine Load Line

4. Experimental Results

Table A. Calculated Biasing Resistance Values

R_1	R_2	R_3	R_4	R_5	R_6
220 kΩ	180 kΩ	91 kΩ	68 kΩ	91 kΩ	200 kΩ

Table B. Calculated Collector and Emitter Resistance Values

R_{E1}	R_{E2}	R_{E3}	R_{E4}	R_{E5}	R_{C1}	R_{C2}	R_L
15 kΩ	1.5 kΩ	15 kΩ	1.3 kΩ	1 kΩ	15 kΩ	13 kΩ	1 kΩ

Table C. Calculated Capacitor Values

C_1	C_2	C_3	C_4	C_5	C_6
10 µF	100 µF	10 µF	100 µF	10 µF	100 µF

Table D. Calculated Values From CC Stage

I_B	$I_{B,DC}$	β	I_C	V	g_m
65 mA	30 µA	153.8	10 mA	5 V	0.385 S

Table E. Calculated Values From CE Stages

I_B	$I_{B,DC}$	β	I_C	V	g_m
3.5 µA	2 µA	114.3	400 µA	4.25 V	0.0154 S

Process:

I went with a three-stage amplifier with Rin ≥ 20 kΩ and a gain of 50. One CC (common cathode/emitter follower) stage and two CE (common emitter) stages are included in the design. In order to make the computations simpler, I calculated the square root of 50, which is roughly 7.1. If I were to multiply the gains from stages 1 and 2, making them equal to -7.1 each, the result would be roughly 50. Because the final stage is a CC, the third stage's gain will be nearly unity, or about 1. Because stages 1 and 2 have equal gains, this guarantees that the voltage gain can be around 50 and that neither will affect the other's operating conditions. The testing circuit was simulated in Multisim using DC sweep to produce the characteristic graph, which allowed the remaining computations to start. A load line was manually constructed, and because of the limited power supply current restriction, a low collector current of 400 A was selected for both CEs. Additionally, this was done for the CC stage. An operating point (quiescent) was chosen from the graphs and served as the beginning point for the human computations (see appendix). The computations began at the final stage (CC) and worked their way backward to the initial stage. The CC emitter resistor was selected in order to ensure that

there would be no noticeable changes when RL is added or removed, as the load (RL) was required to be 1 kΩ. From this point on, the CC's input resistance was computed and utilized in the CE stage 2 calculations (this is the reverse process of moving from stage 3 to stage 1). By assuming that one of the biasing resistors is sufficiently large to cause the divider current to be noticeably greater than the base current, and then using KCL at the node to solve for the other resistor, the biasing resistors for each step were determined. This KCL calculation used the base current, voltage, and DC operating point current from the graphs. The same calculating process was carried out in stage 1 utilizing the input resistance of the second stage since the gains of stages 1 and 2 were made equal. Consequently, a CC amplifier was added to the final circuit design after two cascading CEs.

Resistors/Capacitors:

The choice of resistors was made based on the location. First, using the current and the input resistance of the subsequent step, the emitter and collector resistors were determined. The emitter resistor of the CC stage, RE5 = 1 kΩ, was considered to have a resistance that would not greatly affect the circuit's loading effect when the load is added or removed. Second, the needed gain for each stage was taken into consideration while selecting the emitter degeneration resistors. Since RE (total necessary emitter resistance) equaled the parallel combination of the emitter resistor and emitter degeneration resistor, it was possible to solve for it by rearranging the gain equation. Finally, in order to ensure sufficient current, the remaining biasing resistors were selected to be as large as possible. The input resistance drastically drops if the biasing resistors were too little, which has a major loading effect on the circuit. The original assumptions for each capacitor were tested by calculations (all manual calculations are included in the appendix). The values of the capacitors would vary based on the location and operating frequency. Since the input resistances of the amplifier stages are relatively substantial, C1, C3, and C5 were all 10 µF because coupling capacitors in between stages would require a significant change in resistance to significantly alter the overall circuit characteristic. However, since C2, C4, and C6 are attached to the emitter degeneration resistors, they were all 100 µF. Because tiny changes to the emitter degeneration resistor can have a significant impact on the gain, a large capacitance is required to ensure that resistance does not vary significantly.

Results from Simulation:

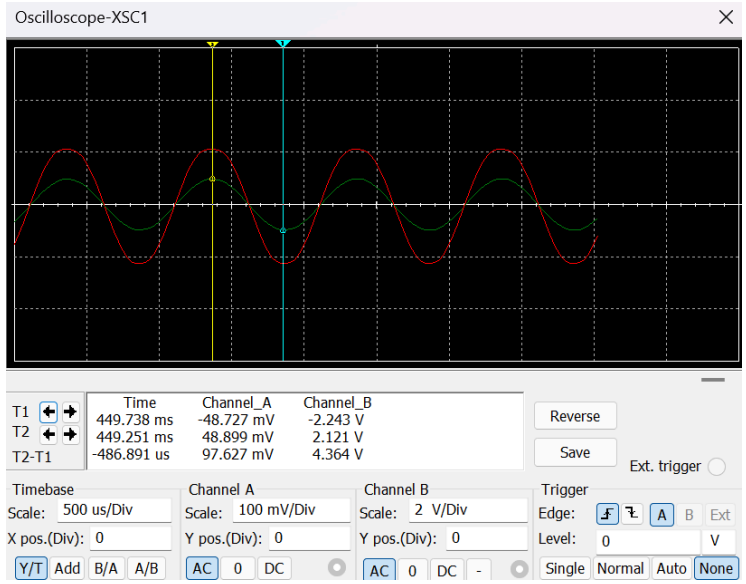


Figure 5. The waveform of input voltage and output voltage of **Figure 2** (RL = 1 kΩ)

Table F. V_I , V_O, A_V (loaded voltage gain) ⟶ RL = 1 kΩ, f = 1 kHz

$V_{I,\ P\text{-}P}$ [mV]	$V_{O,\ P\text{-}P}$ [V]	A_{VO} [V/V]
97.627	4.364	44.70

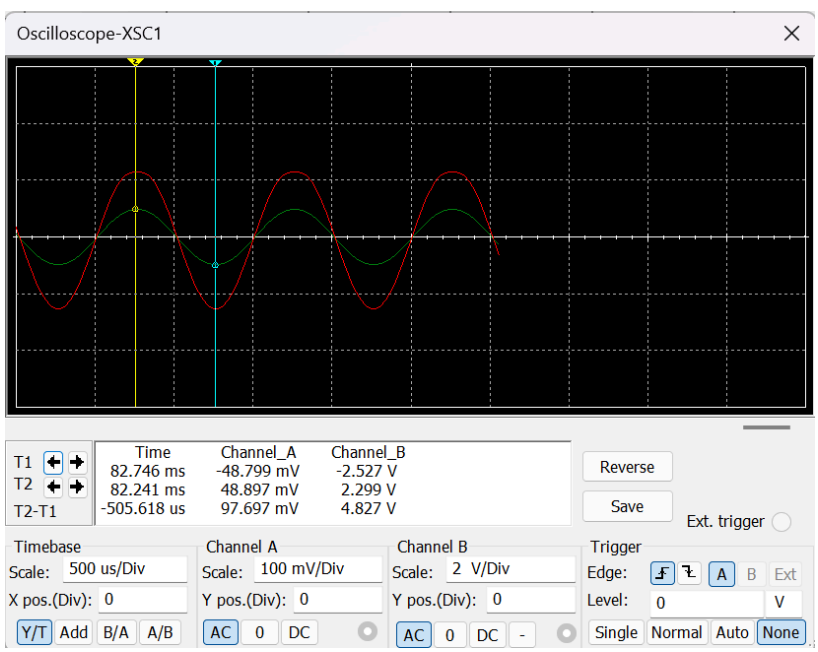


Figure 6. The waveform of input voltage and output voltage of **Figure 3** (RL = ∞)

Table G. V_I , V_O, A_V (loaded voltage gain) → RL = ∞ , f = 1 kHz

$V_{I,\ P\text{-}P}$ [mV]	$V_{O,\ P\text{-}P}$ [V]	A_{VO} [V/V]
97.697	4.827	49.41

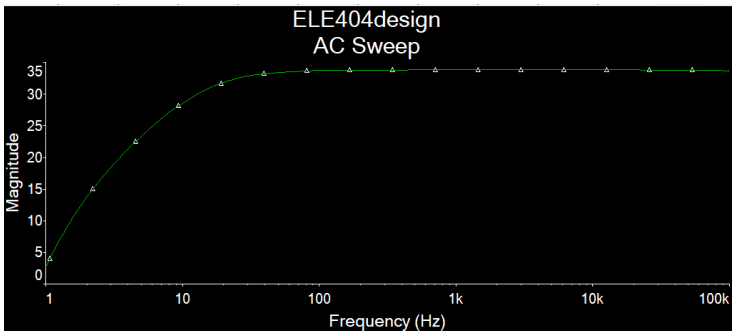


Figure 7. Frequency Response Graph of the Circuit

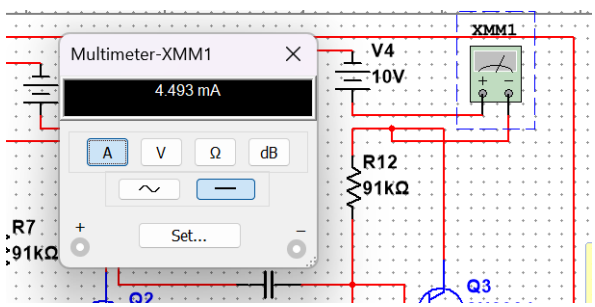


Figure 8. Quiescent Current drawn from power supply

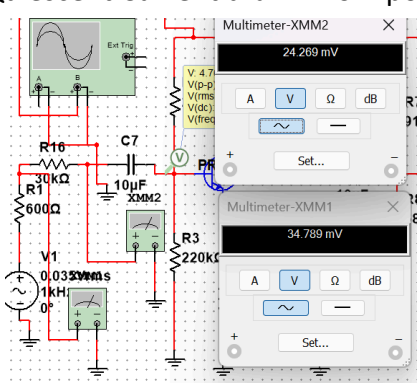


Figure 9. Finding V_t and V_i with new $R_{t,\ in}$

$$R_i = R_{t,\ in}\left(\frac{V_i}{V_t - V_i}\right)$$

Table H. Parameters of the equation used to find input resistance (Ri)

$R_{i,\ Calculated}$ [kΩ]	$R_{t,\ in}$ [kΩ]	$V_{t\ [Vrms]}$	$V_{i\ [Vrms]}$	R_i [kΩ]

60.76	30	34.789	24.269	69.21

5. Conclusions and Remarks

Table I. Design Specifications

Specification	Calculated Value	Simulation Value	Achieved
Power supply: +$\mathbf{10V}$ relative to the ground	10V	10V	Yes
Quiescent current: no larger than $\mathbf{10\ mA}$	5.19mA	4.493mA (< 10mA)	Yes
No-load voltage gain $\lvert Avo \rvert$ = $\mathbf{50}$ (± $\mathbf{10}$%)	50.41	49.41	Yes
Maximum no-load output voltage swing: ≥8 V peak to peak	8 $V_{p\text{-}p}$	4.827 $V_{p\text{-}p}$	No
Loaded voltage gain: no smaller than $\mathbf{90}$% of the no-load voltage gain	47.57	44.70 (no smaller than 90% of no-load voltage gain)	Yes
Maximum loaded output voltage swing: ≥4 V peak to peak	4 $V_{p\text{-}p}$	4.364 $V_{p\text{-}p}$	Yes
Input resistance: ≥$\mathbf{20\ k\Omega}$	60.76 kΩ	69.21 kΩ	Yes
Frequency response: 20 Hz to 50 kHz	N/A	View **Figure 6**	Yes
Type of transistors: BJT	Yes	Yes	Yes
Number of transistors (stages): no more	3	3	Yes

than 3			
Resistances permitted: smaller than $\mathbf{220\ k\Omega}$ from the E24 series	Yes	Yes	Yes
Capacitors permitted: $\mathbf{0.1\ \mu F}$, $\mathbf{1.0\ \mu F}$, $\mathbf{2.2\ \mu F}$, $\mathbf{4.7\ \mu F}$, $\mathbf{10\ \mu F}$, $\mathbf{47\ \mu F}$, $\mathbf{100\ \mu F}$, $\mathbf{220\ \mu F}$	Yes	Yes	Yes

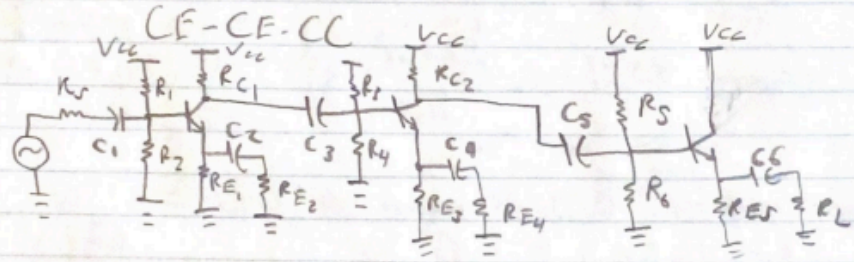
Except for the no-load voltage fluctuation, every requirement for the design was satisfied with little error. Despite the manual calculations suggesting that this would be possible, the Multisim simulation shows that this is not the case. This small error is most likely the result of biasing or the operating point selection based on the load line graphs. Ultimately, despite this small inaccuracy, the circuit's properties remained unaffected because all other essential requirements—such as the voltage gain, input resistance, and frequency response—were satisfied. Any assumptions derived from the load line graphs and human calculation rounding are probably the causes of the smallest percent inaccuracies for the other measurements. Consequently, the 3-stage (CE-CE-CC) design was a successful way to accomplish the project's goals, and all of the efforts, including the manual calculations and the Multisim experiment, proved to be successful.

Appendix:

ELE 404

Design Project

CE-CE-CC



Known elements:

$V_{CC} = 10V$

$I_{DC} < 10mA$

$A_{vo} = 50 \pm 10\%$

$V_o \geq 8\ V_{pp}$

$V_L \geq 4\ V_{pp}$

$R_{in} \geq 20k\Omega$

all $R \leq 220k\Omega$

A_{vo} approximation:

$A_{vo} = A_{vo_1} \times A_{vo_2} \times A_{vo_3}$

$50 = A_{vo_1} \times A_{vo_2} \times 1$

Assume A_{vo_1} and A_{vo_2} are equal

$A_{vo_1} = \frac{V_2}{V_1} = -7.1$

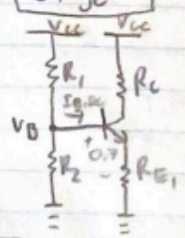
$A_{vo_2} = -7.1$

$\sqrt{50} \approx 7.1$

* Assume $\beta = 150$

Since A_{vo_3} is a CC the gain is close to unity.

Stage 1



$V_B = \frac{R_2}{R_1 + R_2} \cdot V_{CC} = \frac{220k\Omega}{220+220k} \cdot 10V = 5V$

$I_{C,DC} = \frac{V_{CC}}{R_C + R_{E_1}} \rightarrow R_C + R_{E_1} = 25k\Omega$

KVL: $-V_B + 0.7 + I_E R_{E_1} = 0$

$(1+\beta) I_B R_{E_1} = 5 - 0.7V$

$R_{E_1} = 4.3V / (115.3)(2\mu A)$

$\therefore R_{E_1} = 18647.00 \approx 18k\Omega$

$R_C + R_{E_1} = 25k\Omega$

$\therefore R_C = 25k\Omega - 18k\Omega = 6.8k\Omega$

$R_c = R_{c_1} \| R_{in_2}$

Based on load line

$I_C = 400mA$

$g_m = \frac{I_C}{V_t} = \frac{400mA}{26mV} = 0.015S$

$\beta = \frac{I_C}{I_B} = \frac{400mA}{3.5mA} = 114.3$

$I_{B,DC} = 2\mu A$

Stage 3 : CC

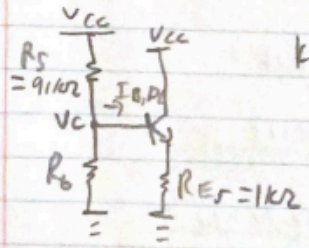
I assume $R_{E5} = 1k\Omega$ to be close to load resistance value.

From load line:

$I_C = 10mA$ $\quad \beta = I_C / I_B = 10mA / 65\mu A \doteq 153.8$ $\quad g_m = \frac{10mA}{26mV} = 0.385\,S$

$I_B = 65\mu A$ $\quad I_{B,DC} = 30\mu A$

Let $R_5 = 91k\Omega$ to ensure the divider current is larger than I_B.

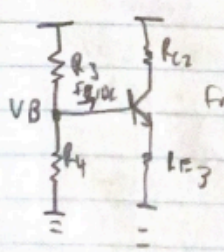


KCL @ V_C: $\frac{5-10}{91k} + \frac{5}{R_6} + 30\mu A = 0$

$R_6 = \frac{5V}{24.95\mu A} = 200498.52$

$\therefore R_6 \approx 200k\Omega$

Stage 2 : CE



KVL @

$-V_{B,DC} + 0.7V + I_E(R_{E3}) = 0$

From load line

$R_{E3} = \frac{3.55}{(115.3)(2mA)} = 153946.227\Omega$

$\therefore R_{E3} \approx 15k\Omega$

$R_C + R_{E3} = \frac{V_{CC}}{I_{C,DC}} = \frac{10V}{400mA} = 25k\Omega$

$\therefore R_C = 25k\Omega - 15k\Omega = 10k\Omega$

Find R_{C2}:

$R_{in3} = R_5 \| R_6 \| \frac{\beta}{g_m} + (\beta+1)R_E$

$R_{in3} = 91k\Omega \| 200k\Omega \| \frac{153.8}{0.385} + (154.8)(1k\Omega)$

$\therefore R_{in3} = 44.57k\Omega$

$\frac{1}{R_{C2}} = \frac{1}{10k\Omega} - \frac{1}{44.57k\Omega}$

$\therefore R_{C2} \approx 13k\Omega$

Find R_E:

$$A_{vo_2} = \frac{V_{3n}}{V_{2n}} = \frac{-g_{m_2}(R_{C_2} \| R_{in_3})}{1 + g_{m_2} R_E}$$

Use assumption that $A_{vo_2} = -7.1$

$$-7.1 = \frac{-0.0154(13k\Omega \| 44.57k)}{1 + 0.0154(R_E)}$$

$$R_E = \left(\frac{-154.99}{-7.1} - 1\right) \div 0.0154$$

$$\therefore R_E = 1352.59 \approx 1.3k\Omega$$

$$A_{v2}(\text{with load}) = \frac{-g_{m_2}(R_{C_2} \| R_{in_3})}{1 + g_{m_2} R_E}$$

$$= \frac{-0.0154(13k\Omega \| 44.57k\Omega)}{1 + 0.0154(1.3k\Omega)}$$

$$= -6.66 \approx \underline{-6.7}$$

Find R_{E4}:

$R_E = 1353\Omega$

$R_E \approx 1.3k\Omega$

$R_E = R_{E3} \| R_{E4}$

$\frac{1}{1.3k\Omega} = \frac{1}{15k\Omega} + \frac{1}{R_{E4}}$

$R_{E4} = 1423.35\Omega$

$\therefore R_{E4} \approx 1.3k\Omega$

I assume $R_3 = 91k\Omega$ to ensure the divider current is much larger than I_B.

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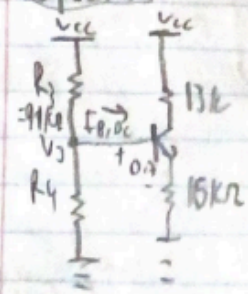


KCL @ V_3: $\frac{4.25 - 10}{91k} + \frac{4.25}{R_4} + (2\mu A) = 0$

$$R_4 = \frac{2uA - \left(\frac{4.25-10}{91k\Omega}\right)}{4.25}$$

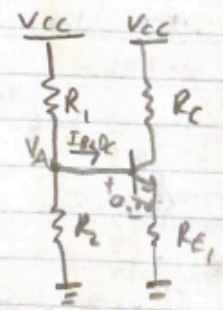
$R_4 = 69459.41\Omega$

$\therefore R_4 \approx 68k\Omega$

Find R_{in2}:

$$R_{in2} = R_3 \parallel R_4 \parallel \frac{\beta}{g_m} + (\beta+1)R_E$$
$$R_{in2} = 91k \parallel 68k \parallel \frac{114.3}{0.0154} (115.3)(1.3k)$$
$$R_{in2} = 31432.72$$
$$R_{in2} \approx 31.4\,k\Omega$$

Stage 1: CE



$$I_{C,DC} = \frac{V_{CC}}{R_C + R_{E_1}}$$
$$R_C + R_{E_1} = \frac{10V}{400\mu A}$$
$$R_C + R_{E_1} = 25k\Omega$$

use value 1kΩ for R_{E_1}

$$R_C = 25k\Omega - R_{E_1}$$
$$R_C = 10\,k\Omega$$

KVL: $-V_A + 0.7 + I_E R_{E_1} = 0$

$$R_{E_1} = \frac{V_A - 0.7}{(\beta+1)I_B} = \frac{3.55}{(115.3)(2\mu)}$$

$$R_{E_1} = 15394.62 \approx 15k\Omega$$

Find R_{C_1}:

$$R_C = R_{C_1} \parallel R_{in2}$$
$$10k = \frac{1}{\frac{1}{R_{C_1}} + \frac{1}{31.4k}}$$

$R_{C_1} = 14665$
$R_{C_1} \approx 15k\Omega$

Use gain equation to find R_E

$$A_{v_1} = \frac{-g_m (R_{C_1} \parallel R_{in2})}{1 + g_m R_E}$$
$$-7.1 = \frac{-0.0154(15k\Omega \parallel 31.4k\Omega)}{1 + 0.0154(R_E)}$$
$$R_E = \left(\frac{-150.5}{-7.1} - 1\right) \div 0.0154$$
$$\therefore R_E \approx 1.3k\Omega$$

Find R_{E2}:

$$R_E = R_{E_1} \parallel R_{E2}$$
$$1.3k = \frac{1}{\frac{1}{1k} + \frac{1}{R_{E2}}}$$
$$R_{E2} = 1432.3$$
$$R_{E2} \approx 1.5\,k\Omega$$

I will assume R_1 to be 220 kΩ because this will make the divider current to be larger than the base current.

KCL, to solve for R_2

$$\frac{4.25-10}{220k} + \frac{4.25}{R_2} + 2mA = 0$$

$$4.25/R_2 = \left(-\frac{4.25-10}{220k}\right) - 2mA$$

$$R_2 = 176082.86$$

$$R_2 \approx 180k\Omega$$

Find R_{in_1}:

$$R_{in_1} = R_1 \parallel R_2 \parallel \frac{\beta}{g_m} + (\beta+1)R_E$$

$$R_{in_1} = 220k \parallel 180k \parallel \frac{114.3}{0.0154}(115.3)(1.5k)$$

$$R_{in_1} = 60761.45\ \Omega$$

$$R_{in_1} \approx 60.76\ k\Omega$$

Determine capacitor values

→ C_2, C_4, C_6 values should be larger to maintain gain of CE stages

→ C_1, C_3, C_5 not as large because input resistances are large

Frequency range: 20 kHz – 50 kHz

I will pick value of 100 uF and 10 uF

Worst case	Best case	Avg case
f = 20 kHz	f = 50 kHz	f = 1 kHz ← frequency
100uF $Z = \frac{1}{j2\pi fc}$	100uF $Z = \frac{1}{j2\pi(50kHz)(100uF)}$	100uF $Z = \frac{1}{j2\pi(1kHz)(100uF)}$
$= \frac{1}{j2\pi(20kHz)(100uF)}$	$Z = 31.8m\Omega$	$Z = 1.6\Omega$
$= 79.6\Omega$		
10uF $Z = \frac{1}{j2\pi(20kHz)(10uF)}$	10uF $Z = \frac{1}{j2\pi(50kHz)(10uF)}$	10uF $Z = \frac{1}{j2\pi(1kHz)(10uF)}$
$Z = 796\Omega$	$Z = 0.32\Omega$	$Z = 15.9\Omega$

By these calculations the circuit should maintain gain by using the chosen capacitor values.

Gain: $A_{v_0} = -7.1 \times -7.1 = 50.41$

$A_v = -6.7 \times -7.1 = 47.57$

There are 2 stages here since stage 3 is a CC where gain would be unity. A_v (with load) at the first CE will not have loading effect of R_L, so we use the calculated value of -6.7 and the initially found value of -7.1.

$$I_{DC,total} = I_{C_1} + I_{R_1} + I_{C_2} + I_{R_2} + I_{C_3} + I_{R_5}$$

$$I_{DC,total} = \beta I_{B_1} + \frac{V_{CC}}{R_1+R_2} + \beta I_{B_2} + \frac{V_{CC}}{R_3+R_4} + \beta I_{B_3} + \frac{V_{CC}}{R_5+R_6}$$

$$I_{DC,total} = (114.3)(2\mu) + \frac{10}{(220+220)k} + (114.3)(2\mu) + \frac{10}{91k+68k} + (153.8)(2\mu) + \frac{10}{200k+91k}$$

$$I_{DC,total} = 0.00519\ldots A$$

$$I_{DC,total} \approx 5.19\ mA \rightarrow \boxed{5.19mA < 10mA}$$

Values determined:

$R_1 = 220k\Omega$ $R_{C_1} = 15k\Omega$ $R_{E_3} = 15k\Omega$ $R_{E_5} = 1k\Omega$

$R_2 = 180k\Omega$ $R_3 = 91k\Omega$ $R_{E_4} = 1.3k\Omega$

$R_{E_1} = 15k\Omega$ $R_4 = 68k\Omega$ $R_5 = 91k\Omega$

$R_{E_2} = 1.5k\Omega$ $R_{C_2} = 13k\Omega$ $R_6 = 200k\Omega$

$C_1, C_3, C_5 = 10uF$

$C_2, C_4, C_6 = 100uF$

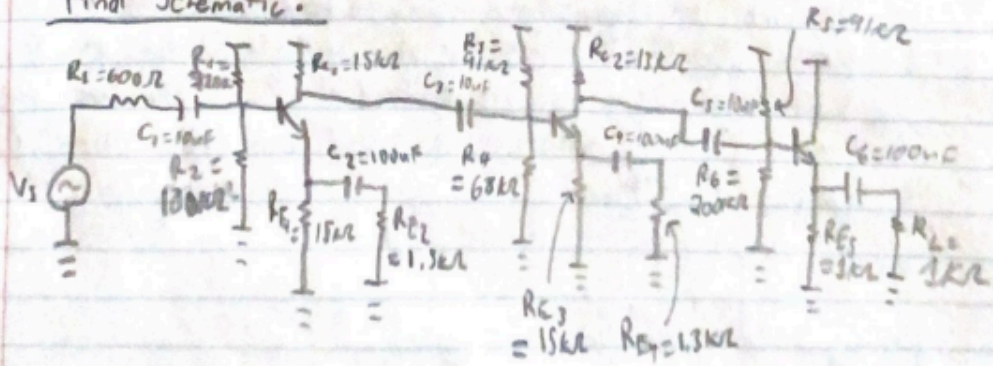
$I_{DC,total} = 5.19mA$

$A_v = 47.57$

$A_{vo} = 50.41$

$R_{in_1} = 60.76k\Omega$

$R_{in_2} = 31.4k\Omega$

$R_{in_3} = 44.57k\Omega$

Final Schematic: