University of California, Santa Cruz
Computer Engineering Department

Laboratory 4, PCB Project
Merging with Gerbtool

EE174, Intro to EDA Tools
S.C. Petersen

1. INTRODUCTION AND OBJECTIVES

This series of laboratories introduces the necessary practical skills associated with two popular Cadence Corp. EDA tools: schematic Capture and pcb Layout. You must have completed all of the earlier labs before attempting this advanced, final laboratory that specifically takes a completed electronic design and turns it into a real, fully constructed, printed circuit board. In this fourth laboratory, students use their skills with Capture and Allegro to realize their own unique designs and prepare them for submission to a real board house, one specializing in engineering prototype PCB's. Allegro will be used to learn how to tile or "panelize" homogeneous and heterogeneous boards. An introduction to state-of-the art surface-mount-technology is included, and will be discussed in lecture.

2. GENERAL DISCUSSION

The design and implementation of engineered circuits on printed circuit boards is seldom done in a single sequence leading to a final, otherwise perfect, design. Most projects include provisions for one or more intermediate **prototype** PCB boards meant specifically for hardware testing and debugging. This provides us with experimental feedback that devoted to refining and perfecting the overall engineering design eventually concluding in a final acceptable circuit. Hence, many board houses have lower cost services aimed specifically at manufacturing prototype boards. These typically omit one or more of the services otherwise included in full final design manufacturing runs that may variously include:

- **Minimal pre-engineering design checks and machinery setup charges**. A full service run always includes a thorough check of your submitted PCB for physical errors, like unconnected traces, drill hole mismatches with padstacks, and boardhouse DRC requirements Indeed some board houses have a "no look" policy; what you submit is what you get!

- **Custom setup is omitted**. Prototype runs specifically minimize the need to customize the manufacturing process to accommodate your board. In other words, rather than setup the machinery just to do your PCB, prototype runs are designed to have you enter a manufacturing process already "setup" ahead of time.

- **Layers, board materials and special services**. Solder mask and silk screen layers may not be available. Certain services, like scoring and custom drill sizes may also be unavailable. Only restricted board materials may be used with limitations on minimum and maximum sizes. Most prototype services are for 2-layer boards, but some exist for 4-layer boards as well.

- **Limited Board Quantities**. Prototype runs are nearly always for a small number of boards, typically two. Hence, some houses may require exactly two, while others make this only a minimum. 4-layer prototype board runs usually restrict this to a specific number and don't allow tiling.

Prototype PCB services are very popular and usually well worth the cost. We will be submitting our designs in this lab to fabrication plant: **Alberta Printed Circuits** (www.apcircuits.com), located in Alberta, Canada. This board house "turns in 24 hrs", *i.e.* they will fully process an order submitted for their fastest service typically in 24 hours. APC currently offers three services: Basic Prototype, Plus Prototype and Multi-Layer. You should have already visited APC and tailored your tutorial board to take advantage of their two low-cost Prototype services. The technology template file used in lab 2 was designed to be used with boards submitted to this board house. You should particulary be careful to observe their no-cost drill and DRC recommendations (spacing rules are already defined in the Allegro technology template file used in lab-2). As noted in lab-2, this service provides 2-layer type FR4 62.5 mil glass-epoxy boards without silk-screen or soldermask layers.

3. PCB PROJECT ASSIGNMENT

You may choose any one of the designs found in the Lab 4 project's folder to implement. Custom designs are also permitted by consent of instructor. Your PCB may be any size you like (within the limits noted by the Boardhouse), providing it's rectangular (or square); sizes greater than 9 square inches (3x3 in) need instructor approval. Regardless of which project you choose, organize your work as you did in the earlier tutorial labs by first creating a set of working subdirectories under an aptly named parent project folder and create the usual minimum set of folders; note you can name the subdirectory containing your design files anything you like. Download and expand *Default Project Tree.zip* (or *rar*) file found on our website to begin a new project. Note this will follow the same general directory organization as for labs 1 and 2.

Relevant application notes and datasheets for each specific project have already been included in the **AppNotes** and **DataSheets** folders to help get you started. You may, of course, add whatever additional files you like.

Create schematics based on the engineering notes provided in the **AssignmentNotes** folder, making schematic symbols and layout footprints as needed.

After completing your board, tile it with additional student boards to fill out a single board, as large as will be acceptable to APC using their Basic Prototype (at the time of this writing the size is 14 x 17 inches). A sign-up list will be put on the whiteboard in BE104 for each board run. For practice, *all of you participating in a particular board run must also produce fully tiled boards of your own from everyone else's*, but only one fully tiled board will actually be submitted to APC and can be decided upon by each group. Tiling is discussed in the next section.

3.1 IMPORTING MULTIPLE PCB'S WITH GERBTOOL

GerbTool has a tool for tiling (its called "panelizing"), but it works only for duplicating homogeneous instances of the same already loaded PCB design. I want to show you a more powerful general way for tiling *any* set of designs, whether the same (homogenenous) or different (heterogeneous). Actually two methods exist for merging designs, one is more difficult and the second easy. We will use the easy method, that merges ***.GTD** files directly (remember, these contain all Gerber, aperture and drill information in a single file), but this relies on the requirement that heterogeneous boards *must first all be created using the same exported layers*. Since you are free to import any files you like in Gerbtool, be sure everyone agrees on which files these are and then save them as a single *.GDR file. Hence, *be sure that GerbTool's layer types and numbers agree for every board to be tiled together before beginning*. To merge GTD files, use the *Merge…* option in the File menu.

The second method is more versatile but requires more work. It relies on importing Gerber files directly and copying them to single common layers. Whenever Gerbtool imports Gerber files, they are always placed successively on the first set of empty layers. Therefore, if 7 files were imported, they would occupy layers 1 through 7; this was was discussed in lab-3, so you should already be familiar with the process. If an additional set of 1 or more layers is imported, even though they may have the same filenames and extensions, Gerbtool will place them sequentially beginning with layer 8. This is also true for imported NC drill files. The technique is to then copy the added layers to each earlier layer respectively. For example, I used the Wizard (try it) to import 8 files with the following results:
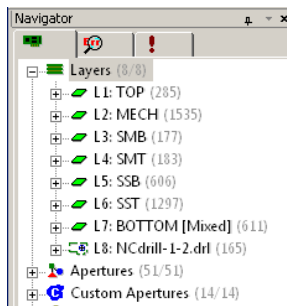
Gerbtool loads files in the order specified when using the Wizard, or the alpha order if imported manually. I deliberately re-ordered them from the alpha orders somewhat for sake of this example. Hence, we see the usual 8 files.
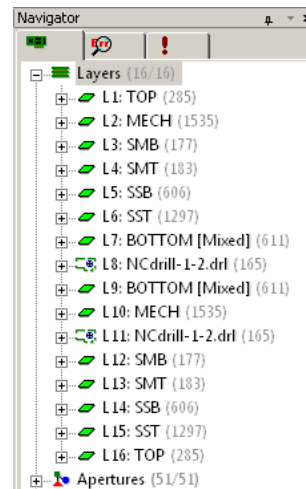
Now suppose I load the same files again but deliberately leave the default alpha order. Notice these were automatically placed on layers L9 through L16.
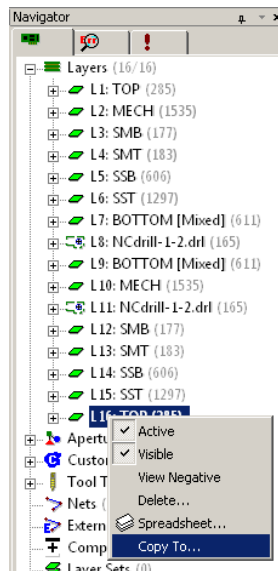
I then decide that L1 – L8 will be the layers I want to keep and contain the newly loaded design on L9 – L16. In other words I want to move L9 to L7 (Bottom); L16 to L1 (Top) etc. This is done by a "copy and delete" sequence: For example I'll do this with the Top layer. Select L16, right-click and select *Copy To…* as shown. This will bring up the *Select Layers* dialog shown on the next page.
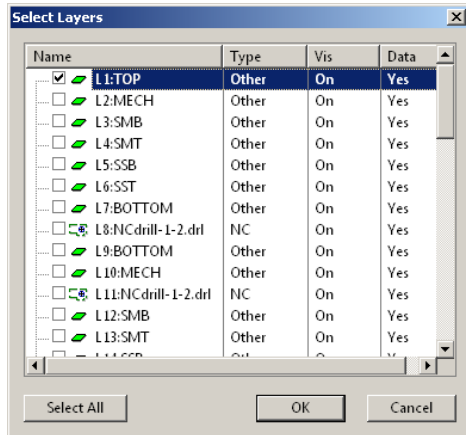
I then select the layers I want to copy L16 to. In this case, just L1:TOP. After pressing *OK*, the copy takes place. Had you done this, you could then go over to the *Colors* panel and observe that L16 did indeed get copied to L1. The last step is to again select L16 and delete it from the *Navigator* panel.

This technique works with any Gerber or drill files, and is the way I typically merge designs that aren't in a suitable *.GTD format already, especially if the layers are out of order…

Be careful that the layers you're moving *do not overalap* any objects already on that layer. In the example above, I loaded the same set of files from the same source, so Gerbtool precisely overlaid them! Since the two PCB's were on different layers (L1 – L8 and L9 – 16 respectively), I moved the first set on L1-L8 to the origin by filtering my window selection in the *Selection Filter* panel. This is a very powerful technique, making Gerbtool quite versatile.

3.2 TILING WITH GERBTOOL

This discussion show how to actually go about doing the tiling. As you will soon see, its very useful to have a copy of the board's outline no thicker than 25mils added to one of the documentation layers, like the ***.Mech** layer; everyone should agree on this. Note that cutting marks or the drill table aren't needed. Thus, keep only the board outline on the Mechanical layer.

You should first have your own board loaded and located with the lower left corner, XY = (0,0), at the origin. To avoid accidentally overwriting your own *.GTD file, save the current session as **"your group name".GTD**, where "your group name" is that indicated on the class website for your particular group; place this in a special folder. Assuming you will be tiling for the largest board APC will run, make the film box 14.000 by 17.000 inches (*Note:* APC now allows up to 14.000 by 17.000 inches; the example shown here was taken from a past cmpe173 class when the maximum allowable board size was smaller, hence the 9.3 x 12.4 limit). Prepare to tile in the first board setting the grid to 25 mils and turn *Snap to grid* on by depressing the **Toggle grid snap** tool. Make only the top and mechanical layers are visible. Note the MECH is assumed to have a 10 to 25 mil thick board outline on it. Assuming your board is 3 x 3 inches, it will look similar to what you see below.
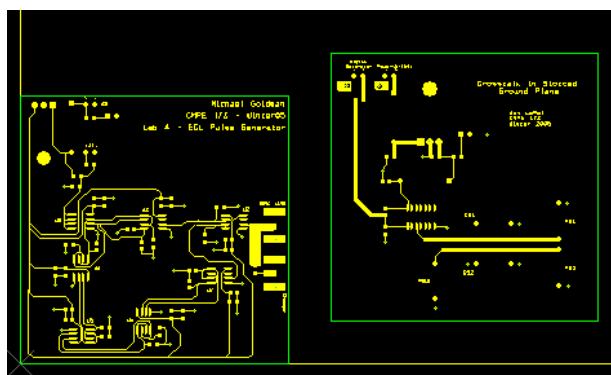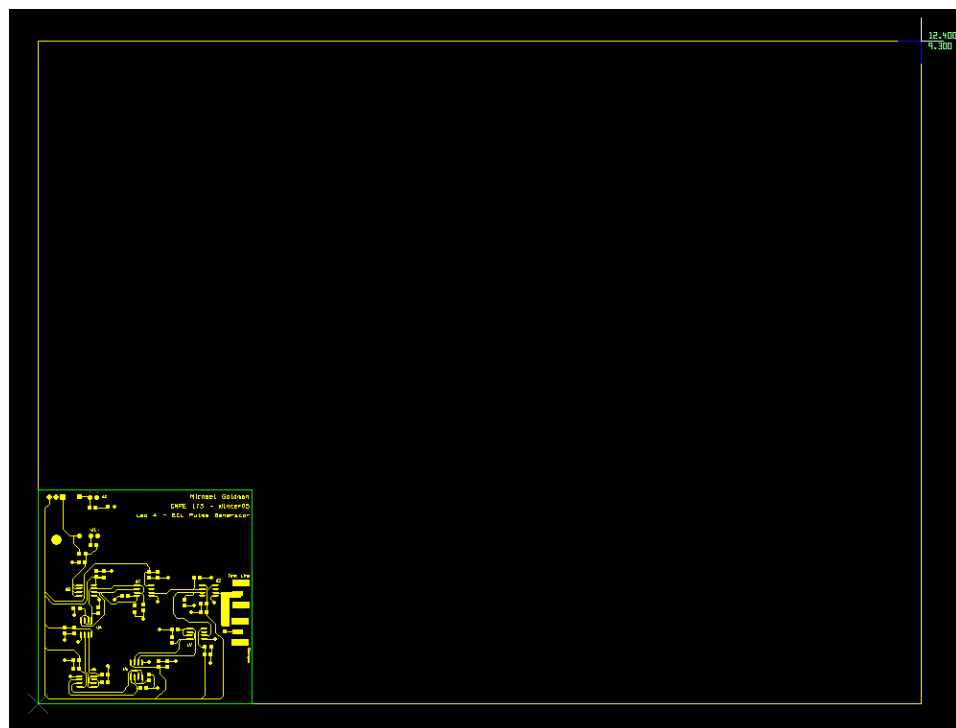
Choose the menu sequence **File → Merge…** and navigate to the *.GTD file you want to tile. GerbTool will load it and show you a white phantom square. The size of this white square has nothing to do with the actual size of the board being merged! Try zooming in and out and you'll see what I mean. You can place the new board anywhere you like (except on top of the current one).   All layers will most likely come on; the example shown has only the top and Fab layers visible.

The position of the new board can now be positioned precisely by selecting all the objects on *all layers* of the new board and moving them to their final position. Hence, first turn on all layers, then select the **Move** tool or choose **Edit → Move…**. Gerbtool will bring up the **Selection Filters (Move)** dialog.

Select all layers on which there are objects you want to move; that would be all them. Since we want to select by drawing rectangles around these objects, select the **Window** mode. After pressing Apply, the window will remain; close it or move it out of the way.
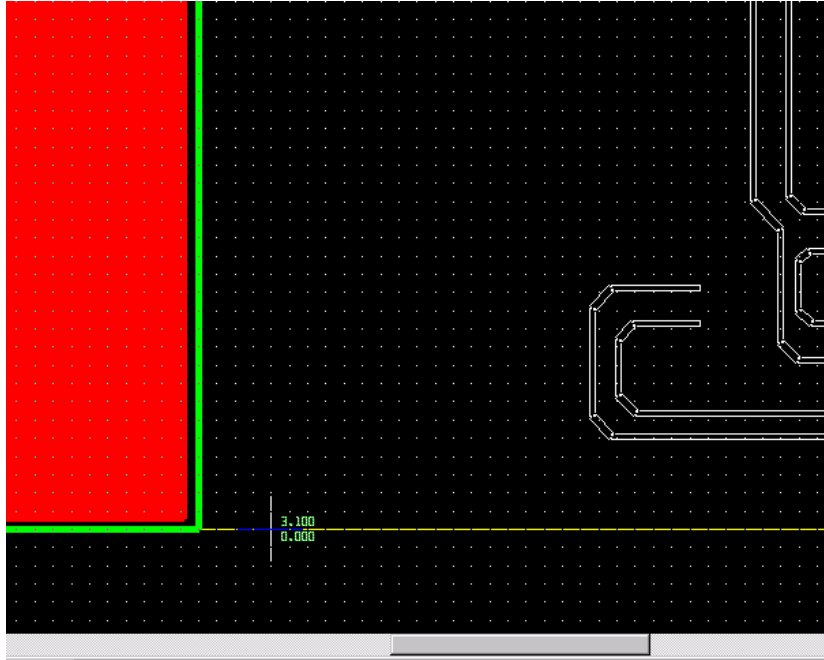
Using the left mouse button, click and drag a rectangle entirely around the new board. Selected objects will all turn white. Zoom in (using the **I hotkey**) at least far enough to see the 25 mil grid points and accurately select the lower-left corner of the board outline. You won't see any change until things begin moving. Zoom out (using the **O hotkey**) and carefully position the new lower-left corner at 100 mils away from the existing board. Anchor it by clicking the left mouse button. You can also use the cursor XY display to position with, as shown, XY=(0.000, 3.100).

The new board's position should appear precisely where you placed it. Zoom out and check the placement. If everthing is correct, then save the file (CTL-S) and proceed to tile the next board.
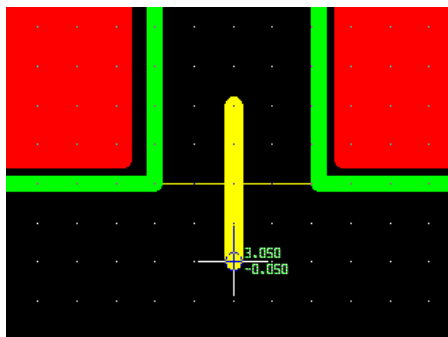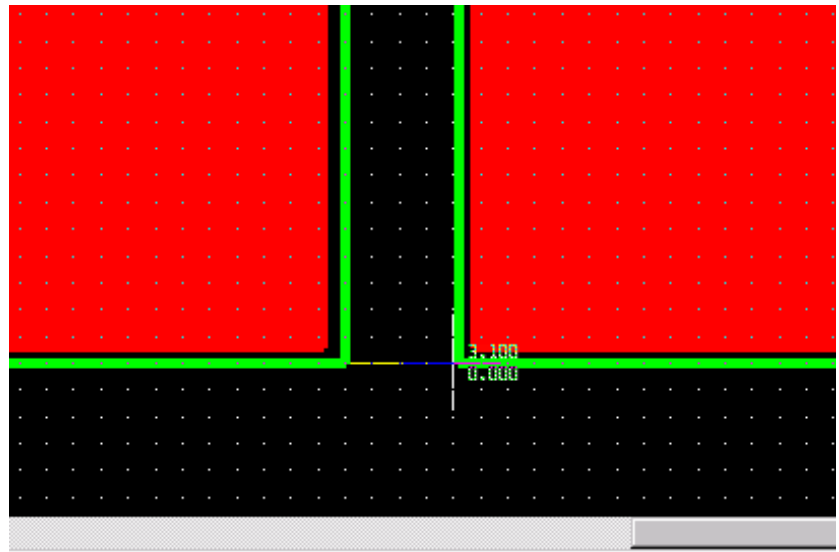
When you're done, cutting marks will need to be placed at the four corners as well as between the tiled boards, so *you* will know where to shear the panels after getting the single finished tiled board back from the boardhouse. Do this by selecting a 10 or 12 mil round D-code from the aperture pull-down list containing all apertures in the design, and activate the **Add Draw** tool. The cursor will change to a circle 10 or 12 mils wide matching the D-code you chose to draw with. Notice that GerbTool states what it expects from us in the lower left corner: "Add Draw: enter first point…". Place marks about 100 mils long between the tiled boards and put them at corners you may to

identify as 90 degree corners 100 mils on each leg.

Shown is a cutting mark created on the top layer using a 12 mil round D-code. Remember to add the board outline on a new mechanical layer as we did in Labl-3.

What is NOT OK, is trying to use D-code *flashes* to draw these copper traces. **Be sure to use ONLY <u>round DRAWS</u>** or the board house will not run your order. If you were preparing a board having solder mask and silk-screen, the silk-screen layer could be used for these marks if you wanted, but placement is usually more accurate when draw as copper traces using draws on the top layer.

HINTS FOR WORKING WITH TILED BOARDS – The drill charts are useless when tiling, since they're relevance applies to only one board. Hence, after merging a particular board for tiling onto the larger board, use the drill chart to check for correct drill sizes and then delete it. This can be done using the **Delete** tool. Select <u>only the DRD layer for safety</u> and choose the **Window** option the same as you did earlier with the Move tool. You can also safely remove objects from any of the other layers (except the top and bottom, obviously!), although its generally best just to make them invisible (except when moving).

An example of what a tiled board looks like for 12 3x3 inch PCB's is shown below. Only the top and bottom layers are visible, as well as the film box. This example does not show the mechanical layer with the board's milling outline, but would be represented by the film box shown. When you do create the board outline on the new *.MCH layer, but sure to offset it so the inner edge is along the actual dimension you want the final tiled board to be. In Lab-3 we simply placed a 10 mil draw on the board's outlined dimension. Here, if you use a 10 mil draw, it should be offset 5 mils so the milling edge is configured to be along the inner resulting rectangle.
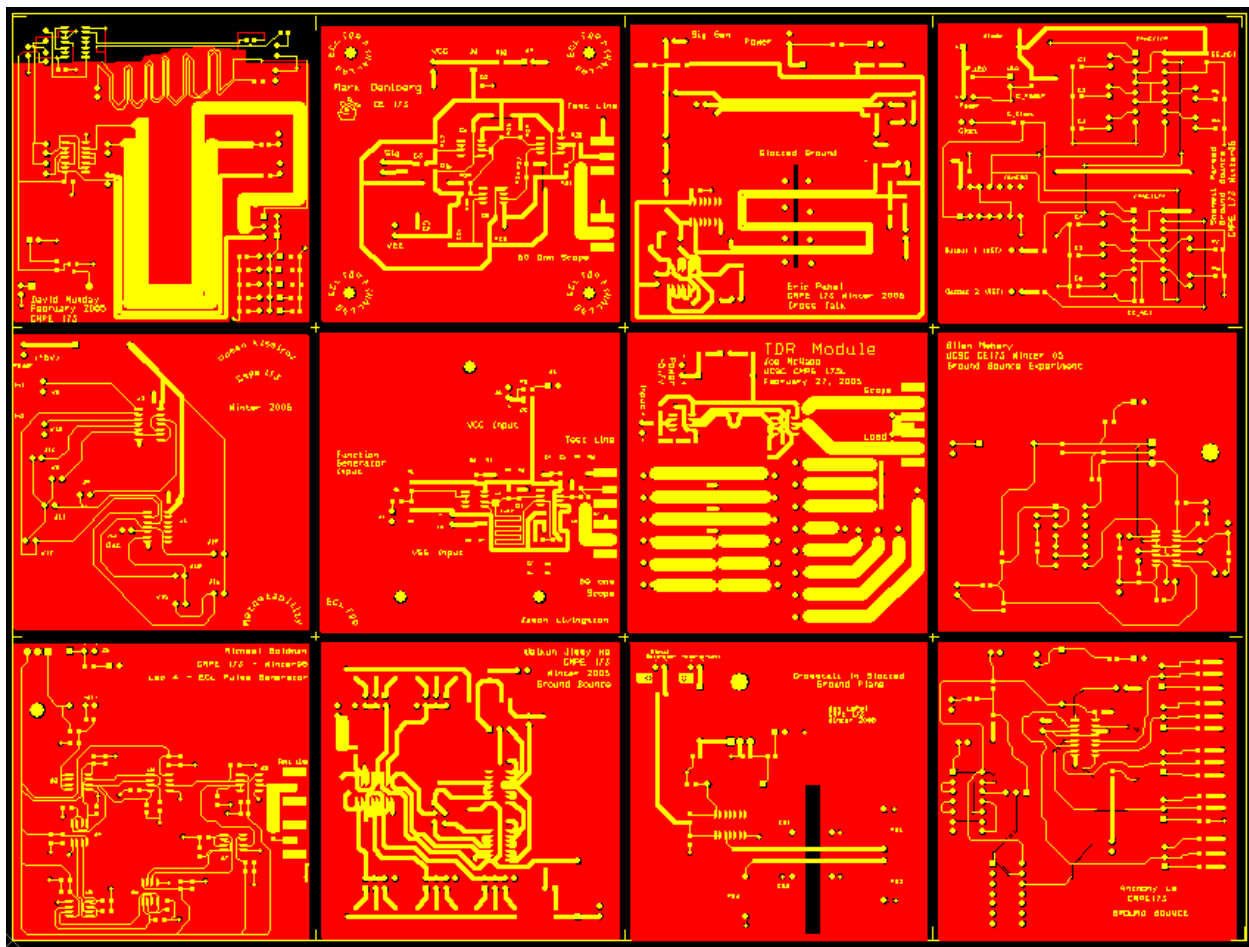
When you're completely done, proceed to convert the ***.GDR** to a new drill layer and export the necessary drill files, Gerber files and aperture file as you did in Lab-3. Have other members of your group double-check things to make sure everything is right.

3.3 SUBMISSION TO APC BOARD HOUSE

After finishing, reviewing and tiling the final set of tiled PCB's in Gerbtool, you should always carefully evaluate exactly what your board house of choice wants for submission. Shown below is a screen dump from APC's website listing required files. From the list it would appear the aperture file is not required. This list implicitly assumes the Gerber files are in RS-274X format.

Prototype Required Documentation

The following files are required for basic board manufacturing:

Description	Data Format	
Required Documents		
Board top side	Gerber	sample
Board bottom side	Gerber	
NC drill file	ASCII	sample
NC Tool list	ASCII	sample
APClient, Online Ordering or use our text based order form	ASCII	sample
Optional Documents		
Mechanical Layer(for cutting)	Gerber	
READ.ME	ASCII	

Although you should already know this, I've included APC's "free" drill rack below for reference. Be sure to check each tiled board for allowable drill sizes.

Prototype Drilling:

Sizes:

AP Circuits is capable of drilling in any number of drill sizes (between drill number 78 (.016") and 1/4 (.250"). However, we can keep our costs down (in terms of setup time) by providing a pre-selected set of drill sizes. Costs we save are then passed on to our customers. For this reason we provide a group of common drill sizes for you to choose from:

Drill Number Set	Drill Size	Finished Size	Approximate Use
#76	.020"	.017"	via holes
#70	.028"	.025"	via holes, fine lead devices such as trim pots etc.
#65	.035"	.032"	IC's, 1/4 watt resistors, small diodes, ripple caps etc.
#62	.038"	.035"	Square posted pins that measure .025" on the flat.
#58	.042"	.039"	TO-220 packages, IDC type square posted headers, 1/2 watt resistors, 1N9000 series diodes, IC chip carriers etc.
#55	.052"	.049"	larger connectors, transformer leads, etc.
#53	.060"	.057"	similar to .052" above
#44	.086"	.083"	TO-220 mounting holes, screw holes, general mounting
1/8 in.	.125"	.122"	mounting holes
#24	.152"	.149"	mounting holes

- We do not stock Metric diameters or off wire size diameters. Please click here for a complete drill list.
- Drill sizes are BEFORE PLATING diameters. Expect after plating hole size to be between 0.003" and 0.005" smaller.
- The common use information above is only a guideline. When placing an order, be sure to calculate the required pre-plate hole sizes using the drilling guidelines

If your project requires drill sizes not outlined above there will be an extra charge for each additional size.

COMPLETED FILES – This will normally include the following specific files for the Basic Prototype run:

1. [project name].TOP   (top copper Gerber file).
2. [project name].BOT   (bottom copper Gerber file).
3. [project name].APP   (master tiled Aperture listing file).
4. [project name].drl   (NC drill file).
5. [project name].rpt   (Drill listing file).
6. Orderform.txt

If you choose to submit these using APC's client, they will automatically be sent via FTP for you. APC gives us a discount if we use their client, so I encourage you to use it instead of the manual method.