ETICD-01 Introduction to IC Design

ETICD Lab#1
Group 3

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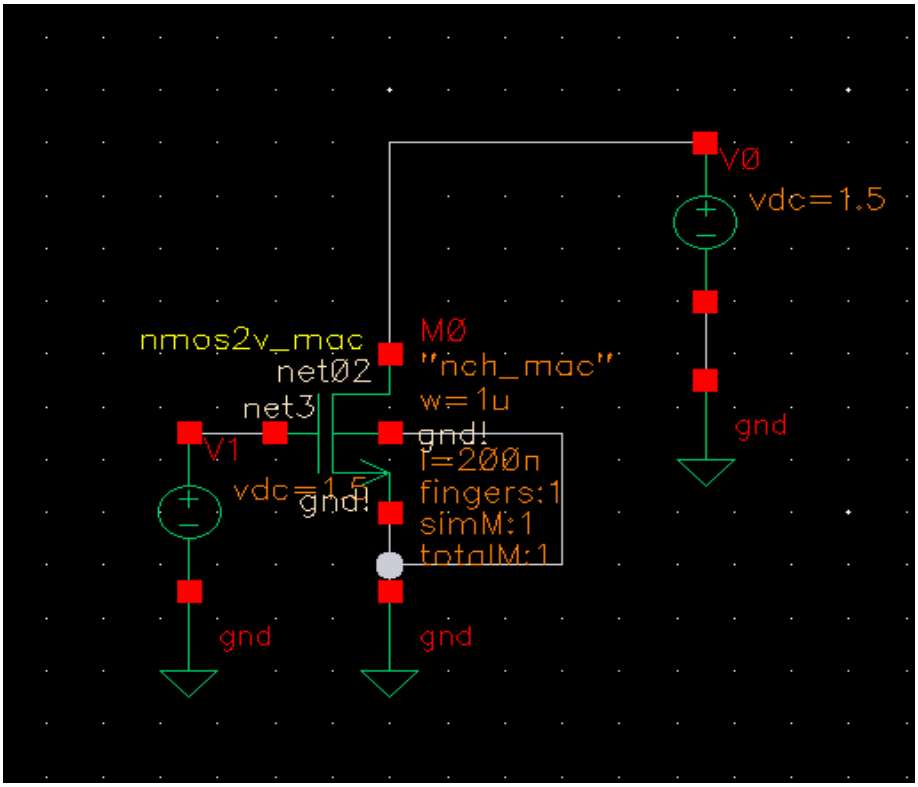
Introduction

This lab consists of using the Cadence software to simulate a PMOS transistor, a NMOS transistor and an inverter. We have been asked to use the simulations to find the different parameters of each transistor and the inverter.

Results

NMOS

The NMOS transistor has to follow the following specifications; W/L=1µm/200nm and Vdd=1.5V. Below is the schematic of the transistor used in our simulations.



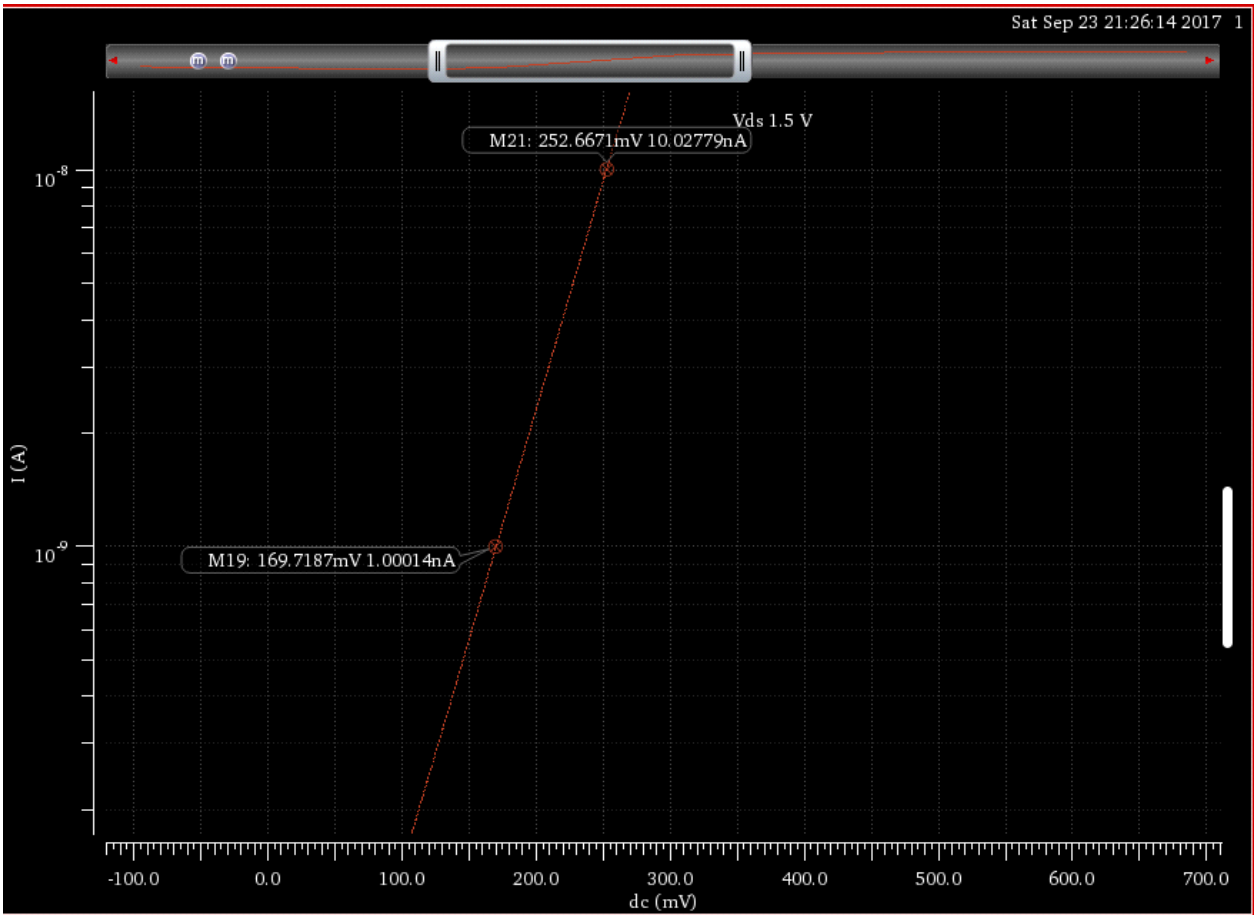
Figur 1 NMOS test bench schematic

Threshold Voltage V_th	0.6 V
Subthreshold swing	85mV/dec
DIBL	17.1mV
Ioff	11.1pA
Channel Length Coefficient	0.118

Table 1 Table for NMOS values found in simulations.

Table 1 shows the values we found in our simulation of a NMOS transistor, the sections after this explain how we found these values and discuss their test bench images.

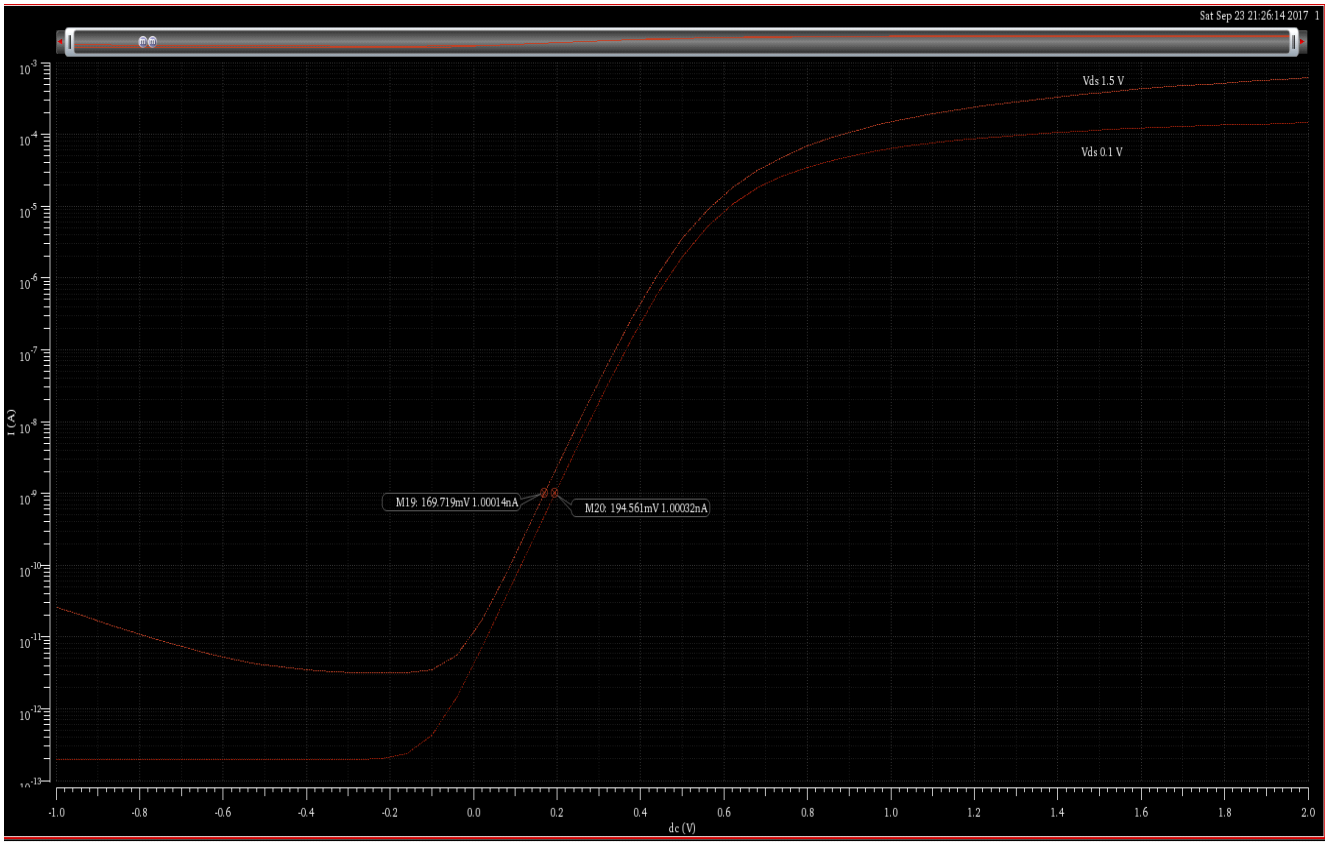
Subthreshold slope



Figur 2 Subthreshold slope of the NMOS transistor

The subthreshold slope is fund be looking at the graph (Figur 2) in the subthreshold region where Vgs < Vth. To find the subthreshold you can measure the voltage difference between two decades. So, for our simulation the subthreshold slope is 252mV-169mV = 83mV/decade. The typical subthreshold at room temperature is around 60mV/decade.

DIBL



Figur 3 DIBL of the NMOS transistor with markers for the two threshold voltages

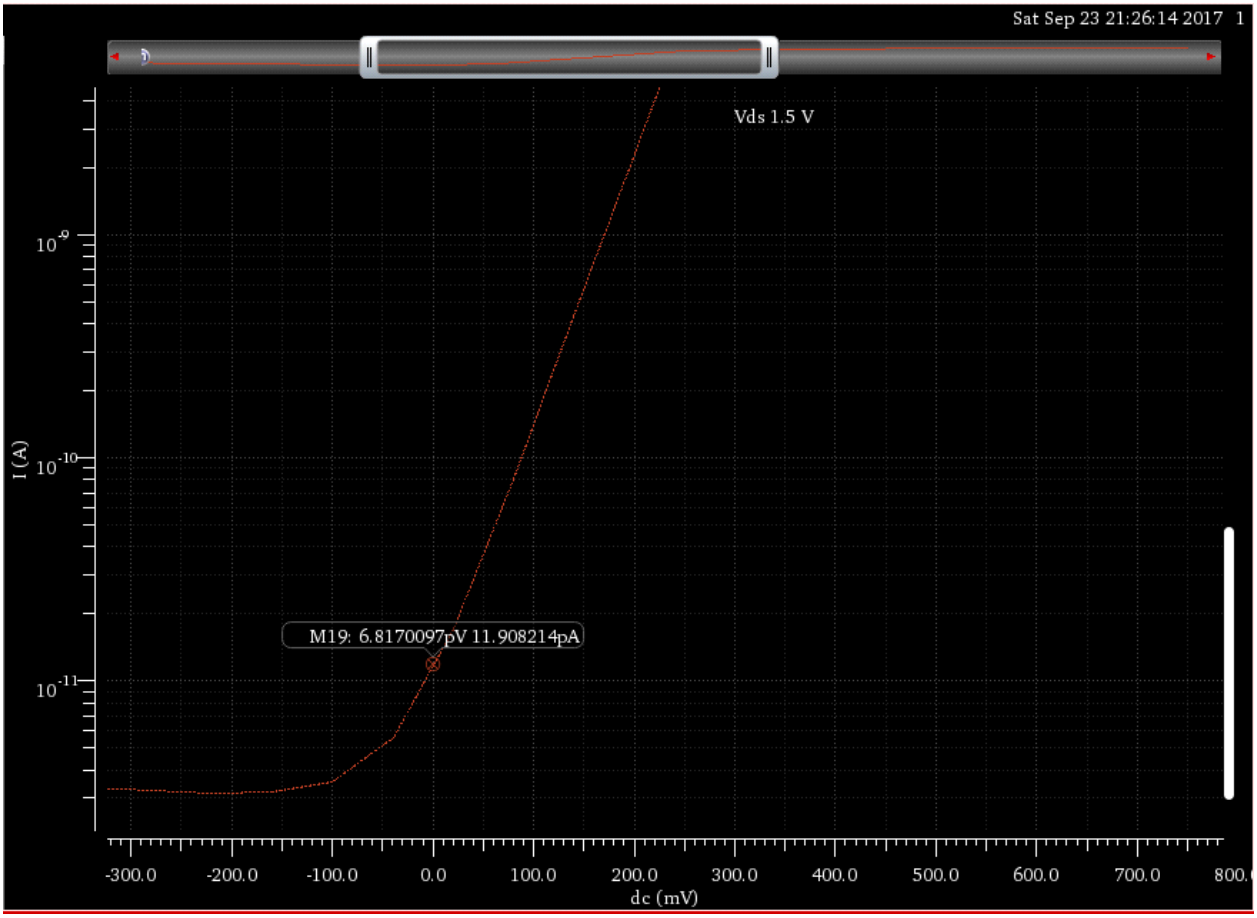
The DIBL (Drain-Induced Barrier Lowering) increases the drain source voltage leaka$ge in transistors with short channels at low Vds voltage. By lowering the Vds voltage on the transistor and plot sweep on the same graph as your normal Vds. You can find the delta Vth and delta Vds and calculate the DIBL effect be this formula $DIBL = \frac{V_{th}^{ds} - V_{th}^{low}}{V_{ds} - V_{low\_ds}}$. For our transistor (see **Fejl! Henvisningskilde ikke fundet.**), the DIBL is

$$DIBL = (194.561mV - 169.719mV)/(1.5V - 0.1V) \quad (1)$$

⇳*Ligningen løses for DIBL vha. CAS-værktøjet WordMat.*

$$DIBL = 17{,}74429 \cdot \frac{mV}{V}$$

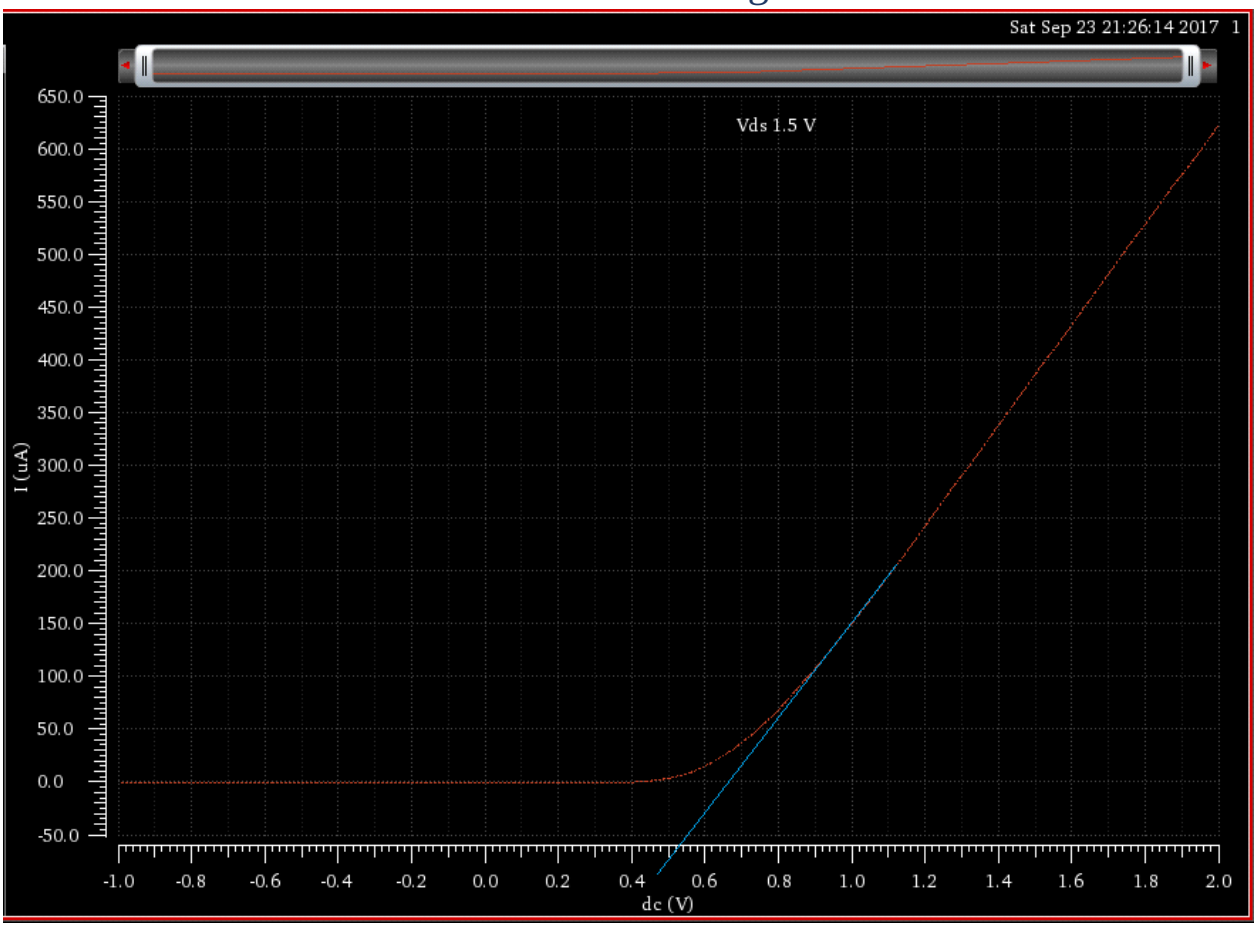
Ioff



Figur 4 Ioff shown on the graph

The Ioff is the current leakage from drain to source when the gate voltage is equal to zero and the NMOS transistor is turned off. As seen in Figur 4 the Ioff for our simulated NMOS transistor is ~12pA.

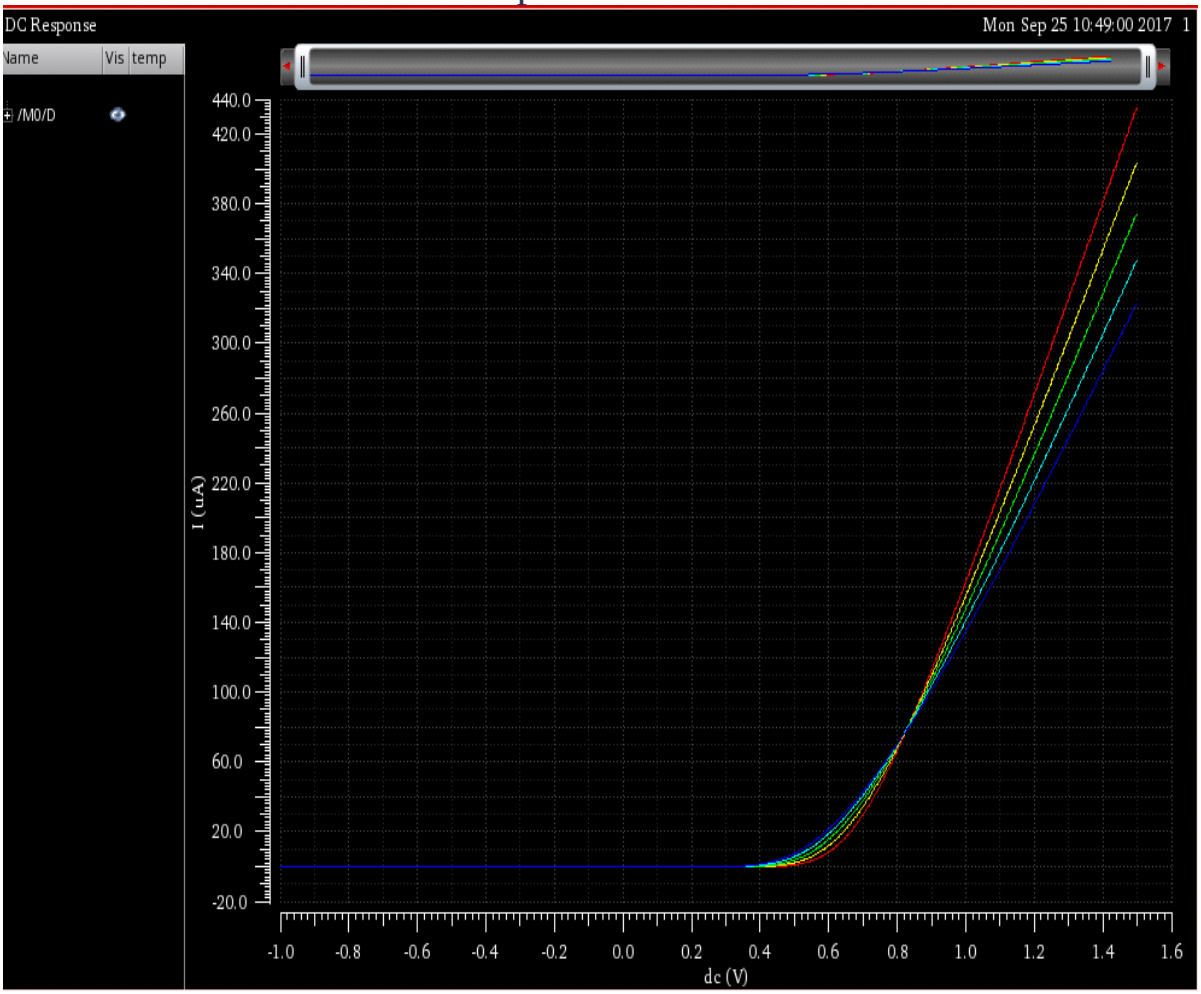
Threshold Voltage



Figur 5 Threshold voltage of the NMOS transistor

To read a transistor threshold voltage from a linear graph. you draw a line from the straight part of the graph as seen on Figur 5. Where the line crosses the x axis you have your threshold voltage. In our case the Vth is ~539mV.

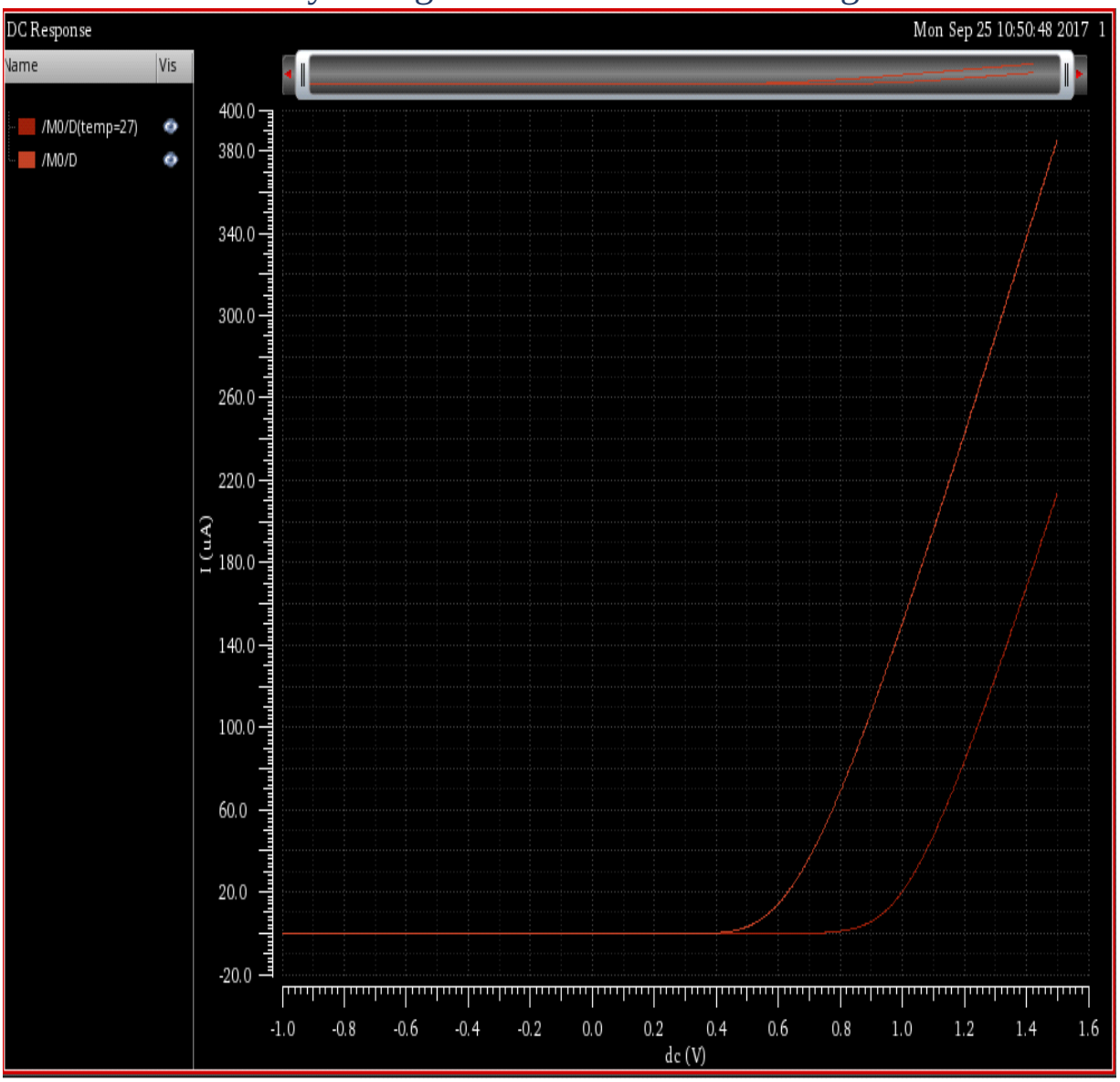
Temperatur effects



Figur 6 Temperature effect on a NMOS transistor shown with 5 graphs between -40 and 125 degrees, blue line is at -40 degrees and the red line is at 125 degrees

In the temperature sweep of the NMOS transistor with Vgs=0. You can see in the graph on Figur 6 that the Ioff increases when the temperature raises. Also we see that the largest effect the temperature has is in the region around Vt, where the spread is the largest between the temperatures before the saturation region.

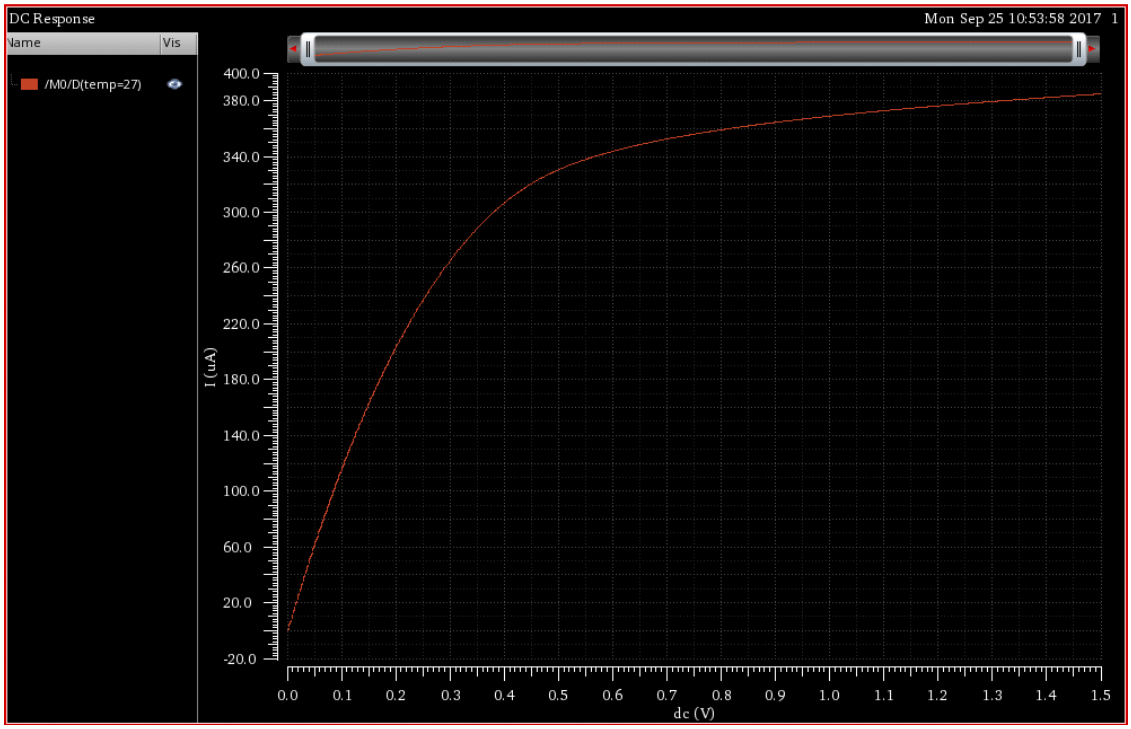
Body voltage effect on threshold voltage



Figur 7 Threshold voltage increased after the Body is connected to Vdc instead of gnd

By increasing the body voltage, we can manipulate the threshold voltage of the transistor. As seen in Figur 7 the threshold voltage is increased to 860mVcompared to the ~560 we had before, when the bulk gate is connected to Vdd instead of gnd.

Channel length modulation coefficient



Figur 8 Graph of the NMOS transistors Ids-Vds characteristics

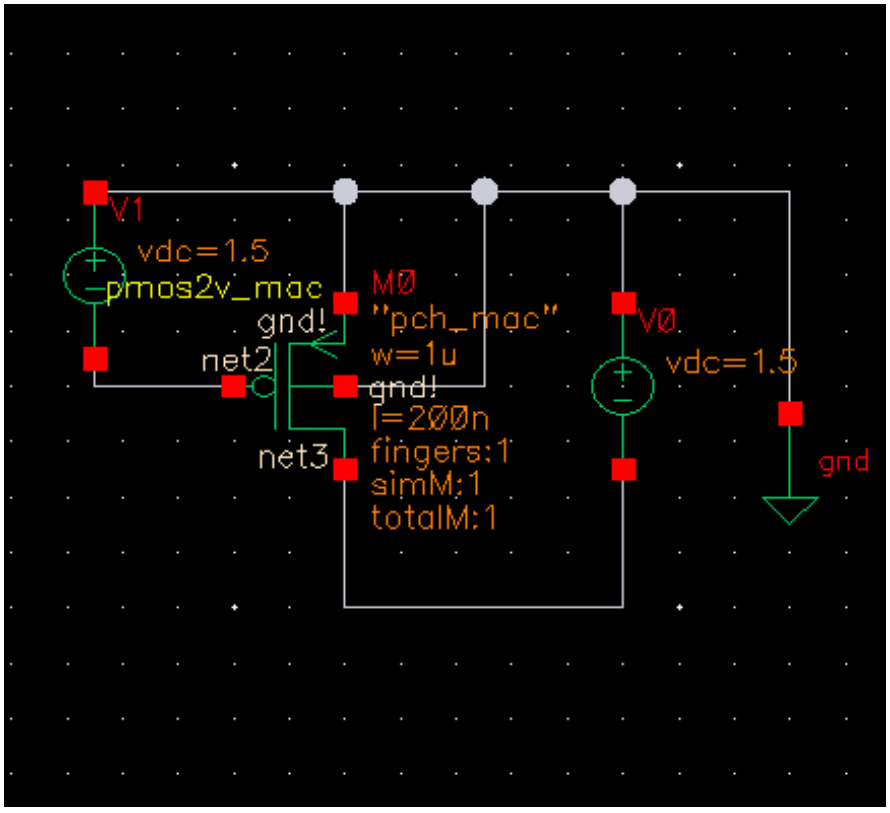
To find the Channel length modulation coefficient we follow the equation I_dsat/R_on, both of these can be found on the graph. I_dsat is the current when the transistor enters the saturation region, read as the current when the voltage is at Vt. R_on is the slope of the linear region after the transistor enters the saturation region. Reading the graph and substituting into our equation we get a Channel length modulation coefficient of: 0.118

PMOS

The PMOS transistor follows the specifications as the NMOS; W/L=1µm/200nm and have a Vdd=1.5V. Below is the schematic of the transistor used in our simulations. For many of the parameters, the same method used for a NMOS transistor applies to the PMOS transistor as well, in these cases we will simply write the final equation or value, while referring to the NMOS section for explanations. Below is a table showing the values we have found, after that are more in-depth explanations and test bench images of these values.

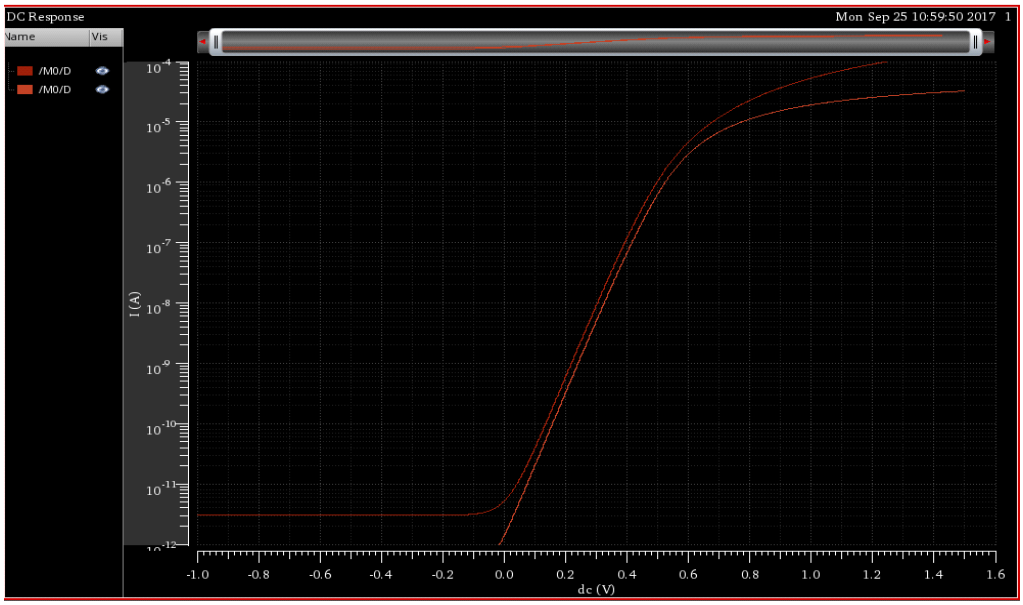
Threshold Voltage V_th	0.49 V
Subthreshold swing	90mV/Dec
DIBL	16.9mV
Ioff	-5.33pA
Channel Length Coefficient	0.218

Table 2 Values found for PMOS through simulations.



Figur 9 Schematic of the PMOS transistor

Subthreshold slope



Figur 10 Subthreshold slope of the PMOS transistor

The subthreshold slope of the PMOS(see NMOS section for definition) is found on figure 10 to be: 90mV/Dec

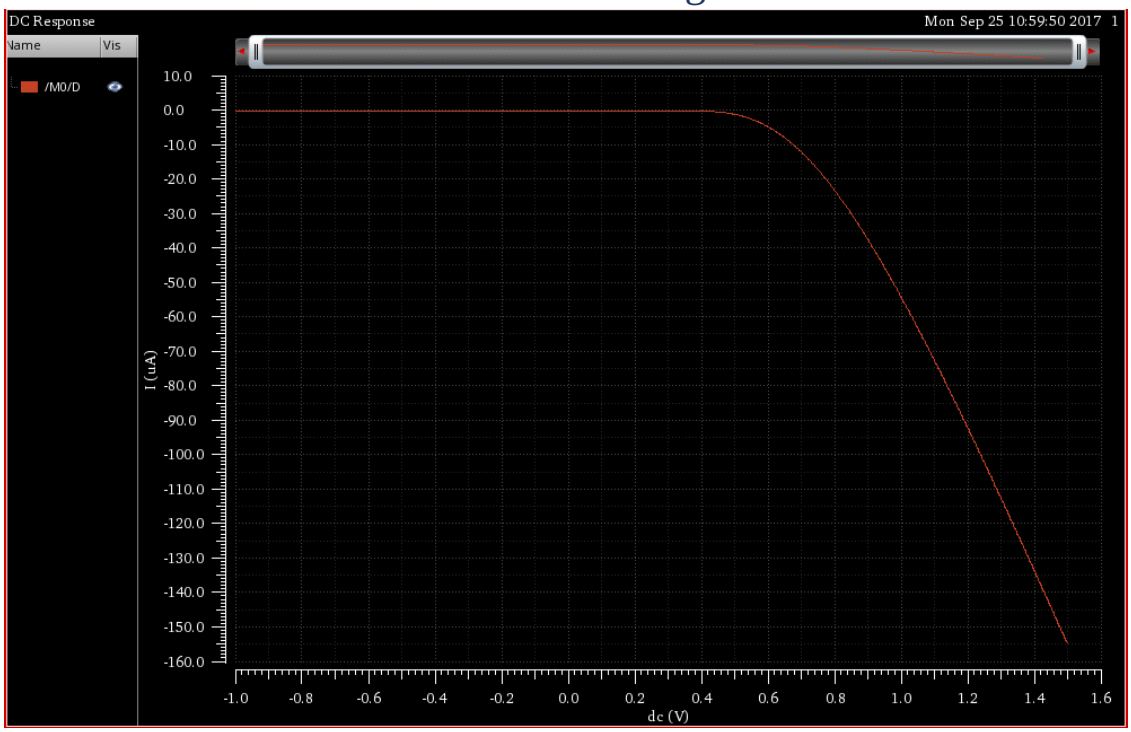
DIBL

The DIBL (Drain-Induced Barrier Lowering) of the (see NMOS section for definition) is found on figure 10 to be: 16.9mV

Ioff

The Ioff current of the (see NMOS section for definition) is found on figure 10 to be: -5.33pA

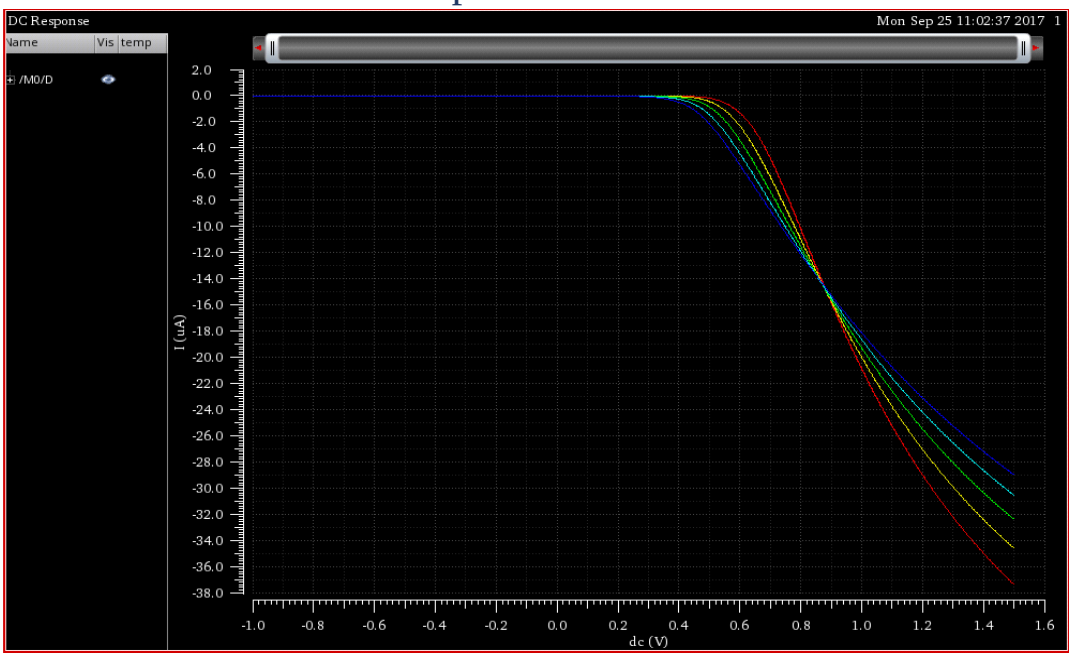
Threshold Voltage



Figur 11 Threshold voltage of the PMOS transistor

Reading the threshold voltage is a bit different for the PMOS graph, here you need to find the point the graph enters the saturation region, or more specific where the graph becomes linear and read the voltage value at this point. The threshold voltage value is: 0.49 V

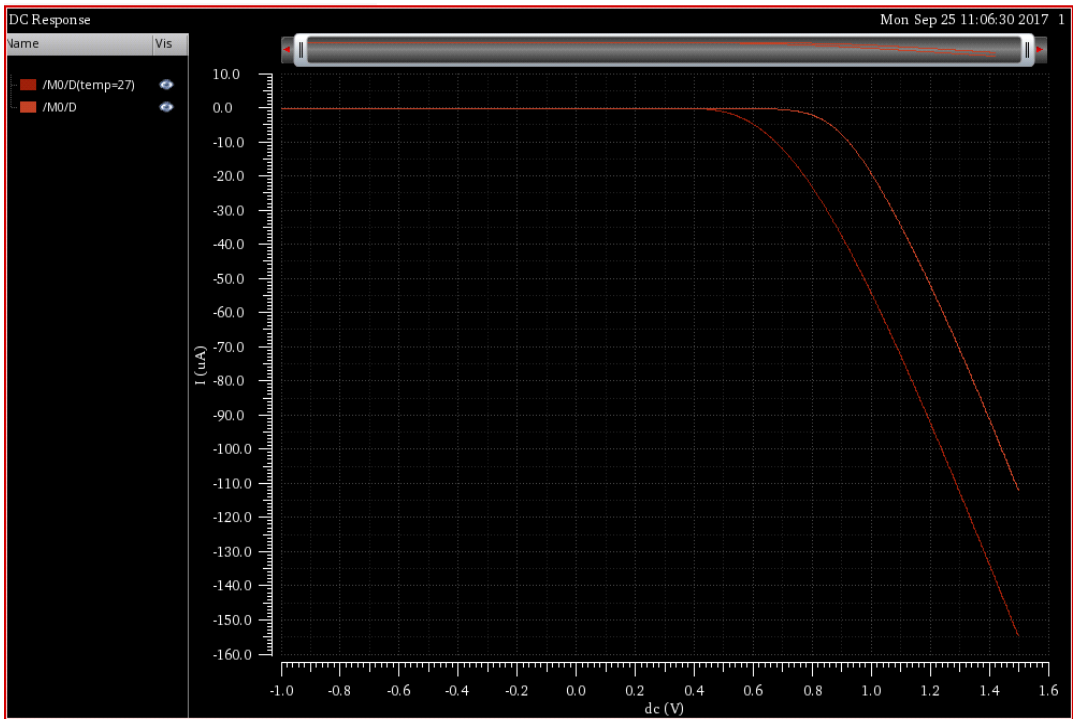
Temperatur effects



Figur 12 Temperature effect on a PMOS transistor shown with 5 graphs between -40 and 125 degrees, blue line is at -40 degrees and the red line is at 125 degrees

Again this graph looks different from the NMOS graph, however it shows the same effect and tendencies in increasing the spread around Vt after changing the temperature.

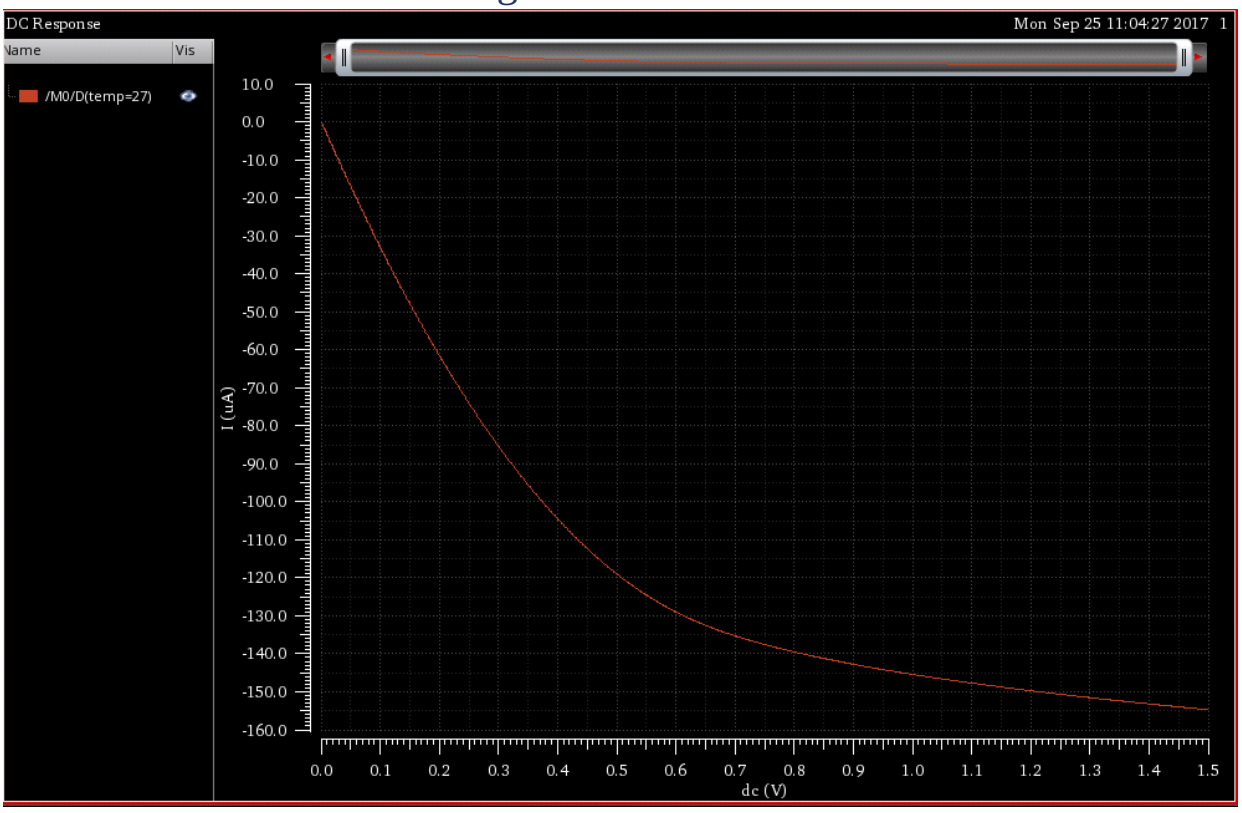
Body voltage effect on threshold voltage



Figur 13 Threshold voltage increased after the Body is connected to Vdd instead of gnd

By increasing the body voltage, we can manipulate the threshold voltage of the transistor. As seen in Figur 13 the threshold voltage is increased to 800mVcompared to the ~560 we had before, when the bulk gate is connected to Vdd instead of gnd.

Channel length modulation coefficient

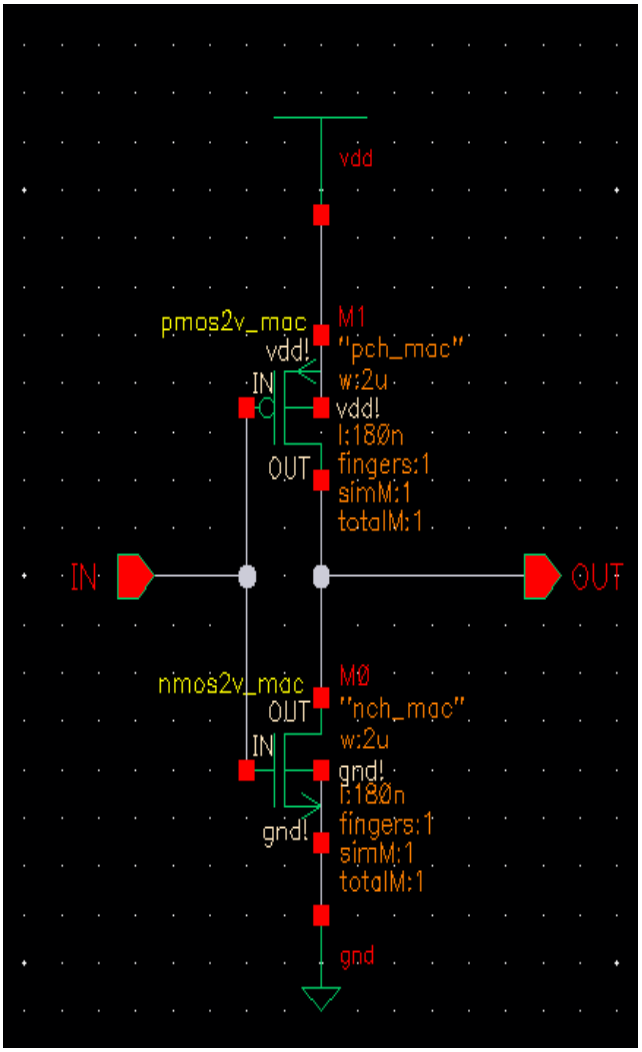


Figur 14 Graph of the PMOS transistors Ids-Vds characteristics

To find the Channel length modulation coefficient we follow the equation I_dsat/R_on, both of these can be found on the graph. I_dsat is the current when the transistor enters the saturation region, read as the current when the voltage is at Vt. R_on is the slope of the linear region after the transistor enters the saturation region. Reading the graph and substituting into our equation we get a Channel length modulation coefficient of: 0.218

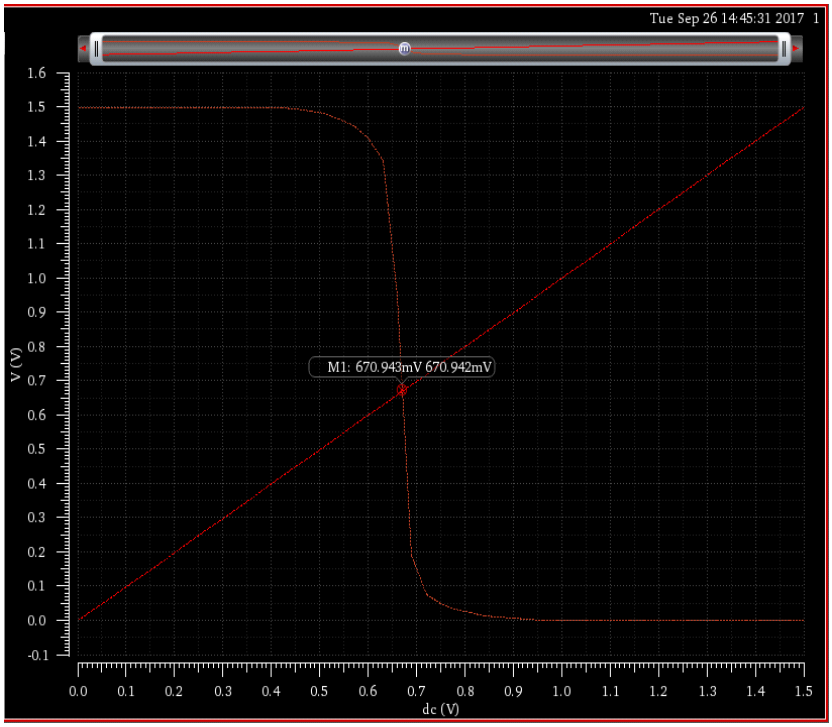
Inverter

The last part of our assignment is simulating a dc-sweep over an inverter. We have used the following schematic for our inverter

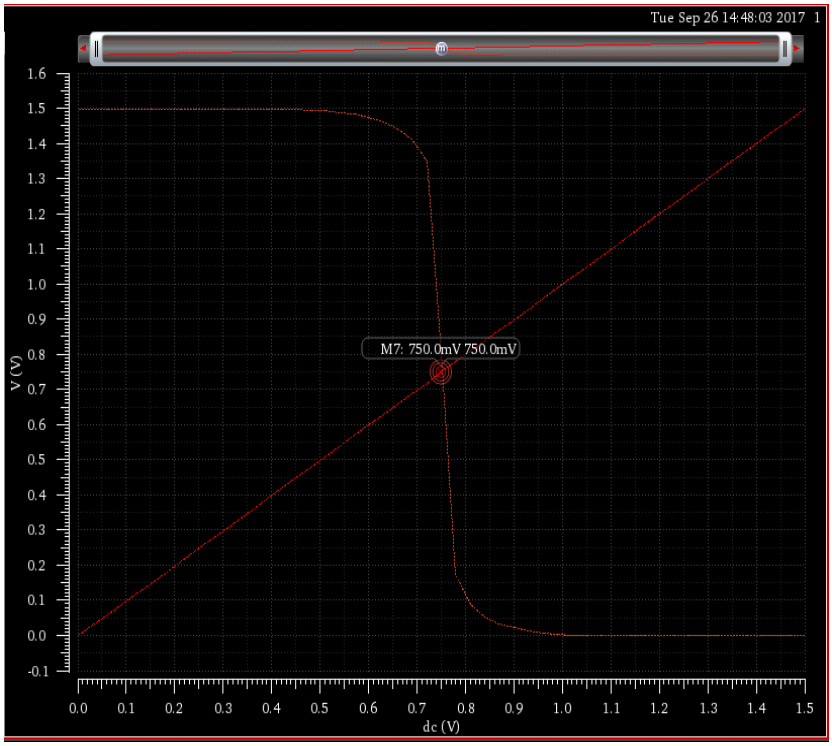


Figur 15 Schematic of inverter in Virtuoso

Sizing the transistors



Figur 16 graph of V(in)/V(out) for inverter without sizing (1 to 1 ratio for transistor width)



Figur 17 graph of V(in)/V(out) for inverter with sizing (1 to 3 ratio of transistor width)

First we have to size the transistors to get the best noise-margin. In order to get the best noise margin, we need to have V_IH and V_IL (see figure 18) to be closer to each other. We can see that after resizing the transistors that our graph tends towards this ideal.

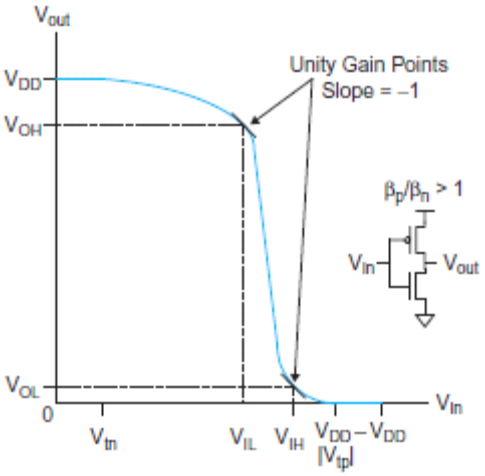
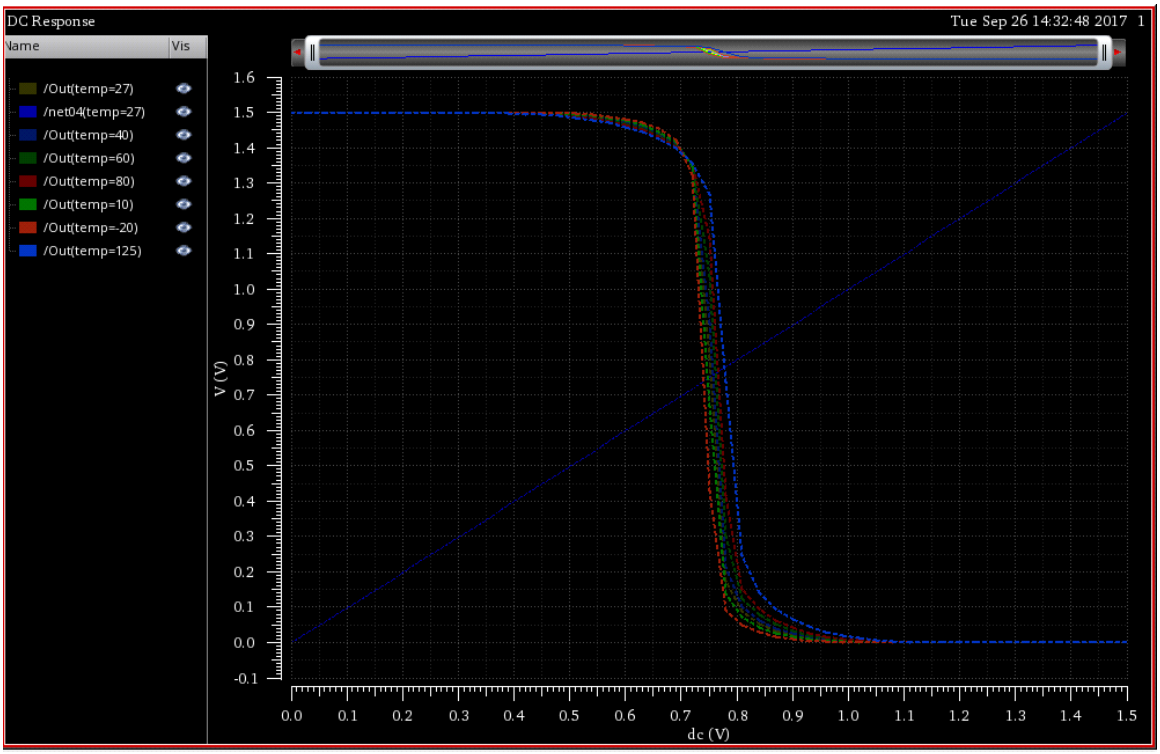


FIGURE 2.30 CMOS inverter noise margins

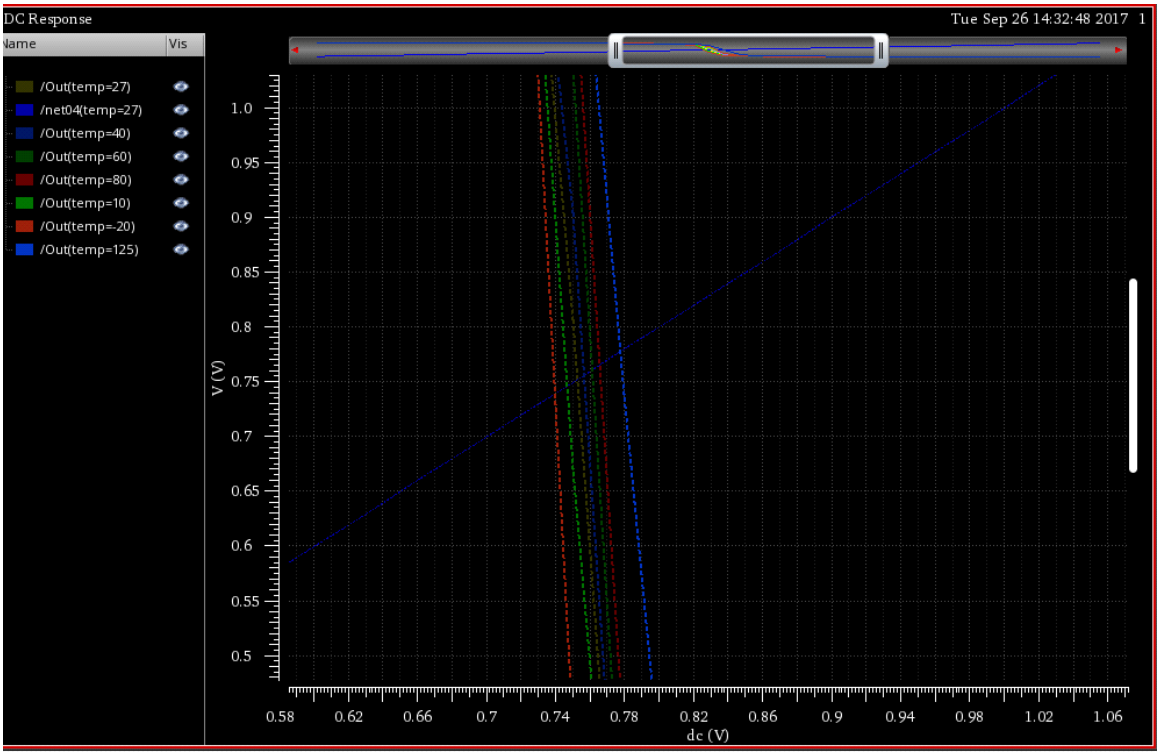
Figur 17 graph of V(in)/V(out) for CMOS taken from "CMOS VLSI design, page 92)

Temperature effect on dc-values of inverter



Figur 18 graph of V(in)/V(out) for inverter range of temperatures

In figur 18 we can see that as the temperature rises the point where the input crosses the output at vdd/2 is moved, this is better seen in figur 19 where we have zoomed in on the region around this point



Figur 19 zoom in of figur 19 around the VDD/2 point (dark blue line is 27 degrees)

In figur 19 we can more clearly see that the temperature swings depending on the temperature. The most noticeable difference is that the noise margin changes with the temperature.