ETICD-01 Introduction to IC Design

ETICD Hand-in assignment #1

Group 3

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1. Design the function F(A,B,C,D) using complementary CMOS logic and size the transistors. Re-design the function using pseudo-nMOS and explain the advantages and disadvantages of pseudo-nMOS compared to Complementary CMOS.

$$F(A,B,C,D) = ABD + \overline{B} + \overline{C}D$$

First the truth table and Karnaugh map have been worked out for function $F(A,B,C,D)$

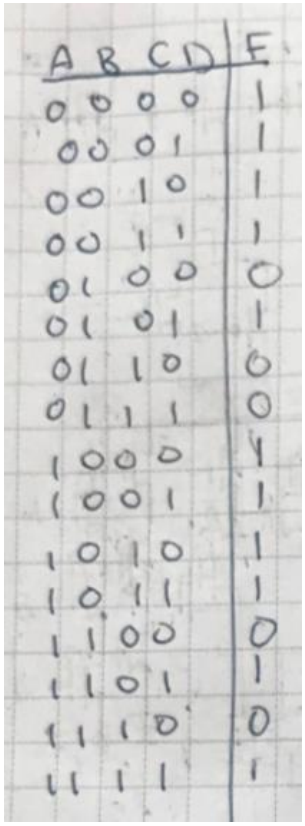


Figure 1 Truth table for F(A,B,C,D)

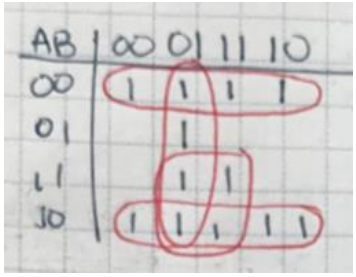


Figure 2 SOP Karnaugh map for F(A,B,C,D)

The SOP expression for the circuit is discovered to be $F = AD + \bar{C}D + \bar{B}$. This expression only reveals half of the complementary CMOS circuit; the nMOS half.
To reveal the pMOS half of the circuit the expression needs to be converted to POS:

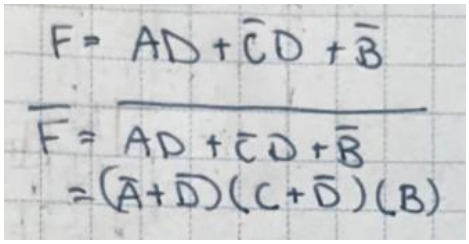


Figure 3 Conversion from SOP to POS of the term F

Now that both the pMOS and the nMOS side of the complementary CMOS design I known, it can be drawn:

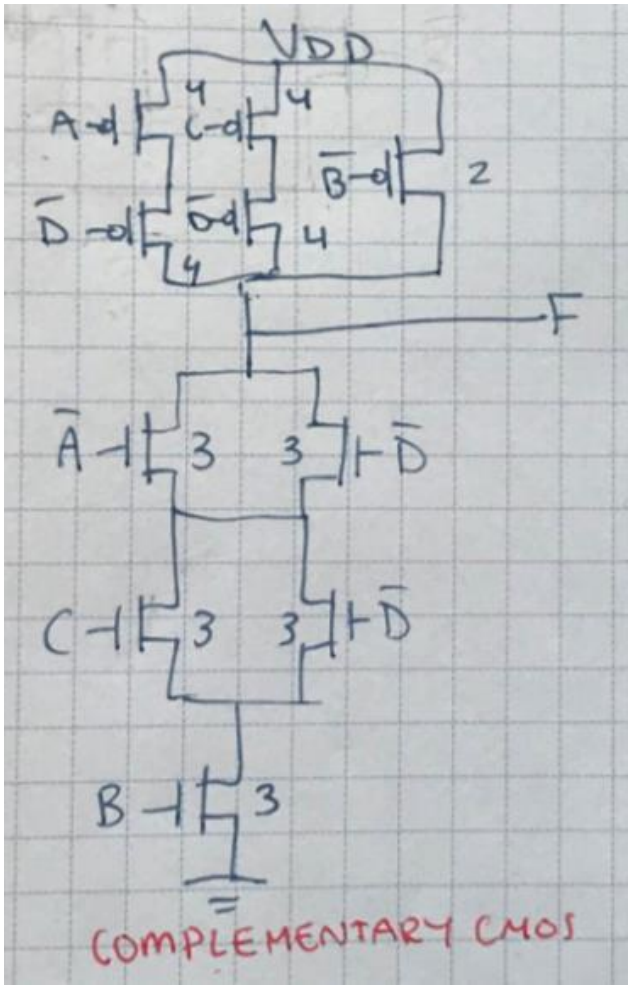


Figure 4 Complementary CMOS design of F(A,B,C,D)

The Complementary CMOS design is now reduced to a pseudo-nMOS by replacing the pMOS section with a single pMOS tied to gound.

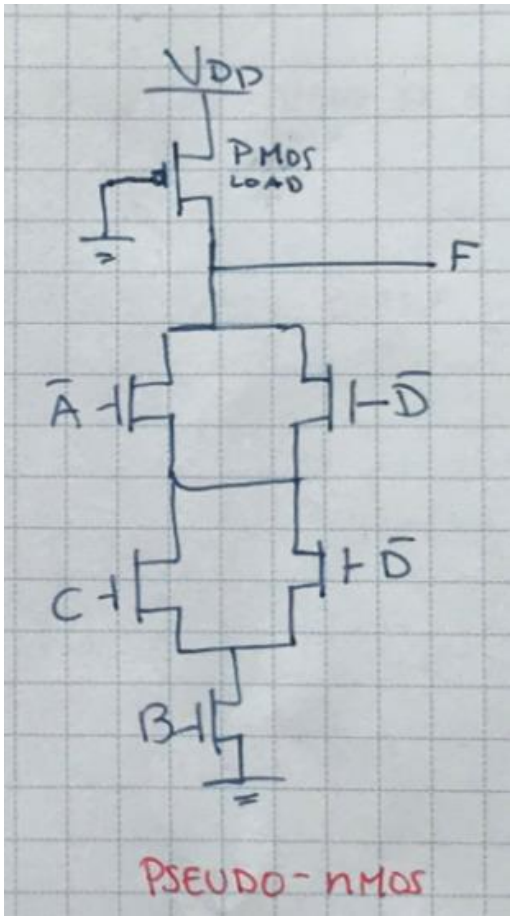


Figure 5 pseudo-nMOS design of F(A,B,C,D)

By replacing the complimentary CMOS with a pseudo-nMOS design, both some advantages and disadvantages follows:

Advantages of pseudo-nMOS

- Ability to control the speed of the system by sizing the pMOS
- Fewer transistors = smaller area
- Smaller load because of smaller parasitic capacitance
- Reduced noise margins

Disadvantages of pseudo-nMOS

- Static power dissipation

2. Implement the following function using dynamic logic:

$$F(A,B,C,D) = \overline{D} + \overline{B} + \overline{C}D$$

What are the main issues with the dynamic logic implementation? Explain how do you solve these issues for your designed circuit?

Implementation of function $F(A,B,C,D)$ is as follows

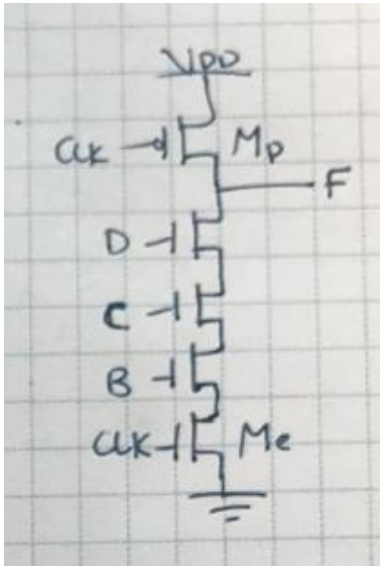


Figure 6 Implementation of F(A,B,C,D)

By implementing the function this way, the circuit will have a charge leakage. When the nMOS transistor is off there will be a leakage current running from the source to the drain. Furthermore the circuit will have an issue with power dissipation, which is usually higher than static CMOS.

To solve these issues a keeper circuit is added on the output F. This helps keeping the output high when the circuit is in evaluation. Sizing of the transistors is important when using a keeper circuit so the nMOS transistor can pull the circuit down.

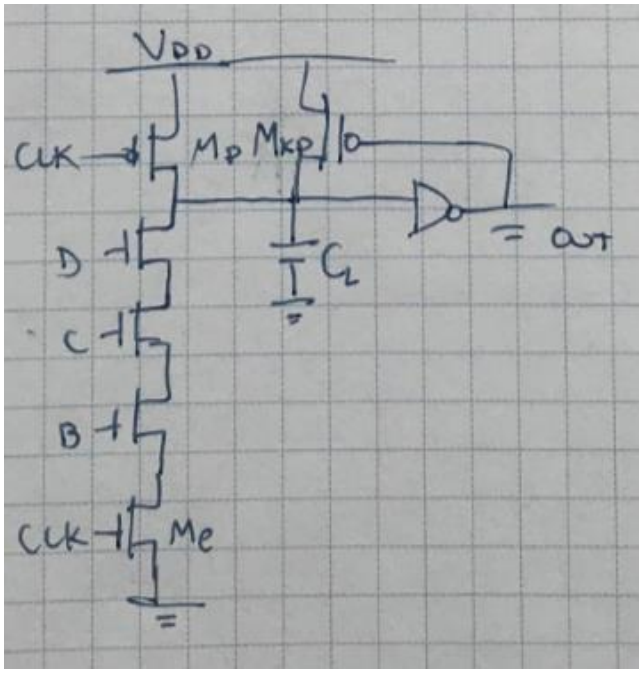
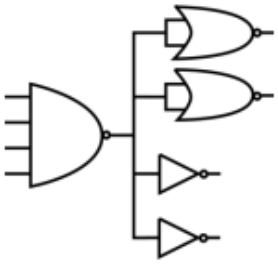


Figure 7 Implementation of function F(A,B,C,D) with a keeper circuit added on the output

3. Find the delay of a 4-input NAND gate connected to a Fan-out=4 of two 2-input NOR gates with connected inputs and two inverters (hint: draw the schematic of 4-input NAND gate, size it, and connect its output to two 2-input NOR gates and two inverters in parallel).



By using the formulas for logical effect $g = \frac{C_{in}}{3C}$, electrical effect $h = \frac{C_{out}}{C_{in}}$, delay $d = gh + p$, and absolute delay $d_{abs} = d \cdot 3RC$ with a table lookup for parasitic delay p, the delay of the of the 4-input NAND gate can be determined.

Before the delay is determined the schematic is sized:

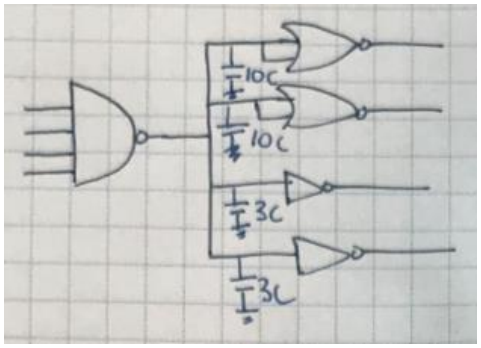


Figure 8 Sized schematic of the circuit

Now the delay of the 4-input NAND gate is determined.
Logical effort:

$$g = \frac{C_{in}}{3C}$$
$$g = \frac{6C}{3C}$$
$$g = 2$$

Electrical effort:

$$h = \frac{C_{out}}{C_{in}}$$
$$h = \frac{26C}{6C}$$
$$h = \frac{26}{6}$$

Parasitic delay:
The parasitic delay for a 4-input NAND gate is

$$p = 4$$

Delay:

$$d = gh + p$$
$$d = 2 \cdot \frac{26}{6} + 4$$
$$d = \frac{38}{3}$$

Absolute delay:

$$d_{abs} = d \cdot 3RC$$
$$d_{abs} = \frac{38}{3} \cdot 3RC$$
$$d_{abs} = 38RC$$

The delay of the 4-input NAND gate is therefore $38RC$.

4. Explain the body effect and show how body-biasing can affect the speed of a circuit (Optional: You can validate your explanation using simulation in Cadence).

The Body effect of a transistor, is created when a voltage is appplied between the source and body, making a fourth terminal, this effect is mainly based on the size of the transistor. This fourth terminal increases the charge reguired to shift the channel, thereby increasing the threshold voltage(V_{th}).

An additional effect that increasing V_{th} has is determining a transistors pass characteristics. nMOS transistors pass 1's poorly, making the voltage level off the 1 V_{dd}- V_{th} this fall in voltage can potentially violate the noise margins off the transistor especially in circuits with low voltage. For pMOS transistors it has the opposite effect making them pass 0's poorly.

How can body biasing affect the speed of a circuit?

To answer this we take a standard pseudo-nMOS circuit.

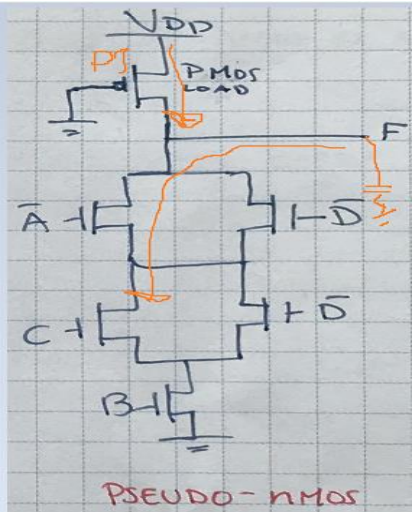


Figure 9 Standard Pseudo-nMOS

As we can see in the circuit the nMOS area is open, and the circuit is trying to discharge the load. However the PMOS transistor P1 is always on and therefore always trying to charge the load. Whether we are discharging or charging is therefore determined by which current is stronger. Therefore the circuit must be made so that the nMOS's have a stronger current, to discharge, but even if this is the case, the size and therefore amount of current P1 can draw, will affect the speed that the nMOS transistors can discharge the load. So often this pMOS must be smaller so that the performance of the circuit is maintained.