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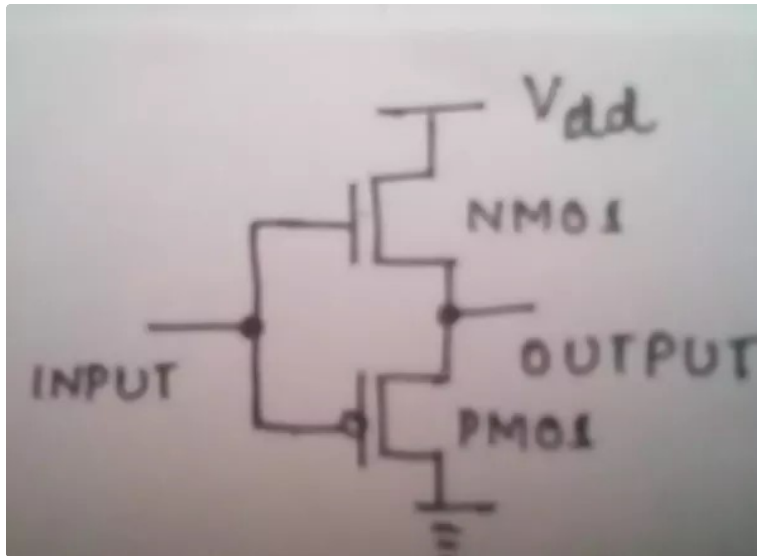# Why do we always use PMOS as a pull up and NMOS as a pull down?

3 Answers

Sowmya Bhat, Assistant Professor
Answered Oct 25 2017

Consider an example shown below:

Here pull up is nMOS transistor and pull down is pMOS transistor.When logic 1 is applied as input, nMOS transistor turns ON and PMOS transistor turns OFF. Hence, the output should get charged to Vdd. But due to threshold voltage effect, nMOS is not capable of passing Vdd/ good logical 1 at the output. Hence, the output will be Vdd-Vth.When logic 0 is applied as input, nMOS transistor turns OFF and PMOS transistor turns ON. Hence, the output should get discharged to ground level. But due to threshold voltage effect, pMOS is not capable of passing good logical 0 at the output. Hence, the output will be 0-|Vth|. Suppose, we need to design buffer, we cannot use the above circuit, rather, we need to cascade two CMOS inverter itself which has pMOS transistor at its pull up and nMOS transistor at its pull down.

Thus, in order to obtain good logic 0 and logic 1 output, always pull up devices are PMOS and pull down devices are NMOS.

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Borna Obradovic, Ph. D. Electrical Engineering & Computer Simulation, The University of Texas at Austin (1999)
Answered Jul 20 2017

A normally-off NMOS (i.e. Vt >0) can't pull all the way up to VDD (VDD being the supply voltage), much like a normally-off (Vt<0) PMOS can't pull all the way down to GND. You can see this as follows:

1. Consider an NMOS with the drain at VDD, and the gate connected to the input signal also at VDD. We're trying to pull the source of the NMOS "high". The node at the source of the NMOS is denoted as 'x' (just a name).

2. The voltage at node x (i.e. V(x)) gets pulled up to the point where Vgs on the NMOS is approximately equal to the Vt (threshold voltage) of the device. At that point, Vgs=Vt=VDD-V(x) (since the gate is at VDD), or V(x)=VDD-Vt. Once this condition is reached, the NMOS is in a very weakly conducting state (near threshold).

3. As Vgs=Vt (from step (2)), the current flowing through the NMOS is small. As V(x) continues to (slowly) increase, the NMOS is rapidly shutting off (now Vgs<Vt, and the transistor is in sub-threshold). So, roughly speaking, for V(x)>VDD-Vt the NMOS is no longer conductive and no longer pulls up the voltage at node x.

4. From (3), we argue that the most an NMOS can pull up to is approximately VDD-Vt.

5. Pulling down to GND is not a problem with the NMOS. Consider an NMOS with a drain at node x (pulling down node x), source at GND, gate at VDD.

6. Vgs-Vt=VDD-Vt, constant during the pull-down. So the NMOS stays on during the entire pull down, even as V(x)→0.

7. The above arguments can be reversed for a PMOS, so a PMOS can pull up to VDD, but only pull down to GND-Vt (and Vt<0).

Hope that help.

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Jeff Gruszynski, My EE focus is analog IC design and semiconductor device modeling
Answered Jul 20 2017

Because it works correctly that way.

There was a time when you used an enhancement-NMOS (like the NMOS in CMOS today) but then used a depletion-NMOS for the pull-up. The first 8080/8286 processors used this type of "depletion-load NMOS".

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