1

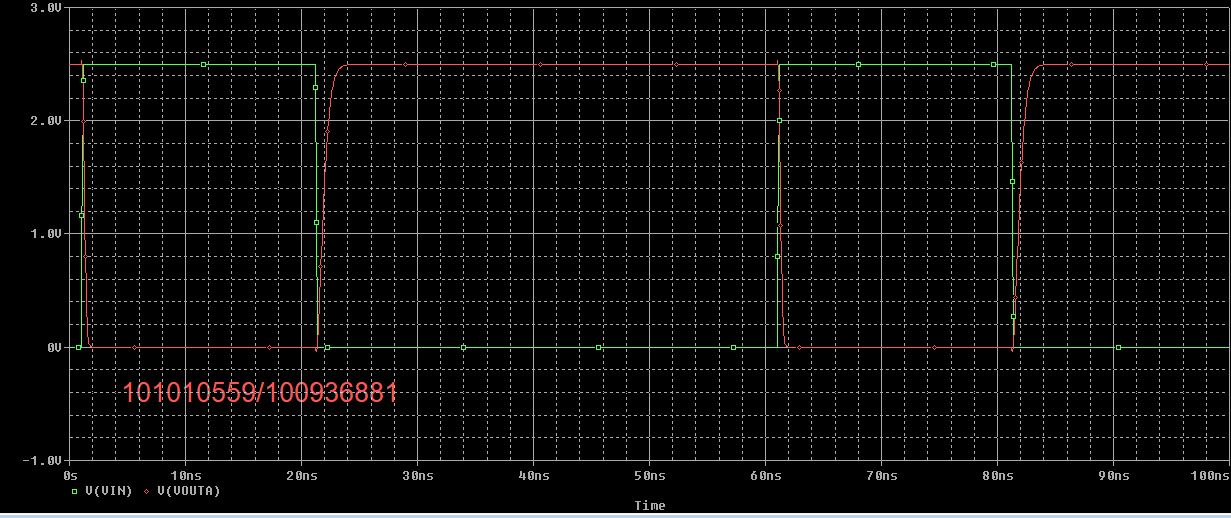
Q1. A) Will work – the NMOS pulls down well and the PMOS pulls up well (invertor).

B) Will work with poor output swing – poor output ranges as the NMOS is in pull up configuration and the PMOS is in pull down (doesn’t invert).

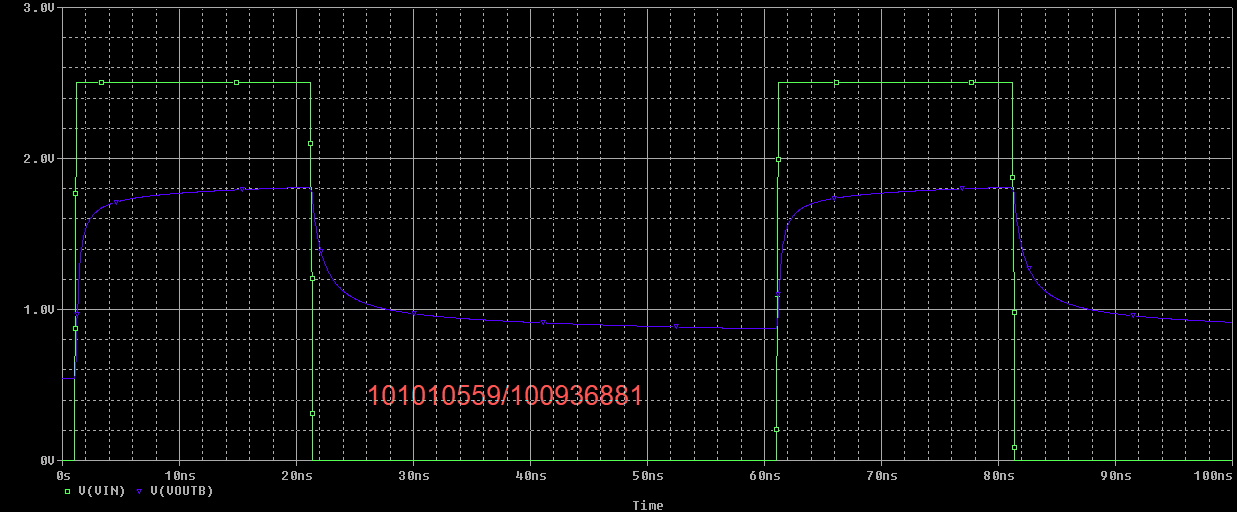
C) Won’t work – both PMOS will either be on (short circuit) or off (output is unknown).

D) Won’t work – both NMOS will either be on (short circuit) or off (output is unknown).

Q2. Circuit (A) is a proper inverter and in this configuration PMOS can pull all the way to Vdd and the NMOS can pull all the way to ground for good output voltages.



Circuit (B) does not work as an inverter and in this configuration, the NMOS cannot pull all the way up to Vdd and the PMOS cannot pull all the way to ground.



Q3. Rising time (10% - 90% swing): t(2.2583) – t(0.253853) = 22.655 ns – 21.486 ns = 1168.6 ps

Falling time (90% - 10% swing): 61.506 ns – 61.171 ns = 335.006 ps

Rising delay (50% input swing to 50% output): 21.906 ns – 21.300 ns = 606.207 ps

Falling delay: 61.305 ns – 61.100 ns = 204.941 ps

Q4. The delay in the PMOS is larger since the size of the PMOS transistor is the same as the NMOS transistor. It is about 3 times larger due to the mobility of holes being slower through the transistor.

Q5. Try w = 3 u for the PMOS.

Rising Time: 407.248 ps

Falling Time: 334.958 ps

Rising Delay: 245.748 ps

Falling Delay: 223.800 ps

Try w = 3.6 u for the PMOS.

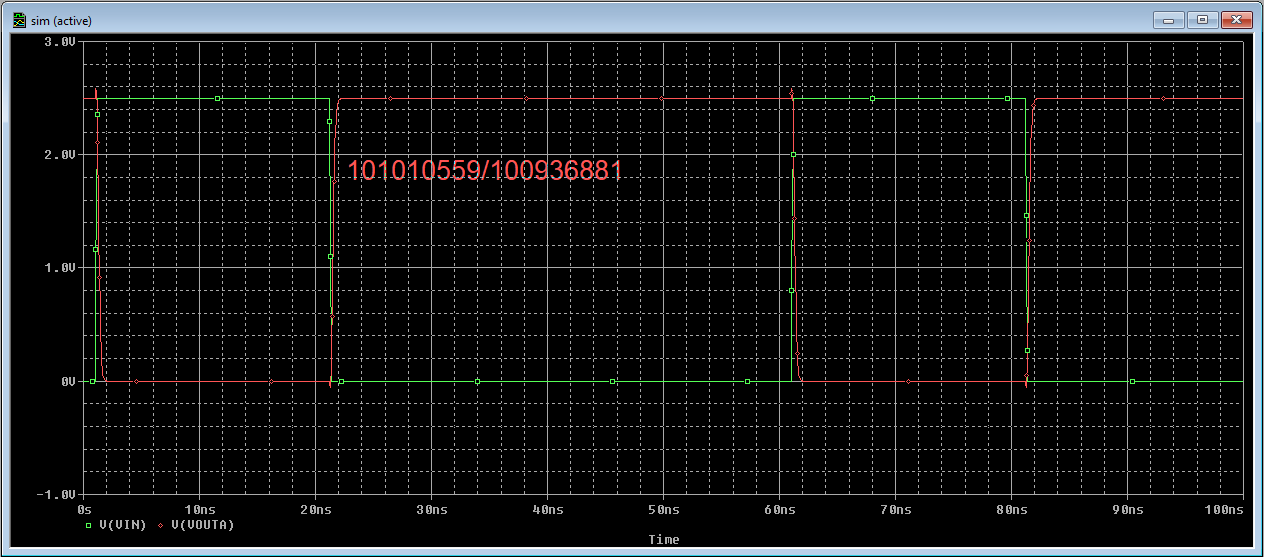
Rising Time: 350.356 ps

Falling Time: 336.904 ps

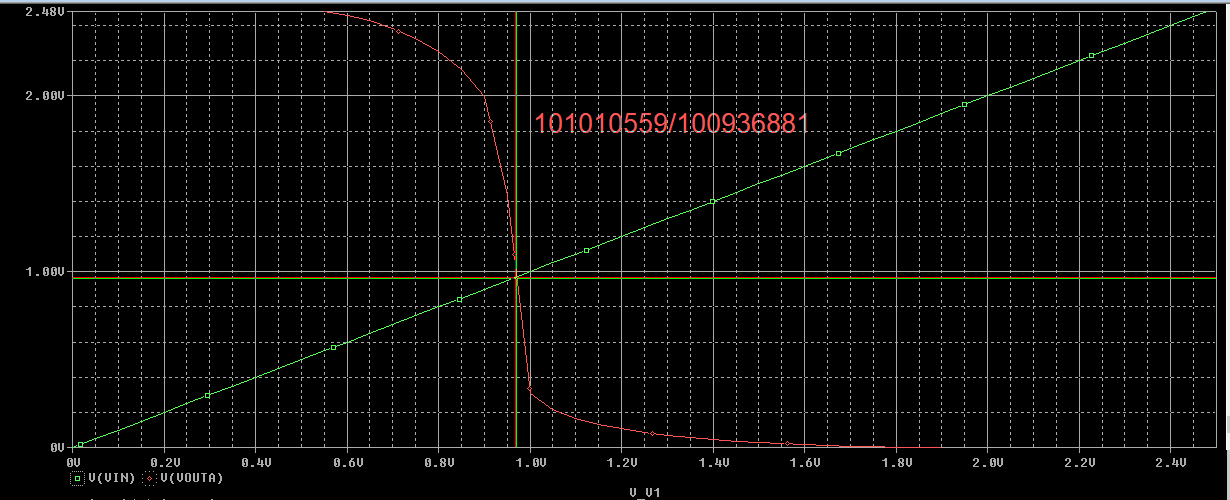
Rising Delay: 220.267 ps

Falling Delay: 228.232 ps

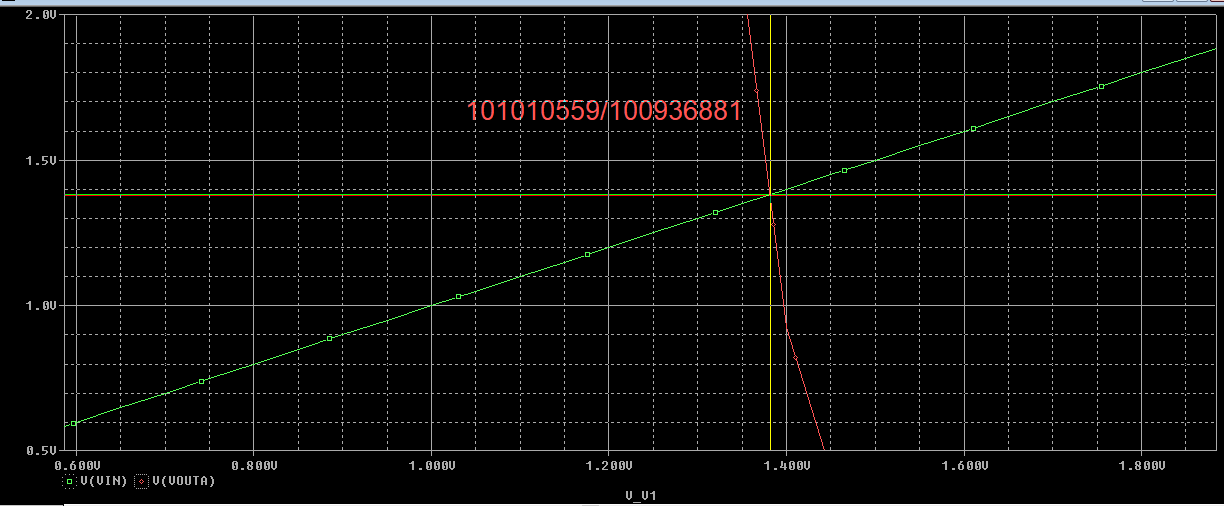
For the W/L ratio of 3.6, the rise and fall delays are within 5%.



Q6. The Switching Threshold is Vin=970.28 mV and Vout=963.88 mV.



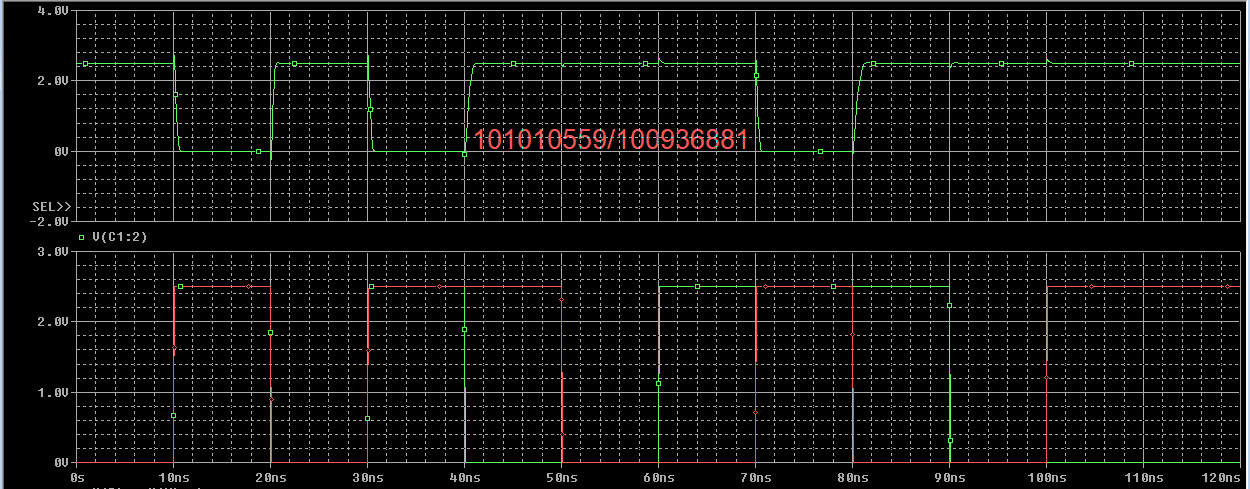
Q7. With the PMOS width at 8u, the Switching Threshold is at Vin = 1.3809 V and Vout = 1.3890 V. The Switching Threshold is much higher due to the lower resistance of the channel, which lets more current through, requiring a greater voltage to turn off.



2.1

Q8.

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Out | Delay |
| 0 | 0 | 1 | Rising: 327.089ps |
| 0 | 1 | 1 | Rising: 728.779 ps |
| 1 | 0 | 1 | Rising: 664.401 ps |
| 1 | 1 | 0 | Falling: 352.631 ps |



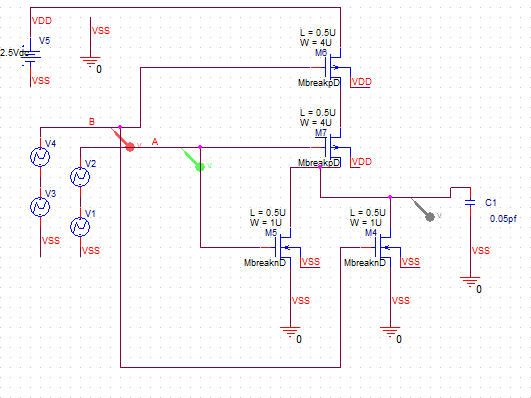
Q9. The worst case delay is when input A is low and B is high. The delay is 728.779 ps.

Q10. The best case rising delay is when both inputs are low. The delay is 327.089 ps.

Q11. When both the inputs are the low, the critical path is through only 1 transistor, since the PMOS are in parallel. When B is high and A is low, there is leakage through both NMOS circuit since they are in series, so it takes longer for the output to charge with one PMOS.

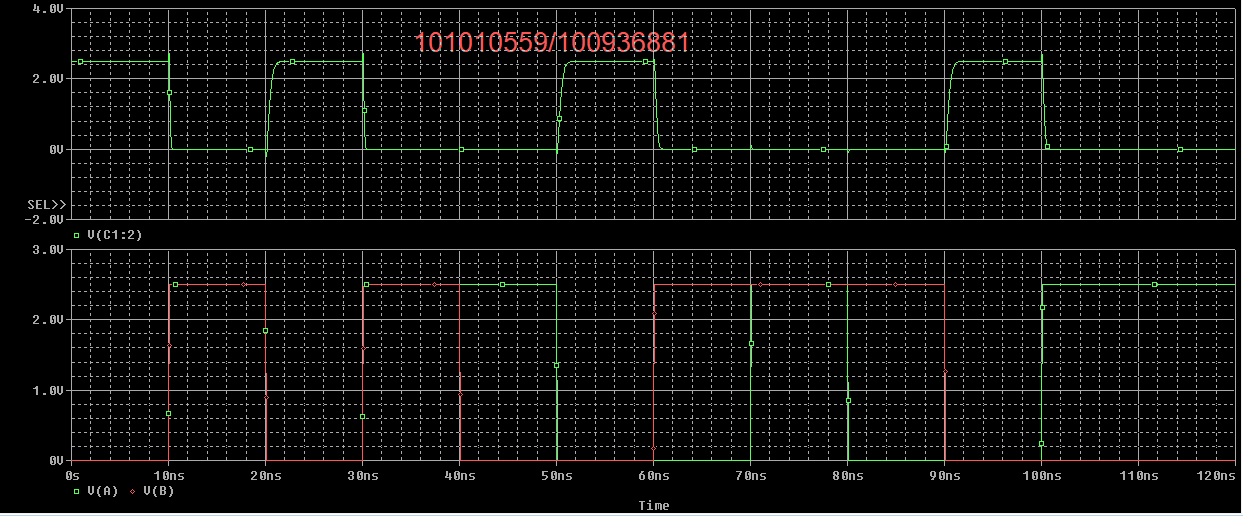
Q12. The falling delay is when both inputs are high because both PMOS are off and there is no way to charge the output. The delay is 352. 631 ps.

Q13.



Q14.

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Out | Delay |
| 0 | 0 | 1 | Rising: 661.454 ps |
| 0 | 1 | 0 | Falling: 344.358 ps |
| 1 | 0 | 0 | Falling: 410.953 ps |
| 1 | 1 | 0 | Falling: 176.568 ps |



Q15. The worst case delay is when input A and B are low. The delay is 661.454 ps.

Q16. The best case rising delay is when both inputs are high. The delay is 176.568 ps.

Q17. Since the PMOS are in series, the critical path when both inputs are low is through 2 transistors, leading to a larger delay. When both outputs are high, the output discharged faster because the NMOS are in parallel.

Q18. The rising delay is when both inputs are low because both PMOS are on and there is one path to charge the output. The delay is 661.454 ps.