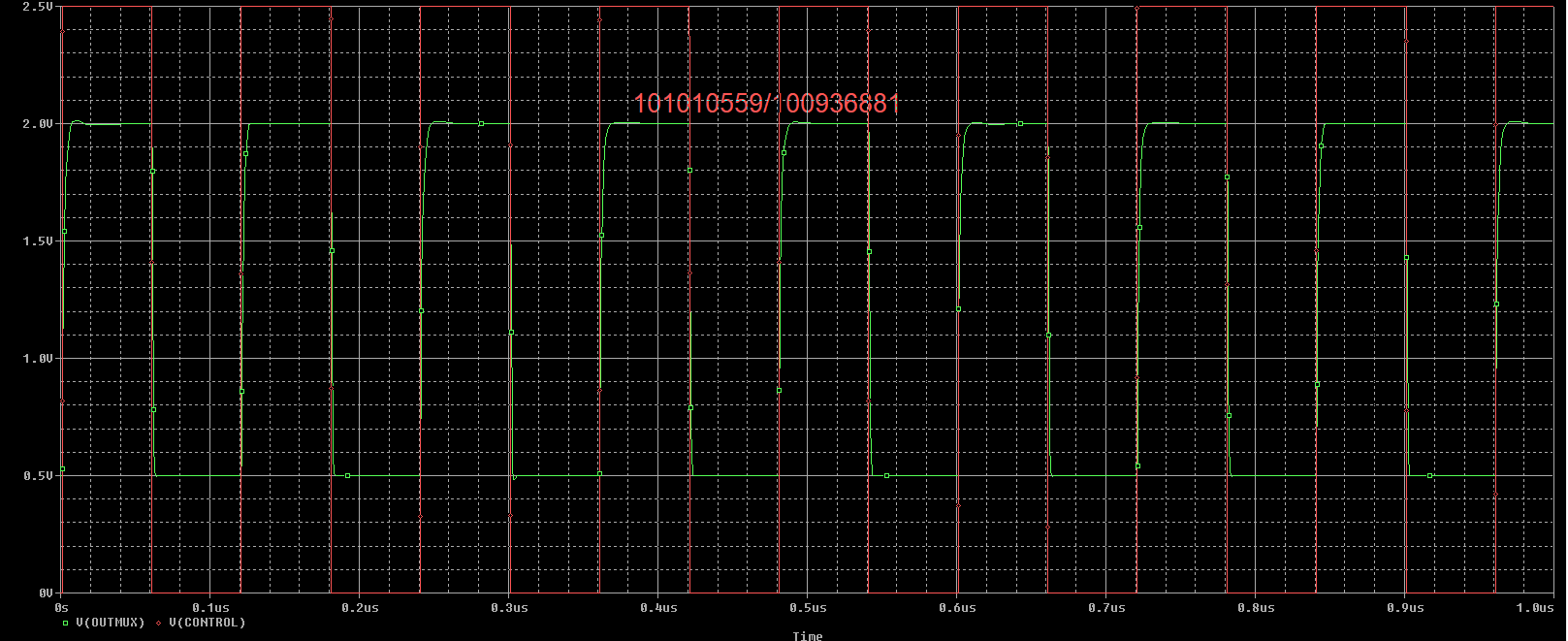
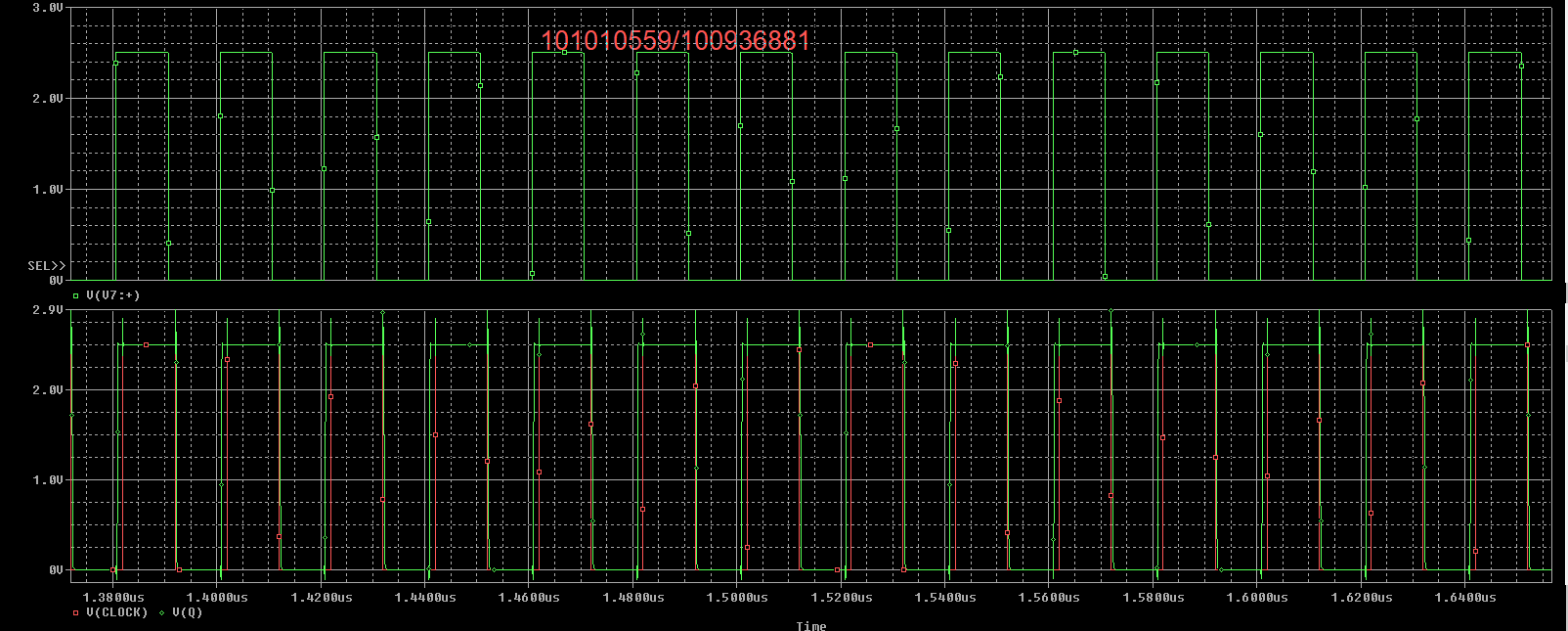
1

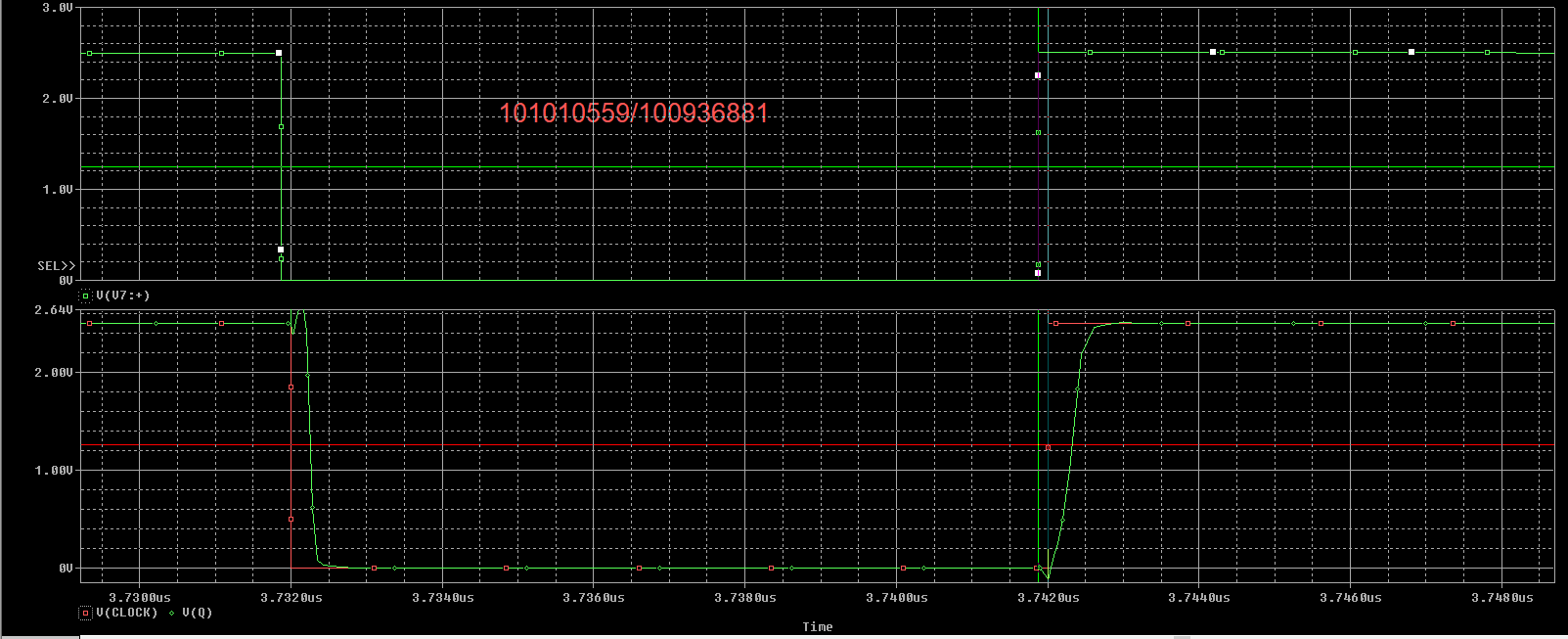
Q1) When the clock is high, the output is Vd=2.0 V and when the clock is low, the output is Vq = 0.5 V.

Q2) The time from control high y valid is tCHYV = 692.87 ps. The time from control low y valid is tCLYV = 650.385 ps.

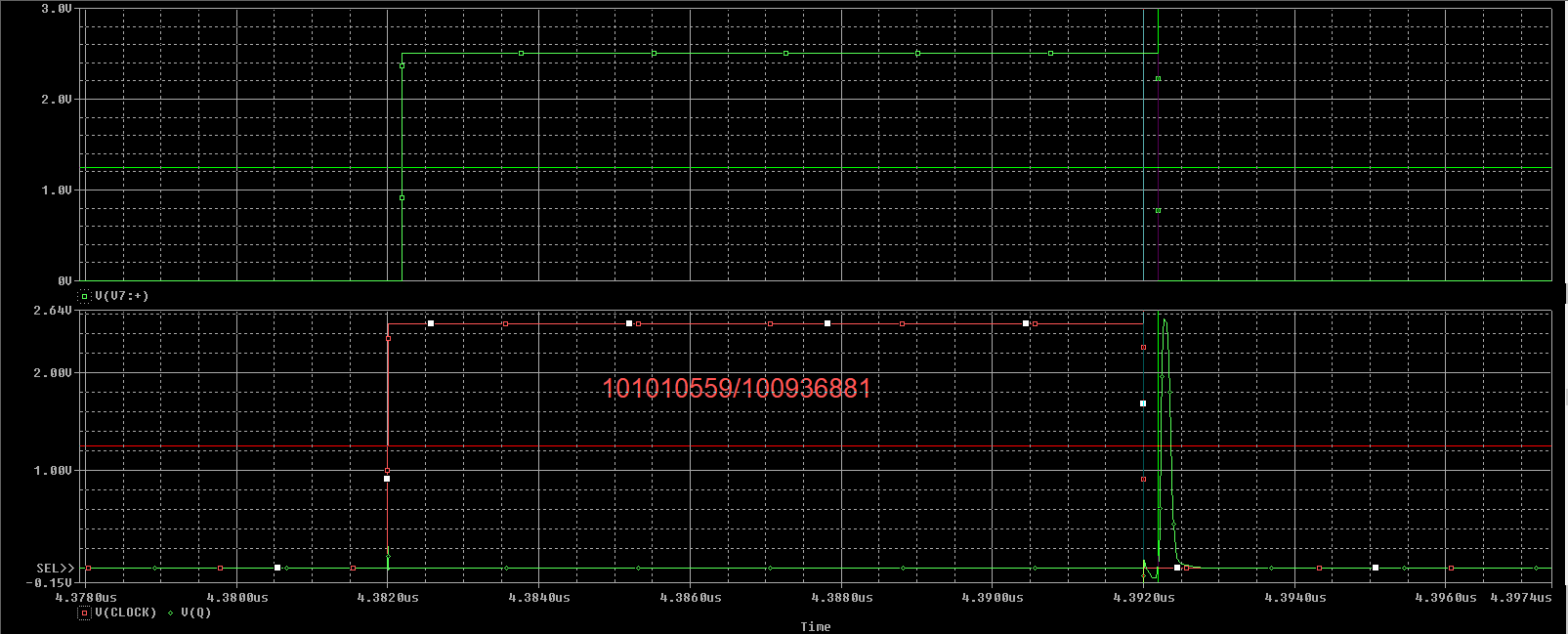
Q3) The buffers are added to the D-Latch to create a feedback loop to latch the data. It also refreshes the signal to keep from losing the data.

Q4) The output is Vin when CLK is zero and latches when CLK is 1. It is transparent because the output matches the input.

Q5) First time t1 = 130.00ps (last good).

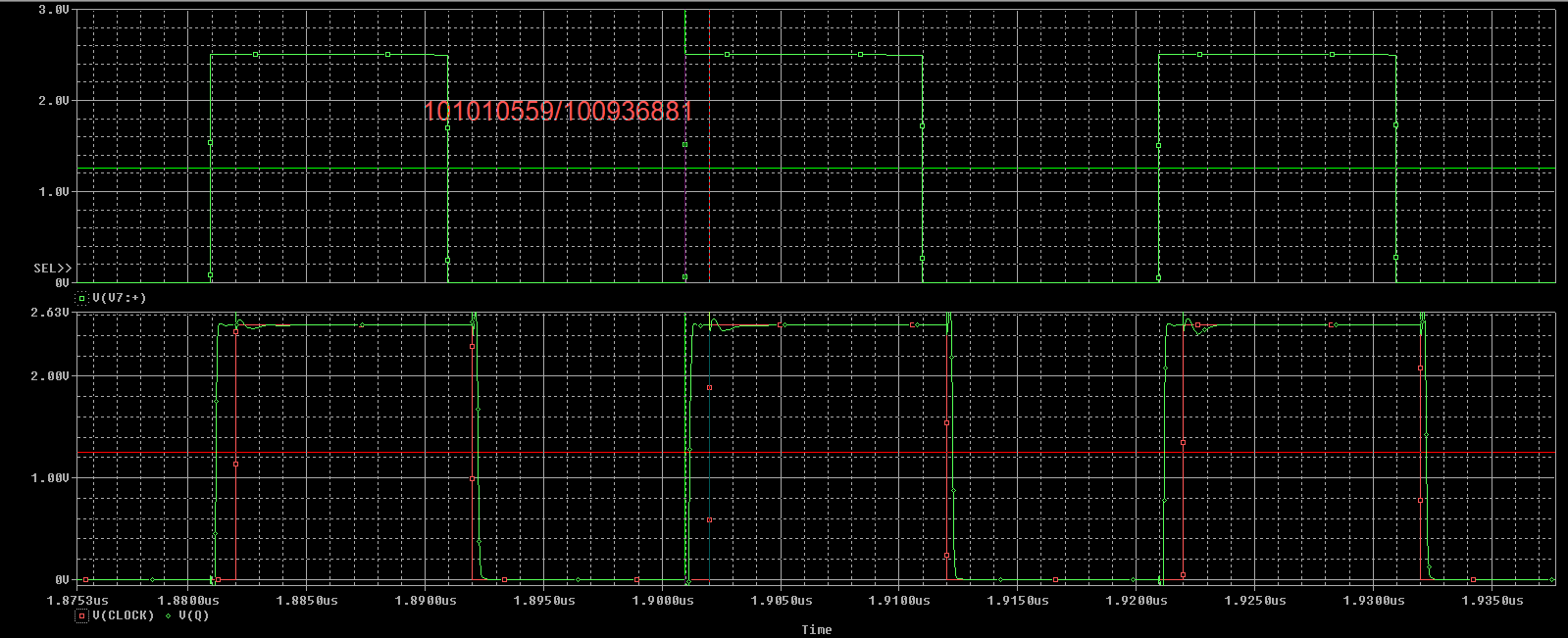


Second time t2 = 195.00 ps (first bad)

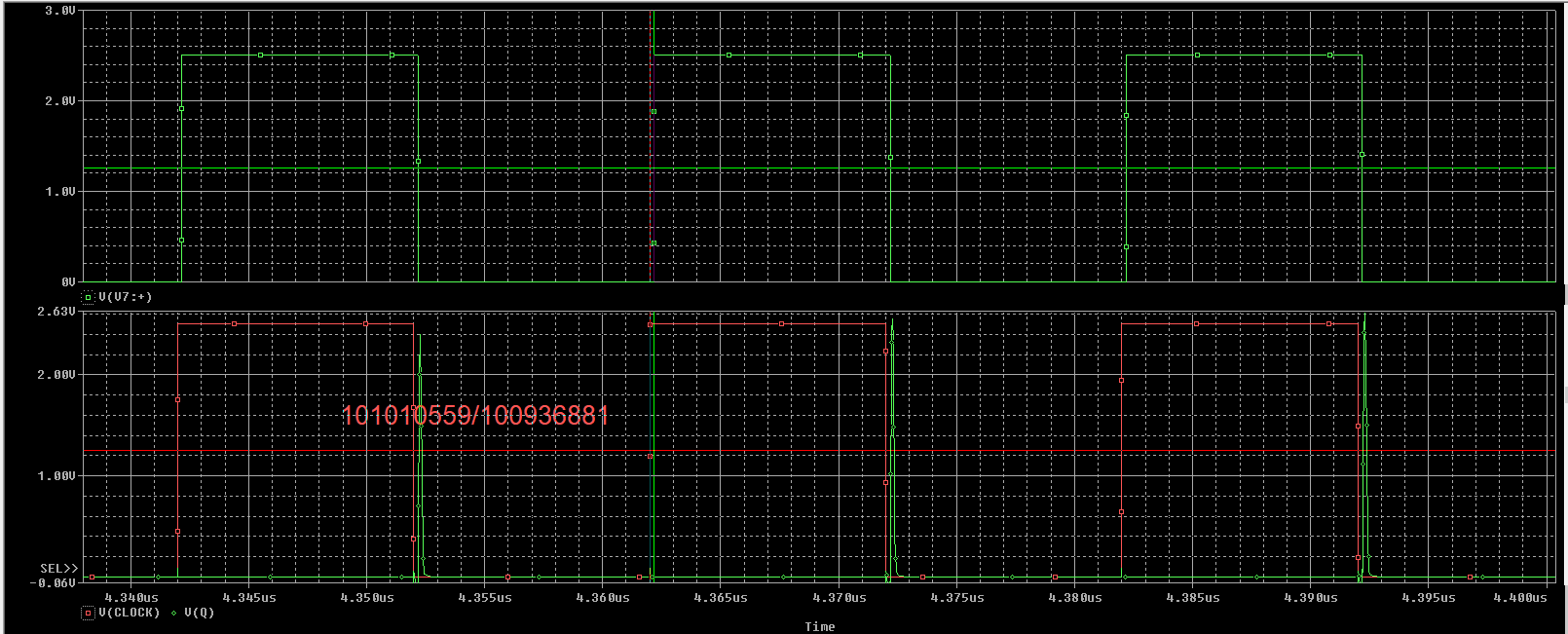


The setup time is between t1 and t2.

Q6) First time t1 = 1.05 ns (last good)



Second time t2 = 180.00 ps.



The setup time is between t1 and t2.

The setup time is longer due to the capacitor charging and discharging.

Q7) First time t1 = 2.5001 ns (last good). Second time t2 = 2.00 ns (first bad).

