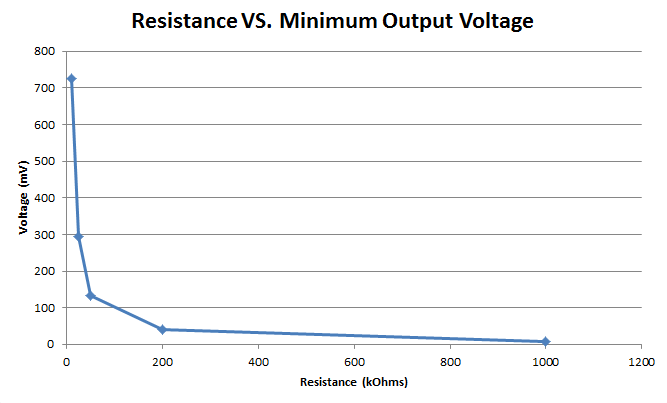
1.2.1

Q1.A)

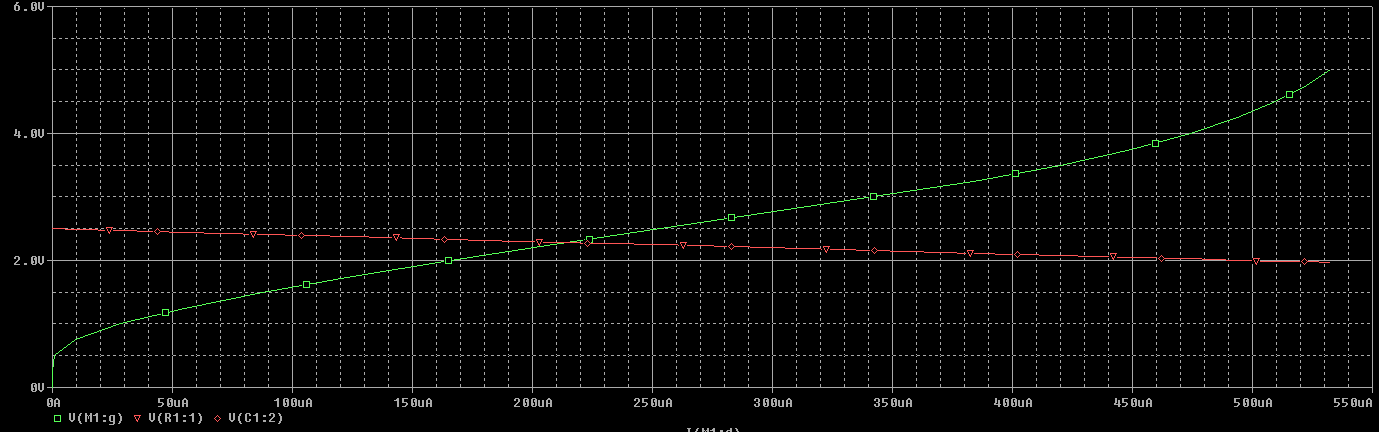
|  |  |
| --- | --- |
| Resistance (kOhms) | Vout min (mV) |
| 10 | 725.818 |
| 25 | 295.504 |
| 50 | 134.110 |
| 200 | 40.432 |
| 1000 | 8.0974 |



Q1.B) The delay from Vin rising 1.25V to Vin falling 1.25v is 435.533 ps.

Q1.C) If the R value is very high then the output charging time is very long.

Q2.A)

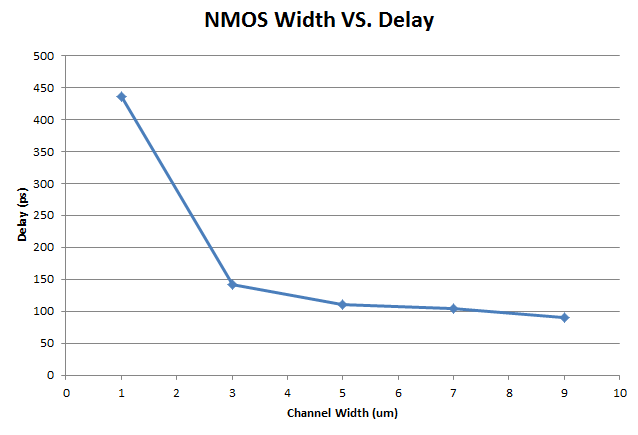


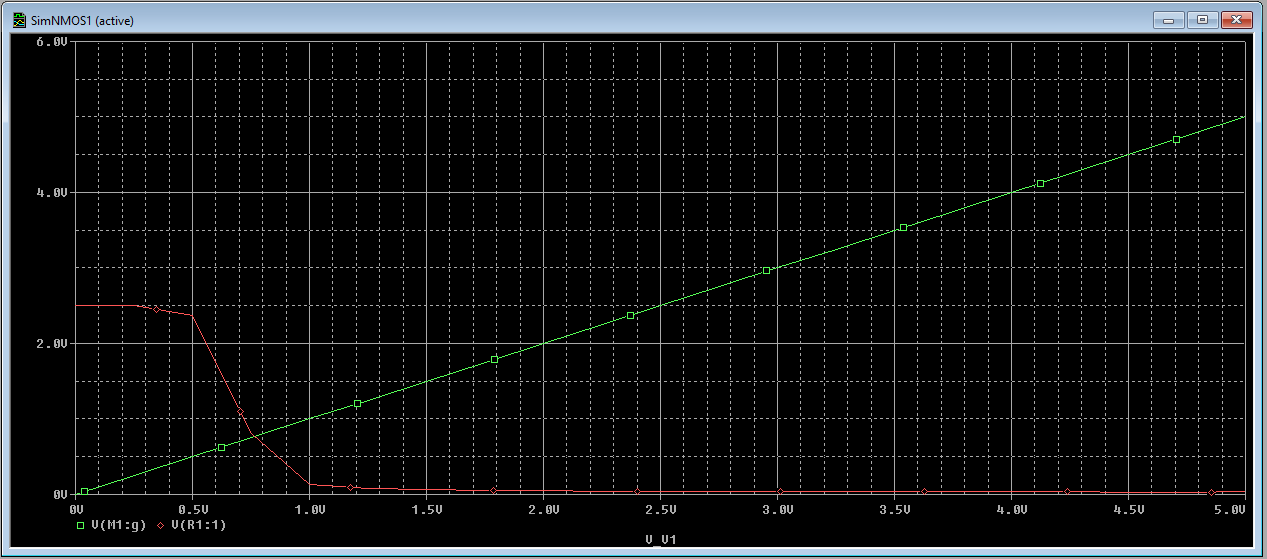
Q2.B) Green curve. From the plot there is a sharply defined threshold voltage, where above it the transistor starts conducting.

Q2.C) From the plot, the sharply defined threshold voltage is about 502 mV and the corresponding current is 792.079 ns. The maximum current is 532.515 µA

Q3. As width increases and length is unchanged, delay decreases due to wider channel to allow more flow.

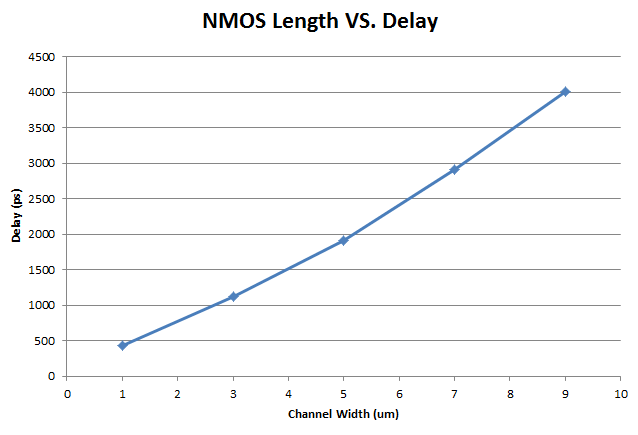
|  |  |
| --- | --- |
| W (um) | Delay (ps) |
| 1 | 436.227 |
| 3 | 141.547 |
| 5 | 110.586 |
| 7 | 103.583 |
| 9 | 90.052 |





Q4. As Length increases and width unchanged, delay increases due to channel distance increasing.

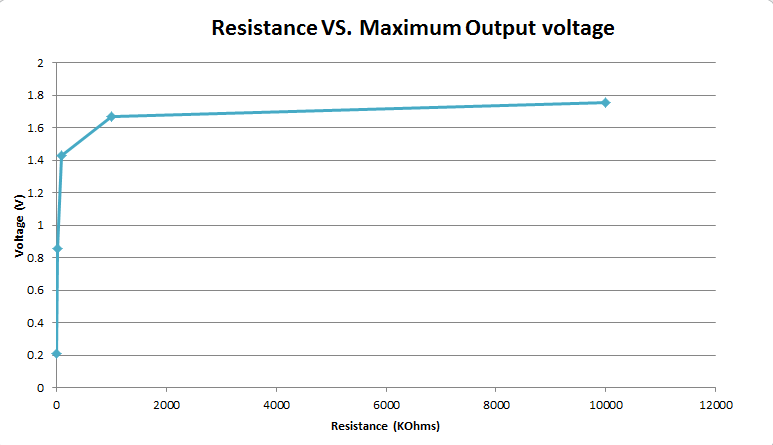
|  |  |
| --- | --- |
| L (um) | Delay (ps) |
| 1 | 434.693 |
| 3 | 1123.4 |
| 5 | 1913.4 |
| 7 | 2916.0 |
| 9 | 4003.4 |



1.2.2

Q5.A)

|  |  |
| --- | --- |
| Resistance k-ohms | Vout max (V) |
| 1 | 0.208950 |
| 10 | 0.856327 |
| 100 | 1.430 |
| 1000 | 1.6669 |
| 10000 | 1.7544 |



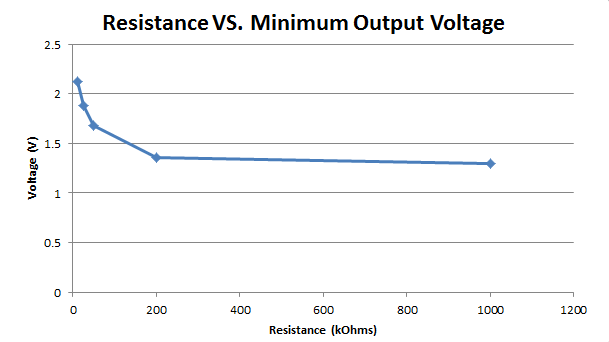
Q5.B) Estimate threshold voltage to be: Vt= Vdd – Vout(max); 2.5 - 1.7920 = 0.708 V. This threshold voltage is greater than the one estimated in Q2.C.

Q6. NMOS better as pulldown since cannot pull all the way up to vdd. At most Vout = VDD-Vt.

1.3.1

Q7.A) Charges slower as R increases

|  |  |
| --- | --- |
| Resistance k-ohms | Vout min (V) |
| 10 | 2.123 |
| 25 | 1.879 |
| 50 | 1.68 |
| 200 | 1.36 |
| 1000 | 1.294 |



Q7.B) About 0.879 V with R = 10000k

Q7.C) Estimate threshold Vt = GND – Vout; Vt = 0 - 0.879 V = 0.879 V.

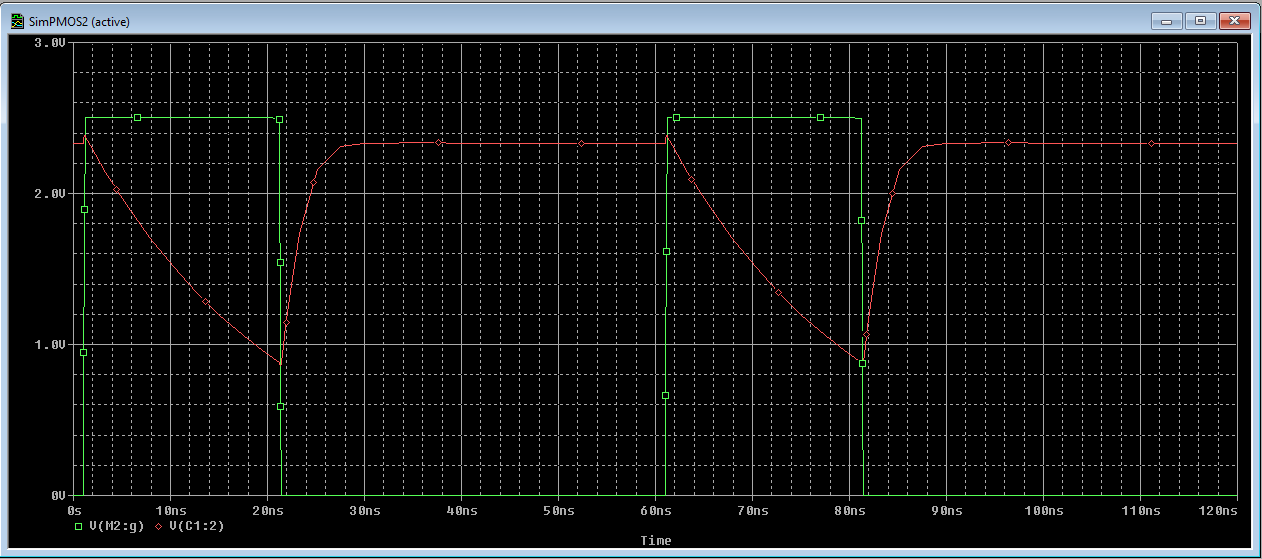
1.3.2

Q8. Discharge slower as R increases

|  |  |
| --- | --- |
| Resistance k-ohms | Vout max (mV) |
| 10 | 609 |
| 25 | 1365 |
| 50 | 1874 |
| 200 | 2334 |
| 1000 | 2466 |

Q9. I think in a digital circuit would perform better with the PMOS transistor in pull up because PMOS cannot pull all the way to ground, approximately GND-Vt.

1. Q10.A) The delay from Vin falling to 1.25V --> vout rising to 1.25V is 818.9 ps



Q10.B) Slower than NMOS; NMOS has delay of 435.533 ps while PMOS has a delay of 818.9 ps