Course Name: EMBEDDED SYSTEMS I / III

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Homework #: 10

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GitHub Link: No classroom link provided, so a public repo was created for PDF upload:

https://github.com/JonathanEly/EmbeddedSys_Sp21_HW10

Chapter 4:

4.1

Given a timer structured as in Figure 4.1 (c) and a clock frequency of 10 MHz: (a) Determine its range and resolution. (b) Calculate the terminal count value needed to measure 3 ms intervals. (c) If a prescaler is added, what is the minimum division needed to measure an interval of 100 ms? (Divisions should be in powers of 2.) Determine this design's range and resolution. (d) If instead of a prescaler a second 16-bit up-counter is cascaded as in Figure 4.1 (d), what is the range and resolution of this design?

a) Resolution: $\frac{1}{10{,}000{,}000 Hz} = 100\, ns$

Range: $(2^{16}) \cdot (100\, ns) = (65{,}536) \cdot (100\, ns) = 6.5536\, ms$

0 to 6.5536 ms

b) Terminal count value needed to measure 3 *ms* intervals:

$$\frac{3.0\, ms}{0.0001\, ms} = 30{,}000$$

c) If a prescaler is added, the minimum division needed to measure an interval of 100 *ms*:

$$\frac{(range)}{X} = 100\, ns$$

$$\frac{6.5536\, ms}{X} = 100\, ns$$

$$X = 15.2587 \approx 16 = 2^4$$

So the prescaler should use the minimum division of 2^4.

Resolution: $16 \cdot (100\, ns) = 1.6\, ms$

Range: $16 \cdot (6.5536\, ms) = 104.8576\, ms$

0 to 104.8576 ms

d) If we add another 16-bit up-counter to the system, the resolution should not change, but the range would be:

Range:

$$(2^{16})^2 \cdot (100\, ns) = (2^{32}) \cdot (100\, ns) = (4{,}294{,}967{,}296) \cdot (100\, ns) =$$

429.4967 s

Therefore, the range is: 0 to 429.4967 s

4.2

A watchdog timer that uses two cascaded 16-bit up-counters as in Figure 4.1 (d) is connected to an 11.981 MHz oscillator. A timeout should occur if the function watchdog_reset is not called within 5 minutes. What value should be loaded into the up-counter pair when the function is called?

Resolution: $\frac{1}{11{,}981{,}000 Hz} = 83.46548702\ldots\ ns$

Range: $(2^{32}) \cdot (83.46548702\ldots\ ns) = 358.481\ldots\ s$

0 to 358.481… s

$5\ mins = 300\ s$

So the loaded value should be the difference between the total range and the desired 5 minute timeout.

$$358.481\ldots\ s - 300\ s = 58.481\ldots\ s$$

Then, to get the counter value, we divide by the amount of time one counter tick takes:

$$\frac{58.481\ldots\ s}{83.465\ ns} = 700{,}667{,}296$$

So the value 700,667,296 should be loaded into the up-counter pair when the function is called.

*The decimal on the range and resolution are very long, so they've been abbreviated, but the complete value was used in the calculator to derive the final answer.

4.6

A particular motor operates at 10 revolutions per second when its controlling input voltage is 3.7 V. Assume that you are using a microcontroller with a PWM whose output port can be set high (5 V) or low (0 V). (a) Compute the duty cycle necessary to obtain 10 revolutions per second. (b) Provide values for a pulse width and period that achieve this duty cycle. You do not need to consider whether the frequency is too high or too low although the values should be reasonable. There is no one correct answer.

a) $Duty\ cycle\ =\ \frac{used\ input}{max\ input}\ \cdot\ (100)\ =\ \frac{3.7V}{5\,V}\ \cdot\ 100\ =\ 74\%\ duty\ cycle$

b) If we use a 125MHz clock:

$Period\ =\ \frac{1}{125{,}000{,}000Hz}\ =\ 8\,ns$

The pulse width would have to be "on" for 74% of the time, so:

$$Pulse\ Width\ =\ 8\,ns\ \cdot\ (0.74)\ =\ 5.92\,ns$$

4.15

Compute the memory needed in bytes to store a 4-bit digital encoding of a 3-second analog audio signal sampled every 10 milliseconds.

$3\,s\ =\ 3000\,ms$

Sampling every 10 *ms*:

$$3000\,ms\ \cdot\ (\frac{1\ sample}{10\ ms})\ =\ 300\ samples$$

300 total samples, storing 4 bits every sample:

$$300\ samples\ \cdot\ 4\ bits\ =\ 1200\ bits$$

Bits to bytes conversion:

$$1200\ bits\ \cdot\ (\frac{1\ byte}{8\ bits})\ =\ 150\ bytes$$

So it would take 150 bytes of memory to store a 4-bit digital encoding of a 3-second analog audio signal sampled every 10 ms.