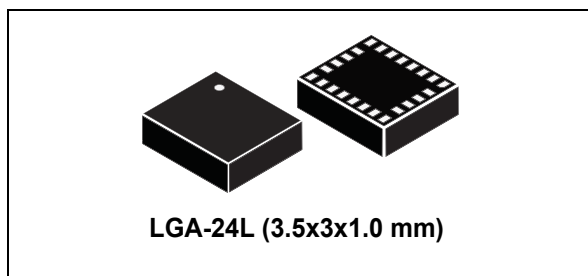


## iNEMO inertial module: 3D accelerometer, 3D gyroscope, 3D magnetometer

Datasheet - production data



### Features

- 3 acceleration channels, 3 angular rate channels, 3 magnetic field channels
- $\pm 2/\pm 4/\pm 8/\pm 16$  g linear acceleration full scale
- $\pm 4/\pm 8/\pm 12/\pm 16$  gauss magnetic full scale
- $\pm 245/\pm 500/\pm 2000$  dps angular rate full scale
- 16-bit data output
- SPI / I<sup>2</sup>C serial interfaces
- Analog supply voltage 1.9 V to 3.6 V
- “Always-on” eco power mode down to 1.9 mA
- Programmable interrupt generators
- Embedded temperature sensor
- Embedded FIFO
- Position and motion detection functions
- Click/double-click recognition
- Intelligent power saving for handheld devices
- ECOPACK<sup>®</sup>, RoHS and “Green” compliant

### Applications

- Indoor navigation
- Smart user interfaces
- Advanced gesture recognition
- Gaming and virtual reality input devices
- Display/map orientation and browsing

### Description

The LSM9DS1 is a system-in-package featuring a 3D digital linear acceleration sensor, a 3D digital angular rate sensor, and a 3D digital magnetic sensor.

The LSM9DS1 has a linear acceleration full scale of  $\pm 2g/\pm 4g/\pm 8/\pm 16$  g, a magnetic field full scale of  $\pm 4/\pm 8/\pm 12/\pm 16$  gauss and an angular rate of  $\pm 245/\pm 500/\pm 2000$  dps.

The LSM9DS1 includes an I<sup>2</sup>C serial bus interface supporting standard and fast mode (100 kHz and 400 kHz) and an SPI serial standard interface.

Magnetic, accelerometer and gyroscope sensing can be enabled or set in power-down mode separately for smart power management.

The LSM9DS1 is available in a plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

| Part number | Temperature range [°C] | Package | Packing       |
|-------------|------------------------|---------|---------------|
| LSM9DS1     | -40 to +85             | LGA-24L | Tray          |
| LSM9DS1TR   | -40 to +85             | LGA-24L | Tape and reel |

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1 Pin description

Figure 1. Pin connections

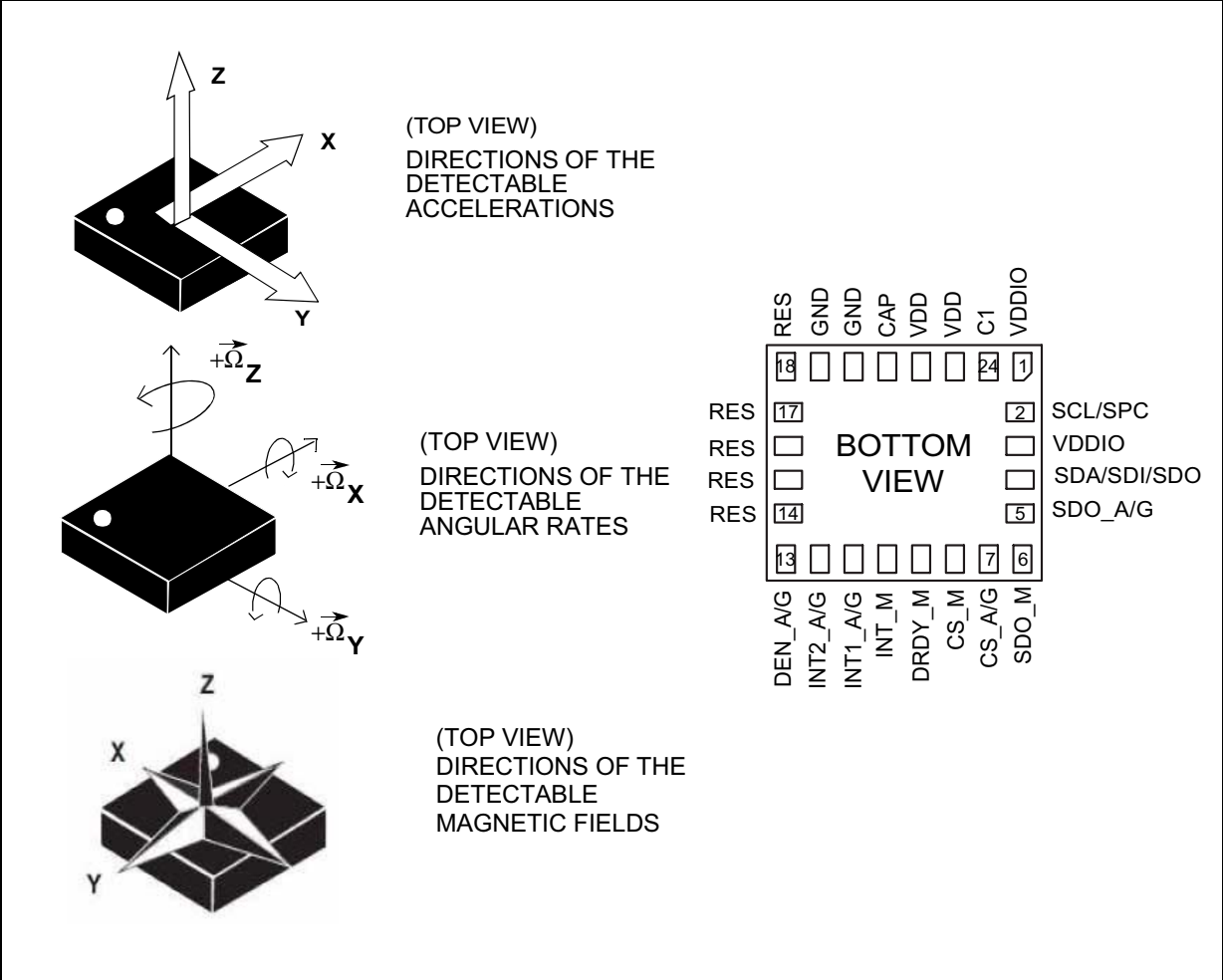


Table 2. Pin description

| Pin # | Name                 | Function   |
|-------|----------------------|--|
| 1     | VDDIO <sup>(1)</sup> | Power supply for I/O pins  |
| 2     | SCL/SPC              | I <sup>2</sup> C serial clock (SCL) / SPI serial port clock (SPC)  |
| 3     | VDDIO <sup>(2)</sup> | Power supply for I/O pins  |
| 4     | SDA/SDI/SDO          | I <sup>2</sup> C serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO)   |
| 5     | SDO_A/G              | SPI serial data output (SDO) for the accelerometer and gyroscope<br>I <sup>2</sup> C least significant bit of the device address (SA0) for the accelerometer and gyroscope                                     |
| 6     | SDO_M                | SPI serial data output (SDO) for the magnetometer<br>I <sup>2</sup> C least significant bit of the device address (SA0) for the magnetometer   |
| 7     | CS_A/G               | SPI enable<br>I <sup>2</sup> C/SPI mode selection for the accelerometer and gyroscope<br>(1: SPI idle mode / I <sup>2</sup> C communication enabled;<br>0: SPI communication mode / I <sup>2</sup> C disabled) |
| 8     | CS_M                 | SPI enable<br>I <sup>2</sup> C/SPI mode selection for the magnetometer<br>(1: SPI idle mode / I <sup>2</sup> C communication enabled;<br>0: SPI communication mode / I <sup>2</sup> C disabled)                |
| 9     | DRDY_M               | Magnetic sensor data ready   |
| 10    | INT_M                | Magnetic sensor interrupt  |
| 11    | INT1_A/G             | Accelerometer and gyroscope interrupt 1  |
| 12    | INT2_A/G             | Accelerometer and gyroscope interrupt 2  |
| 13    | DEN_A/G              | Accelerometer and gyroscope data enable  |
| 14    | RES                  | Reserved. Connected to GND.  |
| 15    | RES                  | Reserved. Connected to GND.  |
| 16    | RES                  | Reserved. Connected to GND.  |
| 17    | RES                  | Reserved. Connected to GND.  |
| 18    | RES                  | Reserved. Connected to GND.  |
| 19    | GND                  | 0 V supply   |
| 20    | GND                  | 0 V supply   |
| 21    | CAP                  | Connected to GND with ceramic capacitor <sup>(3)</sup>   |
| 22    | VDD <sup>(4)</sup>   | Power supply   |
| 23    | VDD <sup>(5)</sup>   | Power supply   |
| 24    | C1                   | Capacitor connection (C1 = 100 nF)   |

1. Recommended 100 nF filter capacitor.

2. Recommended 100 nF filter capacitor.

3. 10 nF (±10%), 16 V. 1 nF minimum value has to be guaranteed under 11 V bias condition.

4. Recommended 100 nF plus 10 µF capacitors.

5. Recommended 100 nF plus 10 µF capacitors.

## 2 Module specifications

### 2.1 Sensor characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted<sup>(a)</sup>

**Table 3. Sensor characteristics**

| Symbol   | Parameter   | Test conditions                     | Min. | Typ. <sup>(1)</sup> | Max. | Unit       |
|----------|---|-------------------------------------|------|---------------------|------|------------|
| LA_FS    | Linear acceleration measurement range                                   |                                     |      | ±2                  |      | g          |
|          |   |                                     |      | ±4                  |      |            |
|          |   |                                     |      | ±8                  |      |            |
|          |   |                                     |      | ±16                 |      |            |
| M_FS     | Magnetic measurement range  |                                     |      | ±4                  |      | gauss      |
|          |   |                                     |      | ±8                  |      |            |
|          |   |                                     |      | ±12                 |      |            |
|          |   |                                     |      | ±16                 |      |            |
| G_FS     | Angular rate measurement range  |                                     |      | ±245                |      | dps        |
|          |   |                                     |      | ±500                |      |            |
|          |   |                                     |      | ±2000               |      |            |
| LA_So    | Linear acceleration sensitivity   | Linear acceleration FS = ±2 g       |      | 0.061               |      | mg/LSB     |
|          |   | Linear acceleration FS = ±4 g       |      | 0.122               |      |            |
|          |   | Linear acceleration FS = ±8 g       |      | 0.244               |      |            |
|          |   | Linear acceleration FS = ±16 g      |      | 0.732               |      |            |
| M_GN     | Magnetic sensitivity  | Magnetic FS = ±4 gauss              |      | 0.14                |      | mgauss/LSB |
|          |   | Magnetic FS = ±8 gauss              |      | 0.29                |      |            |
|          |   | Magnetic FS = ±12 gauss             |      | 0.43                |      |            |
|          |   | Magnetic FS = ±16 gauss             |      | 0.58                |      |            |
| G_So     | Angular rate sensitivity  | Angular rate FS = ±245 dps          |      | 8.75                |      | mdps/LSB   |
|          |   | Angular rate FS = ±500 dps          |      | 17.50               |      |            |
|          |   | Angular rate FS = ±2000 dps         |      | 70                  |      |            |
| LA_TyOff | Linear acceleration typical zero-g level offset accuracy <sup>(2)</sup> | FS = ±8 g                           |      | ±90                 |      | mg         |
| M_TyOff  | Zero-gauss level <sup>(3)</sup>   | FS = ±4 gauss                       |      | ±1                  |      | gauss      |
| G_TyOff  | Angular rate typical zero-rate level <sup>(4)</sup>                     | FS = ±2000 dps                      |      | ±30                 |      | dps        |
| M_DF     | Magnetic disturbance field  | Zero-gauss offset starts to degrade |      |                     | 50   | gauss      |
| Top      | Operating temperature range   |                                     | -40  |                     | +85  | °C         |

1. Typical specifications are not guaranteed

2. Typical zero-g level offset value after soldering

3. Typical zero-gauss level value after test and trimming

4. Typical zero rate level offset value after MSL3 preconditioning

a. The product is factory calibrated at 2.2 V. The operational power supply range is from 1.9 V to 3.6 V.

## 2.2 Electrical characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted<sup>(b)</sup>

**Table 4. Electrical characteristics**

| Symbol | Parameter  | Test conditions | Min. | Typ. <sup>(1)</sup> | Max.    | Unit |
|--------|--|-----------------|------|---------------------|---------|------|
| Vdd    | Supply voltage   |                 | 1.9  |                     | 3.6     | V    |
| Vdd_IO | Module power supply for I/O  |                 | 1.71 |                     | Vdd+0.1 |      |
| Idd_XM | Current consumption of the accelerometer and magnetic sensor in normal mode <sup>(2)</sup> |                 |      | 600                 |         | μA   |
| Idd_G  | Gyroscope current consumption in normal mode <sup>(3)</sup>                                |                 |      | 4.0                 |         | mA   |
| Top    | Operating temperature range  |                 | -40  |                     | +85     | °C   |
| Trise  | Time for power supply rising <sup>(4)</sup>  |                 | 0.01 |                     | 100     | ms   |
| Twait  | Time delay between Vdd_IO and Vdd <sup>(4)</sup>   |                 | 0    |                     | 10      | ms   |

1. Typical specifications are not guaranteed

2. Magnetic sensor in high-resolution mode (ODR = 20 Hz), accelerometer sensor in normal mode, gyroscope in power-down mode

3. Accelerometer and magnetic sensor in power-down mode

4. Please refer to [Section 2.2.1: Recommended power-up sequence](#) for more details.

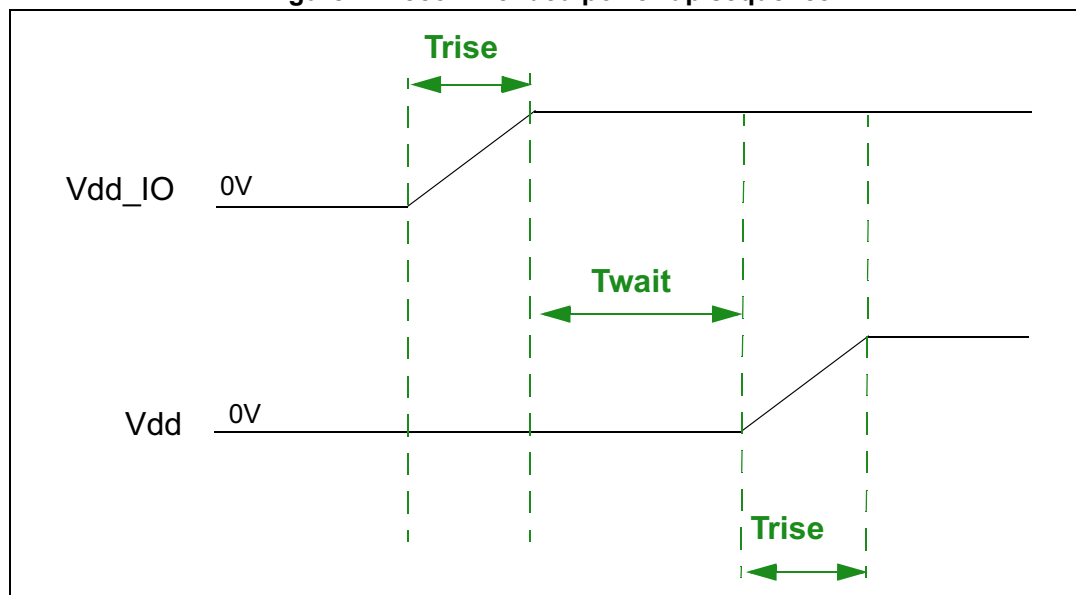
b. LSM9DS1 is factory calibrated at 2.2 V.

### 2.2.1 Recommended power-up sequence

For the power-up sequence please refer to the following figure, where:

- Trise is the time for the power supply to rise from 10% to 90% of its final value
- Twait is the delay between the end of the Vdd\_IO ramp (90% of its final value) and the start of the Vdd ramp

Figure 2. Recommended power-up sequence



## 2.3 Temperature sensor characteristics

@ Vdd = 2.2 V, T = 25 °C unless otherwise noted <sup>(c)</sup>

Table 5. Temperature sensor characteristics

| Symbol | Parameter                              | Test condition          | Min. | Typ. <sup>(1)</sup> | Max. | Unit   |
|--------|--|-------------------------|------|---------------------|------|--------|
| TODR   | Temperature refresh rate               | Gyro OFF <sup>(2)</sup> |      | 50                  |      | Hz     |
|        |  | Gyro ON                 |      | 59.5                |      |        |
| TSen   | Temperature sensitivity <sup>(3)</sup> |                         |      | 16                  |      | LSB/°C |
| Top    | Operating temperature range            |                         | -40  |                     | +85  | °C     |

1. Typical specifications are not guaranteed.

2. When the accelerometer ODR is set to 10 Hz and the gyroscope part is turned off, the TODR value is 10 Hz.

3. The output of the temperature sensor is 0 (typ.) at 25 °C

c. The product is factory calibrated at 2.2 V.

## 2.4 Communication interface characteristics

### 2.4.1 SPI - serial peripheral interface

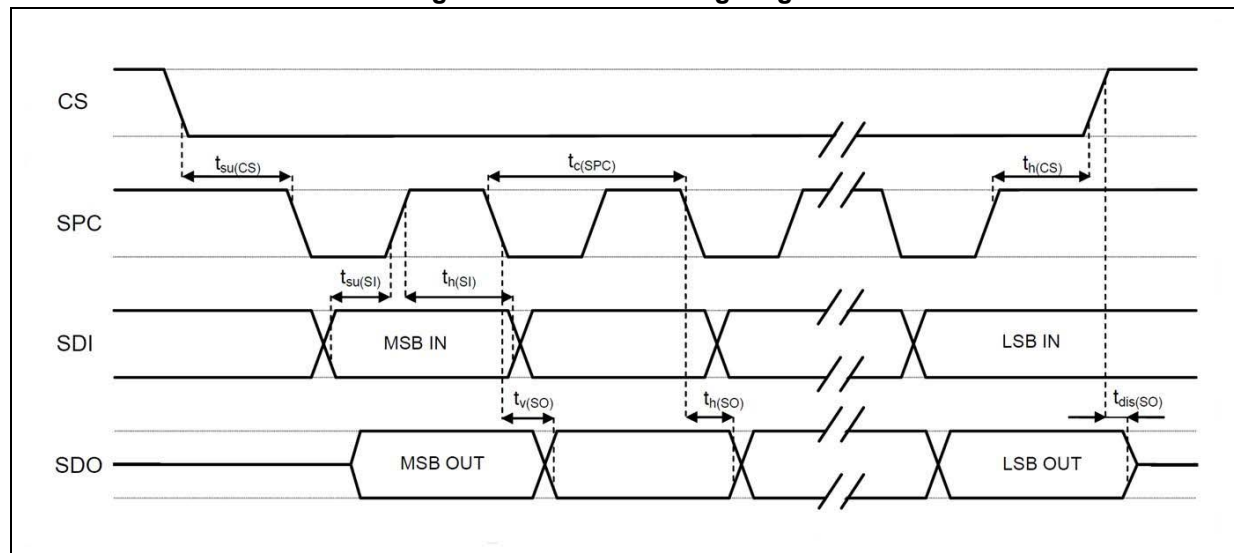
Subject to general operating conditions for Vdd and Top.

**Table 6. SPI slave timing values**

| Symbol        | Parameter               | Value <sup>(1)</sup> |     | Unit |
|---------------|-------------------------|----------------------|-----|------|
|               |                         | Min                  | Max |      |
| $t_{c(SPC)}$  | SPI clock cycle         | 100                  |     | ns   |
| $f_{c(SPC)}$  | SPI clock frequency     |                      | 10  | MHz  |
| $t_{su(CS)}$  | CS setup time           | 5                    |     | ns   |
| $t_{h(CS)}$   | CS hold time            | 20                   |     |      |
| $t_{su(SI)}$  | SDI input setup time    | 5                    |     |      |
| $t_{h(SI)}$   | SDI input hold time     | 15                   |     |      |
| $t_{v(SO)}$   | SDO valid output time   |                      | 50  |      |
| $t_{h(SO)}$   | SDO output hold time    | 5                    |     |      |
| $t_{dis(SO)}$ | SDO output disable time |                      | 50  |      |

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

**Figure 3. SPI slave timing diagram**



**Note:** Measurement points are done at  $0.2 \cdot V_{dd\_IO}$  and  $0.8 \cdot V_{dd\_IO}$ , for both input and output ports.

## 2.4.2 I<sup>2</sup>C - inter-IC control interface

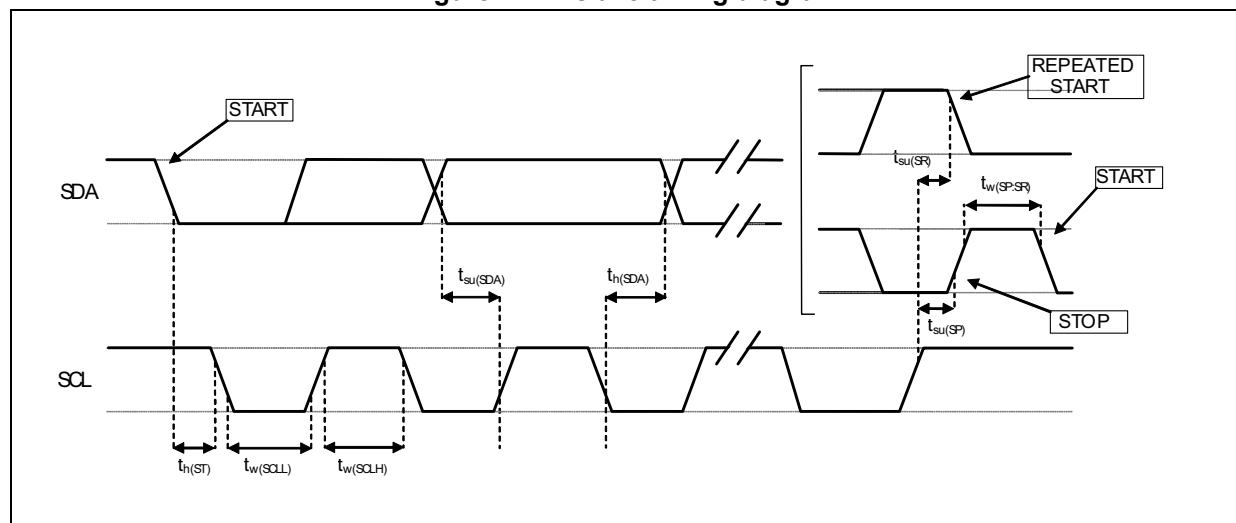
Subject to general operating conditions for V<sub>dd</sub> and T<sub>op</sub>.

Table 7. I<sup>2</sup>C slave timing values

| Symbol                | Parameter                                      | I <sup>2</sup> C Standard mode <sup>(1)</sup> |      | I <sup>2</sup> C Fast mode <sup>(1)</sup> |     | Unit |
|-----------------------|--|---|------|---|-----|------|
|                       |  | Min   | Max  | Min                                       | Max |      |
| f <sub>(SCL)</sub>    | SCL clock frequency                            | 0   | 100  | 0   | 400 | kHz  |
| t <sub>w(SCLL)</sub>  | SCL clock low time                             | 4.7   |      | 1.3                                       |     | μs   |
| t <sub>w(SCLH)</sub>  | SCL clock high time                            | 4.0   |      | 0.6                                       |     |      |
| t <sub>su(SDA)</sub>  | SDA setup time                                 | 250   |      | 100                                       |     | ns   |
| t <sub>h(SDA)</sub>   | SDA data hold time                             | 0   | 3.45 | 0   | 0.9 | μs   |
| t <sub>h(ST)</sub>    | START condition hold time                      | 4   |      | 0.6                                       |     | μs   |
| t <sub>su(SR)</sub>   | Repeated START condition setup time            | 4.7   |      | 0.6                                       |     |      |
| t <sub>su(SP)</sub>   | STOP condition setup time                      | 4   |      | 0.6                                       |     |      |
| t <sub>w(SP:SR)</sub> | Bus free time between STOP and START condition | 4.7   |      | 1.3                                       |     |      |

1. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production.

Figure 4. I<sup>2</sup>C slave timing diagram



Note: Measurement points are done at 0.2·V<sub>dd\_IO</sub> and 0.8·V<sub>dd\_IO</sub>, for both ports



## 2.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 8. Absolute maximum ratings**

| Symbol             | Ratings   | Maximum value                   | Unit  |
|--------------------|---|---------------------------------|-------|
| V <sub>dd</sub>    | Supply voltage  | -0.3 to 4.8                     | V     |
| V <sub>dd_IO</sub> | I/O pins supply voltage   | -0.3 to 4.8                     | V     |
| V <sub>in</sub>    | Input voltage on any control pin<br>(including CS_A/G, CS_M, SCL/SPC, SDA/SDI/SDO,<br>SDO_A/G, SDO_M) | 0.3 to V <sub>dd_IO</sub> + 0.3 | V     |
| A <sub>UNP</sub>   | Acceleration (any axis)   | 3,000 for 0.5 ms                | g     |
|                    |   | 10,000 for 0.1 ms               | g     |
| M <sub>EF</sub>    | Maximum exposed field   | 1000                            | gauss |
| ESD                | Electrostatic discharge protection (HBM)  | 2                               | kV    |
| T <sub>STG</sub>   | Storage temperature range   | -40 to +125                     | °C    |

*Note:* Supply voltage on any pin should never exceed 4.8 V.



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

## 2.6 Terminology

### 2.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so,  $\pm 1$  *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

An angular rate gyroscope is device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

Magnetic sensor sensitivity describes the gain of the sensor and can be determined, for example, by applying a magnetic field of 1 *gauss* to it.

### 2.6.2 Zero-g, zero-rate and zero-gauss level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X-axis and Y-axis, whereas the Z-axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in [Table 3](#). The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

Zero-gauss level offset (M\_TyOff) describes the deviation of an actual output signal from the ideal output if no magnetic field is present.

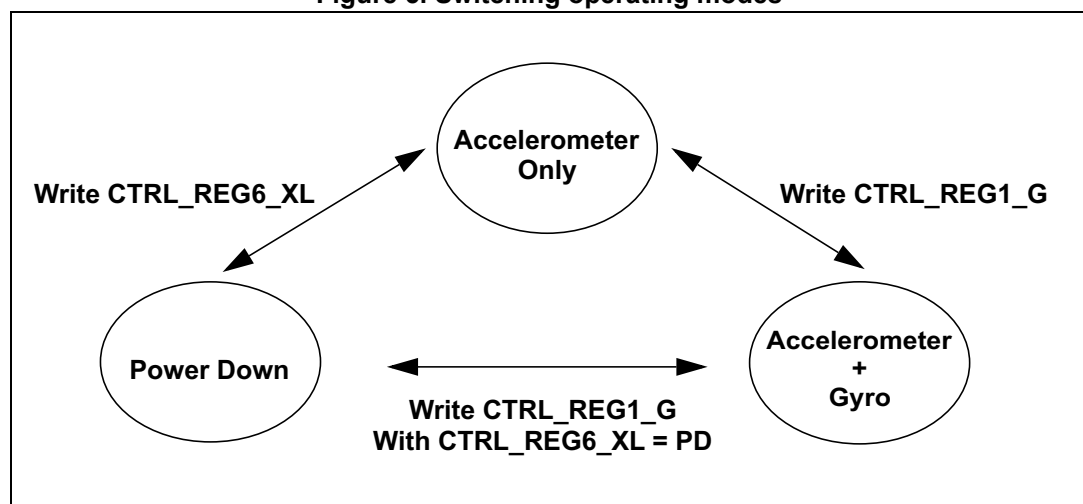
## 3 LSM9DS1 functionality

### 3.1 Operating modes

In the LSM9DS1 the accelerometer and gyroscope have two operating modes available: only accelerometer active and gyroscope in power down or both accelerometer and gyroscope sensors active at the same ODR. Switching from one mode to the other requires one write operation: writing to [CTRL\\_REG6\\_XL \(20h\)](#), the accelerometer operates in normal mode and the gyroscope is powered down, writing to [CTRL\\_REG1\\_G \(10h\)](#) both accelerometer and gyroscope are activated at the same ODR.

[Figure 5](#) depicts both modes of operation from power down.

**Figure 5. Switching operating modes**



The magnetic sensor has three operating modes available: power-down (default), continuous-conversion mode and single-conversion mode. Switching from power-down to the other modes requires one write operation to [CTRL\\_REG3\\_M \(22h\)](#), setting values in the MD[1:0] bits. For the output of the magnetic data compensated by temperature, the TEMP\_COMP bit in [CTRL\\_REG1\\_M \(20h\)](#) must be set to '1'.

### 3.2 Gyroscope power modes

In the LSM9DS1, the gyroscope can be configured in three different operating modes: power-down, low-power and normal mode.

Low-power mode is available for lower ODR (14.9, 59.5, 119 Hz) while for greater ODR (238, 476, 952 Hz) the device is automatically in normal mode. [Table](#) summarizes the ODR configuration (ODR\_G[2:0] bits set in [CTRL\\_REG1\\_G \(10h\)](#)) and corresponding power modes.

To enable low-power mode, the LP\_mode bit in [CTRL\\_REG3\\_G \(12h\)](#) has to be set to '1'.

Low-power mode allows reaching low power consumption while maintaining the device always on, refer to [Table 10](#).

**Table 9. Gyroscope operating modes**

| ODR_G [2:0] | ODR [Hz]   | Power mode            |
|-------------|------------|-----------------------|
| 000         | Power down | Power-down            |
| 001         | 14.9       | Low-power/Normal mode |
| 010         | 59.5       | Low-power/Normal mode |
| 011         | 119        | Low-power/Normal mode |
| 100         | 238        | Normal mode           |
| 101         | 476        | Normal mode           |
| 110         | 952        | Normal mode           |

**Table 10. Operating mode current consumption**

| ODR [Hz] | Power mode  | Current consumption <sup>(1)</sup><br>[mA] |
|----------|-------------|--|
| 14.9     | Low-power   | 1.9  |
| 59.5     | Low-power   | 2.4  |
| 119      | Low-power   | 3.1  |
| 238      | Normal mode | 4.3  |
| 476      | Normal mode | 4.3  |
| 952      | Normal mode | 4.3  |

1. Typical values of gyroscope and accelerometer current consumption are based on characterization data.

**Table 11. Accelerometer turn-on time**

| ODR [Hz] | BW = 400 Hz <sup>(1)</sup> | BW = 200 Hz <sup>(1)</sup> | BW = 100 Hz <sup>(1)</sup> | BW = 50 Hz <sup>(1)</sup> |
|----------|----------------------------|----------------------------|----------------------------|---------------------------|
| 14.9     | 0                          | 0                          | 0                          | 0                         |
| 59.5     | 0                          | 0                          | 0                          | 0                         |
| 119      | 1                          | 1                          | 1                          | 2                         |
| 238      | 1                          | 1                          | 2                          | 4                         |
| 476      | 1                          | 2                          | 4                          | 7                         |
| 952      | 2                          | 4                          | 7                          | 14                        |

1. The table contains the number of samples to be discarded after switching between power-down mode and normal mode.

Table 12. Gyroscope turn-on time

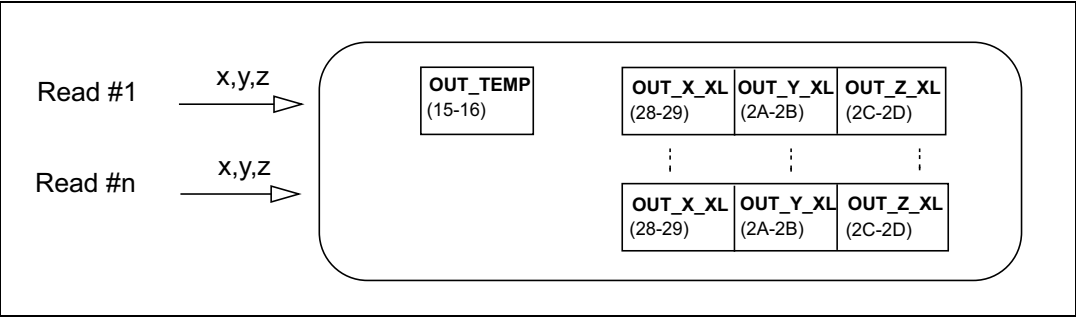
| ODR [Hz]    | LPF1 only <sup>(1)</sup> | LPF1 and LPF2 <sup>(1)</sup> |
|-------------|--------------------------|------------------------------|
| 14.9        | 2                        | LPF2 not available           |
| 59.5 or 119 | 3                        | 13                           |
| 238         | 4                        | 14                           |
| 476         | 5                        | 15                           |
| 952         | 8                        | 18                           |

1. The table contains the number of samples to be discarded after switching between low-power mode and normal mode.

### 3.3 Accelerometer and gyroscope multiple reads (burst)

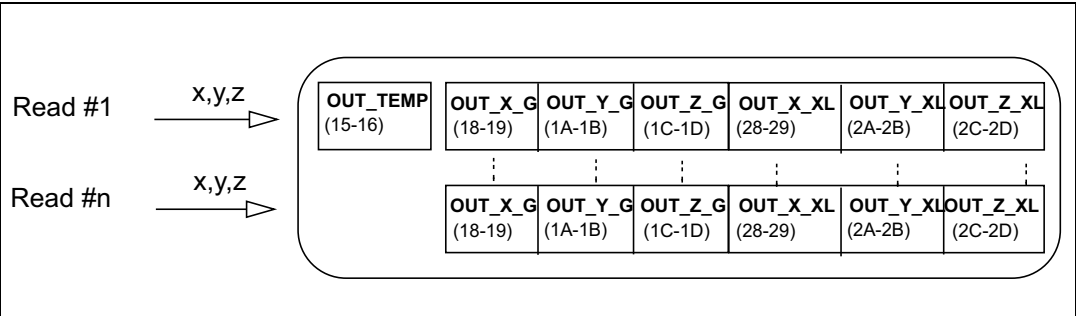
When only accelerometer is activated and the gyroscope is in power down, starting from [OUT\\_X\\_XL \(28h - 29h\)](#) multiple reads can be performed. Once [OUT\\_Z\\_XL \(2Ch - 2Dh\)](#) is read, the system automatically restarts from [OUT\\_X\\_XL \(28h - 29h\)](#) (see [Figure 6](#)).

Figure 6. Multiple reads: accelerometer only



When both accelerometer and gyroscope sensors are activated at the same ODR, starting from [OUT\\_X\\_G \(18h - 19h\)](#) multiple reads can be performed. Once [OUT\\_Z\\_XL \(2Ch - 2Dh\)](#) is read, the system automatically restarts from [OUT\\_X\\_G \(18h - 19h\)](#) (see [Figure 7](#)).

Figure 7. Multiple reads: accelerometer and gyroscope



3.4 Block diagram

Figure 8. Accelerometer and gyroscope digital block diagram

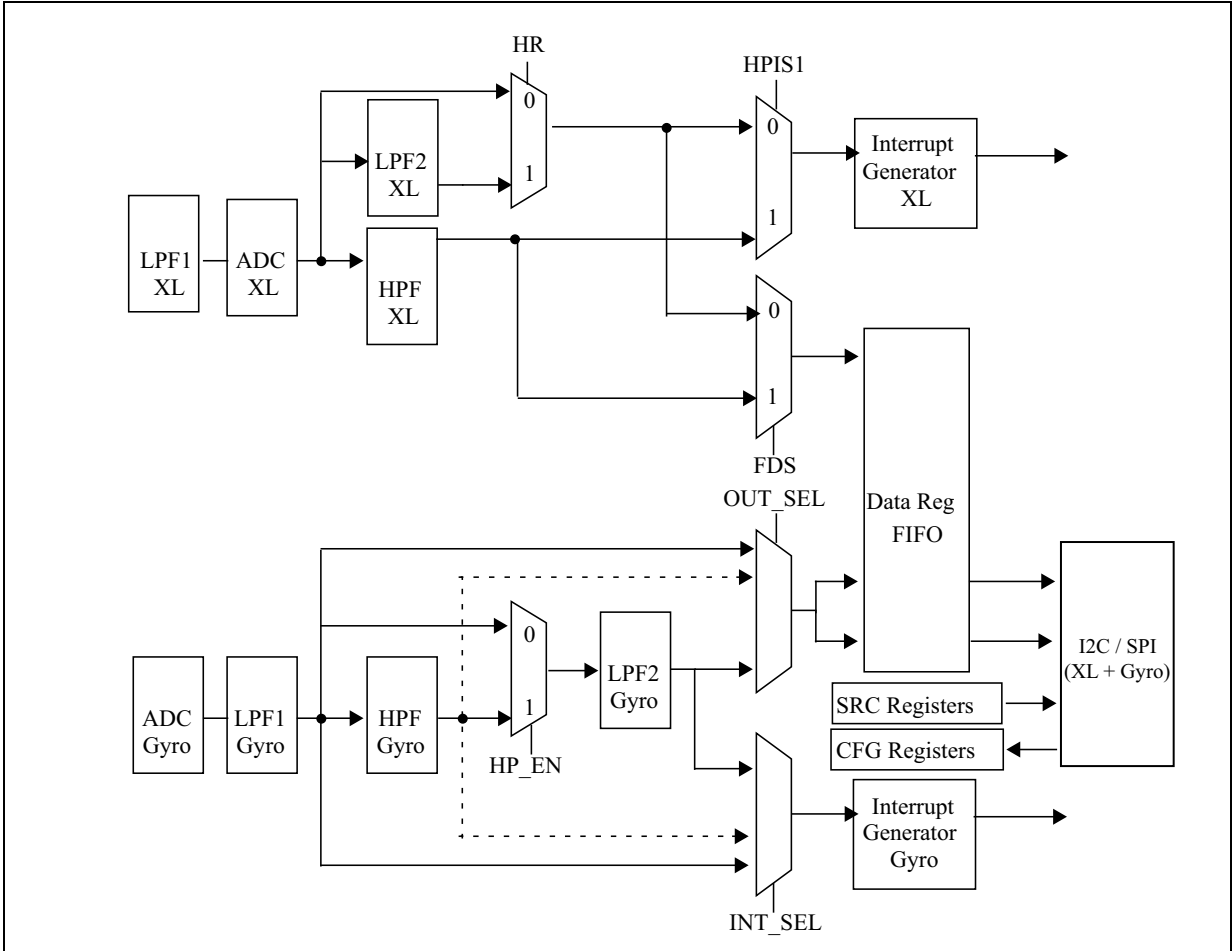
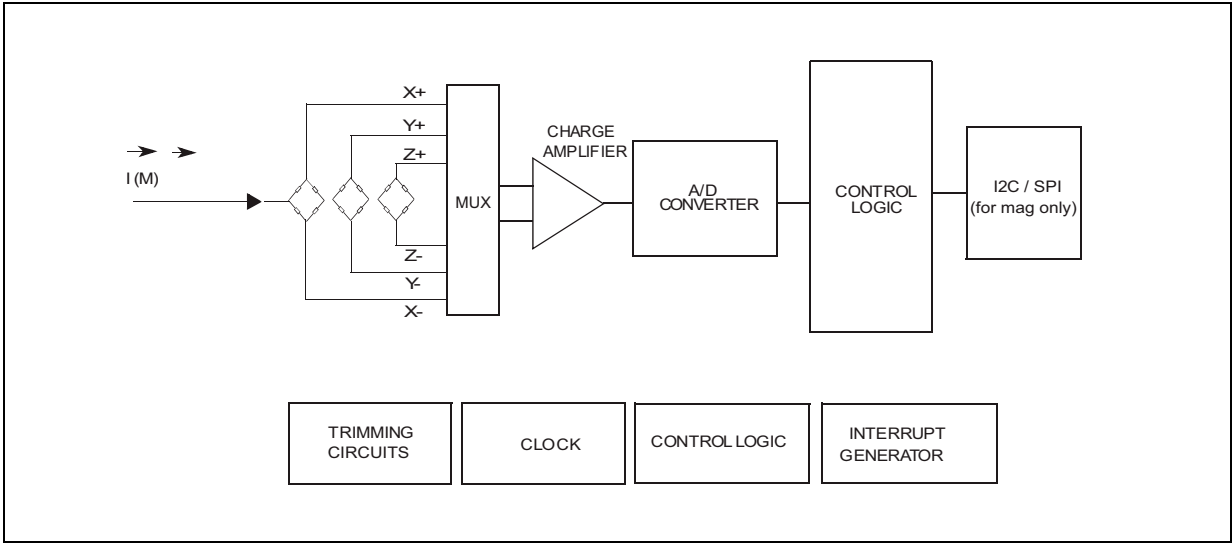


Figure 9. Magnetometer block diagram



### 3.5 Accelerometer and gyroscope FIFO

The LSM9DS1 embeds 32 slots of 16-bit data FIFO for each of the gyroscope's three output channels, yaw, pitch and roll, and 16-bit data FIFO for each of the accelerometer's three output channels, X, Y and Z. This allows consistent power saving for the system since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly to five different modes: Bypass mode, FIFO-mode, Continuous mode, Continuous-to-FIFO mode and Bypass-to-Continuous. Each mode is selected by the FMODE [2:0] bits in the [FIFO\\_CTRL \(2Eh\)](#) register. Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the [FIFO\\_SRC \(2Fh\)](#) register and can be set to generate dedicated interrupts on the INT1\_A/G pin in the [INT1\\_CTRL \(0Ch\)](#) register and on the INT2\_A/G pin in the [INT2\\_CTRL \(0Dh\)](#) register.

[FIFO\\_SRC \(2Fh\)](#)(FTH) goes to '1' when the number of unread samples ([FIFO\\_SRC \(2Fh\)](#) (FSS5:0)) is greater than or equal to FTH [4:0] in [FIFO\\_CTRL \(2Eh\)](#). If [FIFO\\_CTRL \(2Eh\)](#) (FTH[4:0]) is equal to 0, [FIFO\\_SRC \(2Fh\)](#)(FTH) goes to '0'.

[FIFO\\_SRC \(2Fh\)](#)(OVRN) is equal to '1' if a FIFO slot is overwritten.

[FIFO\\_SRC \(2Fh\)](#)(FSS [5:0]) contains stored data levels of unread samples. When FSS [5:0] is equal to '000000' FIFO is empty, when FSS [5:0] is equal to '100000' FIFO is full and the unread samples are 32.

The FIFO feature is enabled by writing '1' in [CTRL\\_REG9 \(23h\)](#) (FIFO\_EN).

To guarantee the correct acquisition of data during the switching into and out of FIFO mode, the first sample acquired must be discarded.

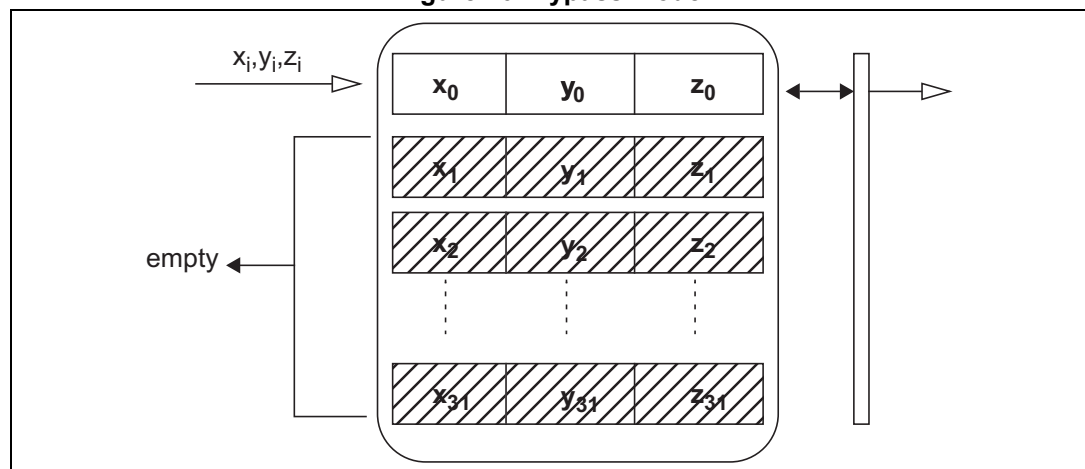
#### 3.5.1 Bypass mode

In Bypass mode ([FIFO\\_CTRL \(2Eh\)](#)(FMODE [2:0]= 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO mode.

As described in [Figure 10](#), for each channel only the first address is used. When new data is available the old data is overwritten.

**Figure 10. Bypass mode**



### 3.5.2 FIFO mode

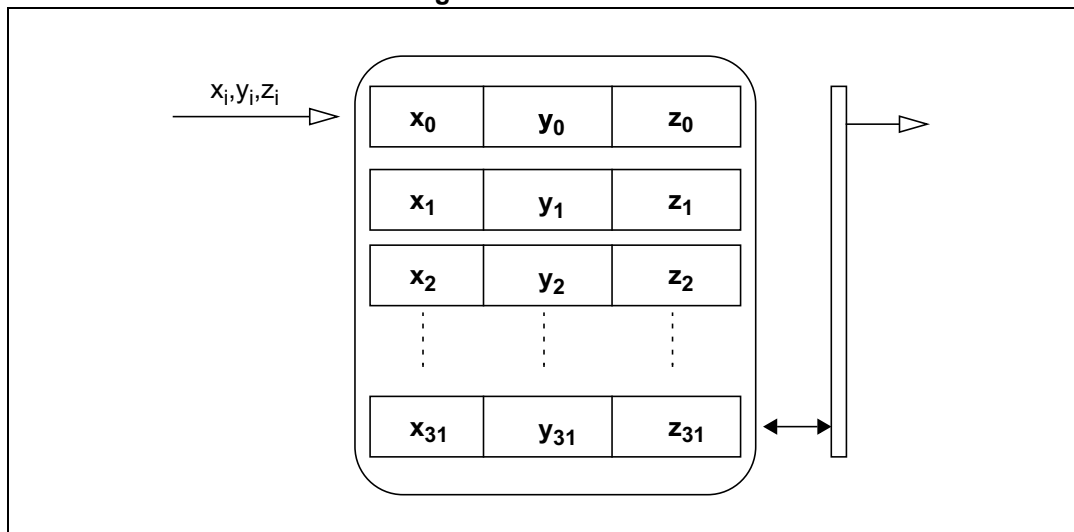
In FIFO mode (*FIFO\_CTRL (2Eh)* (FMODE [2:0] = 001) data from the output channels are stored in the FIFO until it is overwritten.

To reset FIFO content, Bypass mode should be selected by writing *FIFO\_CTRL (2Eh)* (FMODE [2:0]) to '000'. After this reset command, it is possible to restart FIFO mode by writing *FIFO\_CTRL (2Eh)* (FMODE [2:0]) to '001'.

The FIFO buffer memorizes 32 levels of data but the depth of the FIFO can be resized by setting the STOP\_ON\_FTH bit in *CTRL\_REG9 (23h)*. If the STOP\_ON\_FTH bit is set to '1', FIFO depth is limited to *FIFO\_CTRL (2Eh)*(FTH [4:0]) + 1 data.

A FIFO threshold interrupt can be enabled (INT\_OVR bit in *INT1\_CTRL (0Ch)* ) in order to be raised when the FIFO is filled to the level specified by the FTH[4:0] bits of *FIFO\_CTRL (2Eh)*. When a FIFO threshold interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

Figure 11. FIFO mode



### 3.5.3 Continuous mode

Continuous mode (*FIFO\_CTRL (2Eh)*(FMODE[2:0] = 110) provides continuous FIFO update: as new data arrives the older is discarded.

A FIFO threshold flag *FIFO\_SRC (2Fh)*(FTH) is asserted when the number of unread samples in FIFO is greater than or equal to *FIFO\_CTRL (2Eh)*(FTH4:0).

It is possible to route *FIFO\_SRC (2Fh)*(FTH) to the INT1\_A/G pin by writing in register *INT1\_CTRL (0Ch)* (INT1\_FTH) = '1', or to the INT2\_A/G pin by writing in register *INT2\_CTRL (0Dh)* (INT2\_FTH) = '1'.

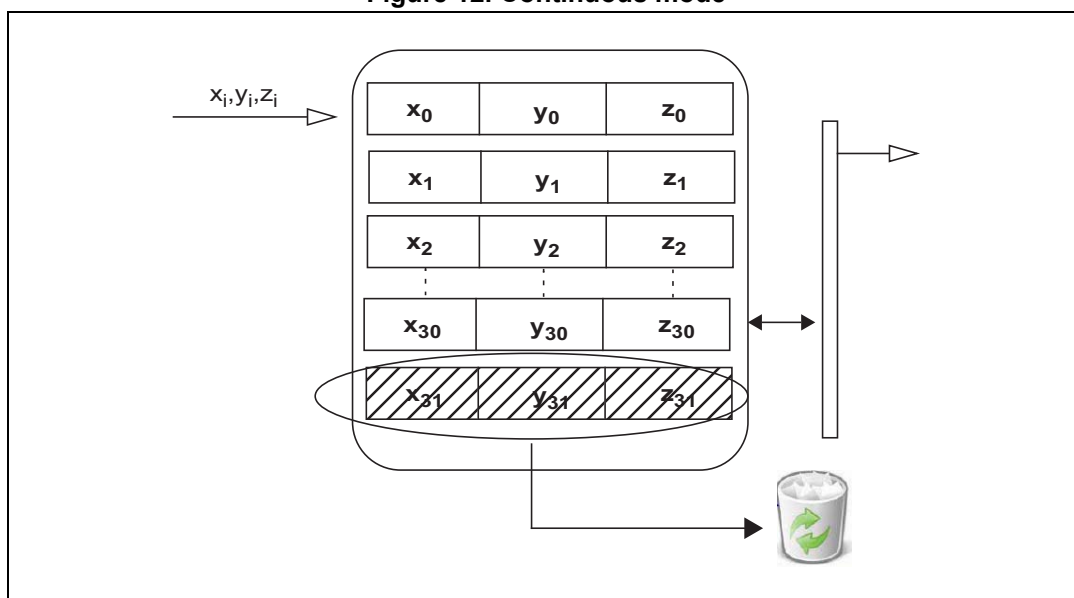
A full-flag interrupt can be enabled, (*INT1\_CTRL (0Ch)* (INT\_FSS5) = '1') when the FIFO becomes saturated and in order to read the contents all at once.

If an overrun occurs, the oldest sample in FIFO is overwritten and the OVRN flag in *FIFO\_SRC (2Fh)* is asserted.

In order to empty the FIFO before it is full it is also possible to pull from FIFO the number of unread samples available in *FIFO\_SRC (2Fh)* (FSS[5:0]).



Figure 12. Continuous mode



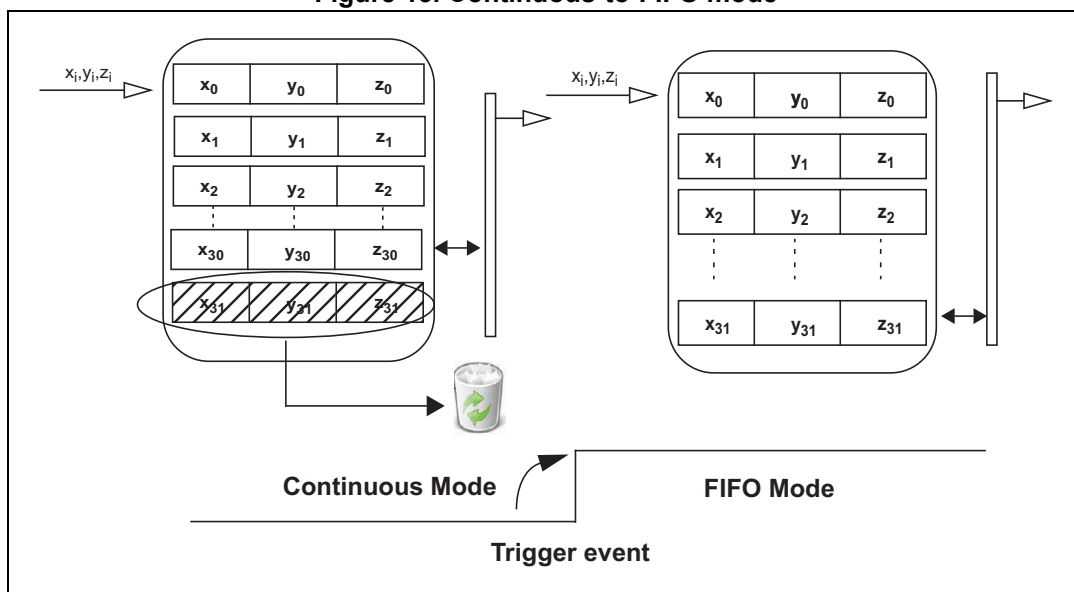
### 3.5.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode (*FIFO\_CTRL* (2Eh)(FMODE [2:0] = 011), FIFO behavior changes according to the *INT\_GEN\_SRC\_XL* (26h)(IA\_XL) bit. When the *INT\_GEN\_SRC\_XL* (26h)(IA\_XL) bit is equal to '1', FIFO operates in FIFO-mode, when the *INT\_GEN\_SRC\_XL* (26h)(IA\_XL) bit is equal to '0', FIFO operates in Continuous mode.

The interrupt generator should be set to the desired configuration by means of *INT\_GEN\_CFG\_XL* (06h), *INT\_GEN\_THS\_X\_XL* (07h), *INT\_GEN\_THS\_Y\_XL* (08h) and *INT\_GEN\_THS\_Z\_XL* (09h).

The *CTRL\_REG4* (1Eh)(LIR\_XL) bit should be set to '1' in order to have latched interrupt.

Figure 13. Continuous-to-FIFO mode



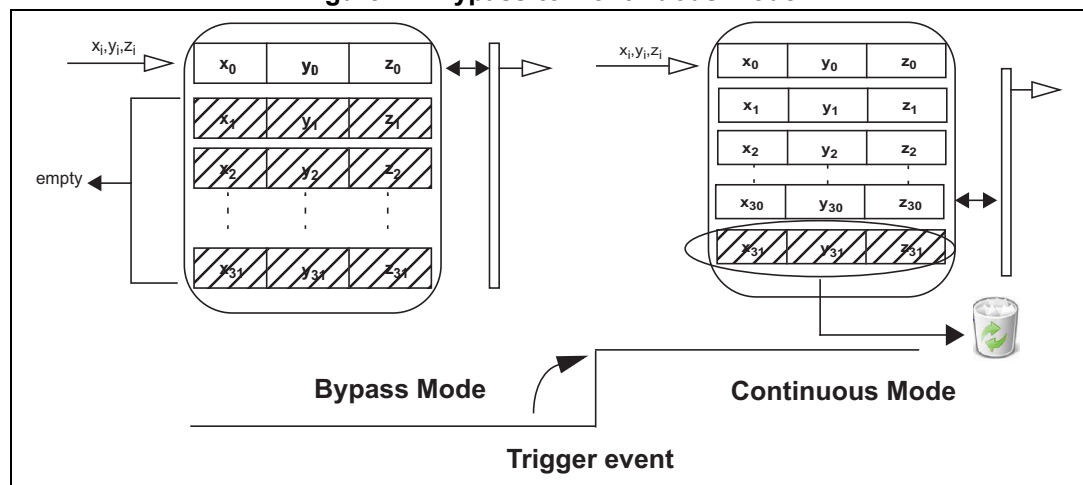
### 3.5.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (*FIFO\_CTRL (2Eh)*(FMODE[2:0] = '100'), data measurement storage inside FIFO operates in Continuous mode when *INT\_GEN\_SRC\_XL (26h)*(IA\_XL) is equal to '1', otherwise FIFO content is reset (Bypass mode).

The interrupt generator should be set to the desired configuration by means of *INT\_GEN\_CFG\_XL (06h)*, *INT\_GEN\_THS\_X\_XL (07h)*, *INT\_GEN\_THS\_Y\_XL (08h)* and *INT\_GEN\_THS\_Z\_XL (09h)*.

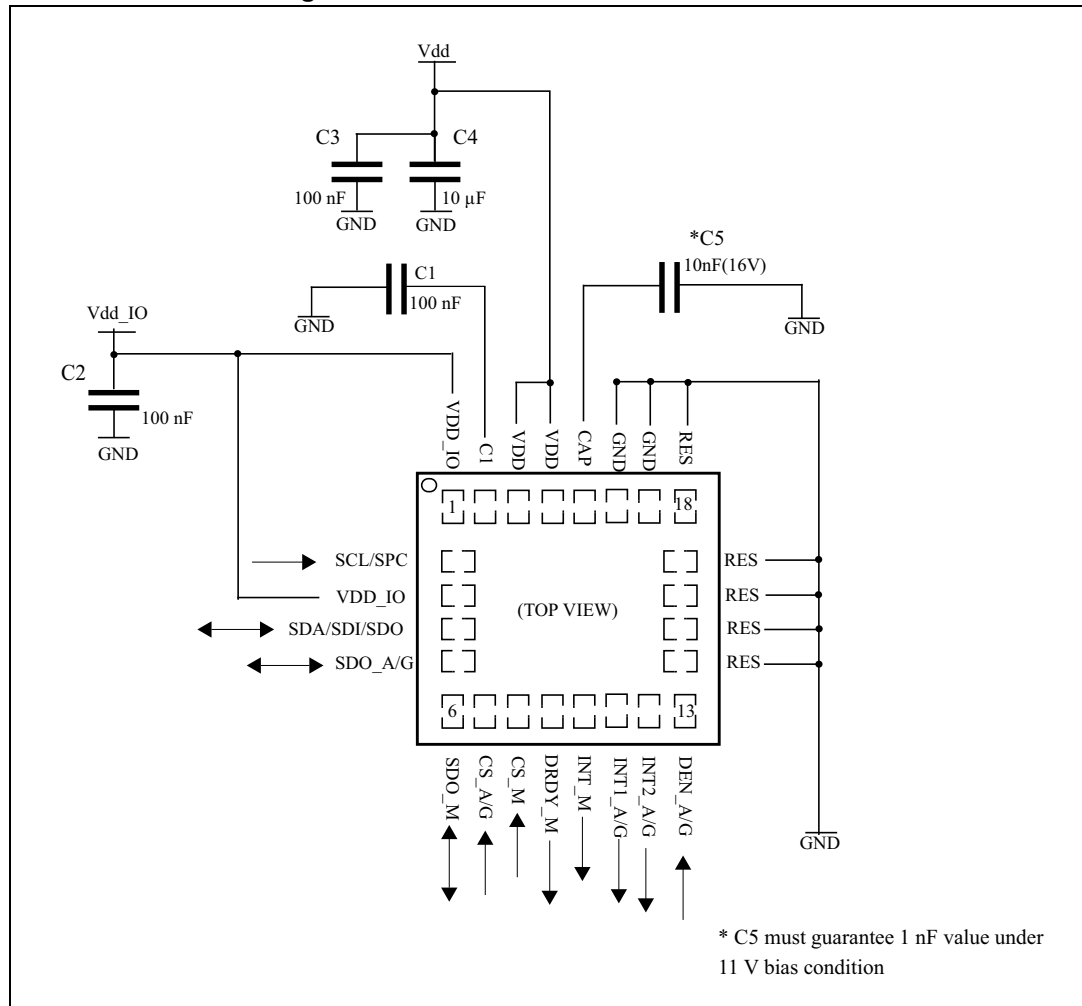
The *CTRL\_REG4 (1Eh)*(LIR\_XL) bit should be set to '1' in order to have latched interrupt.

**Figure 14. Bypass-to-Continuous mode**



## 4 Application hints

**Figure 15. LSM9DS1 electrical connections**



## 4.1 External capacitors

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C2, C3 = 100 nF ceramic, C4 = 10  $\mu$ F Al) should be placed as near as possible to the supply pin of the device (common design practice). Capacitor C1 (100 nF) should be a capacitor with low ESR value and should be placed as near as possible to the C1 pin.

All voltage and ground supplies must be present at the same time to achieve proper behavior of the IC (refer to [Figure 15](#)).

## 5 Digital interfaces

The registers embedded inside the LSM9DS1 may be accessed through both the I<sup>2</sup>C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I<sup>2</sup>C interface, the CS line must be tied high (i.e connected to Vdd\_IO).

**Table 13. Serial interface pin description**

| Pin name       | Pin description  |
|----------------|--|
| CS_A/G, CS_M   | SPI enable<br>I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled) |
| SCL/SPC        | I <sup>2</sup> C Serial Clock (SCL)<br>SPI Serial Port Clock (SPC)   |
| SDA/SDI/SDO    | I <sup>2</sup> C Serial Data (SDA)<br>SPI Serial Data Input (SDI)<br>3-wire Interface Serial Data Output (SDO)   |
| SDO_A/G, SDO_M | SPI Serial Data Output (SDO)<br>I <sup>2</sup> C less significant bit of the device address  |

### 5.1 I<sup>2</sup>C serial interface

The LSM9DS1 I<sup>2</sup>C is a bus slave. The I<sup>2</sup>C is employed to write the data to the registers, whose content can also be read back.

The relevant I<sup>2</sup>C terminology is provided in the table below.

**Table 14. I<sup>2</sup>C terminology**

| Term        | Description  |
|-------------|--|
| Transmitter | The device which sends data to the bus   |
| Receiver    | The device which receives data from the bus  |
| Master      | The device which initiates a transfer, generates clock signals and terminates a transfer |
| Slave       | The device addressed by the master   |

There are two signals associated with the I<sup>2</sup>C bus: the serial clock line (SCL) and the Serial Data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd\_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I<sup>2</sup>C interface is implemented with fast mode (400 kHz) I<sup>2</sup>C standards as well as with the standard mode.

In order to disable the I<sup>2</sup>C block for accelerometer and gyroscope the I2C\_DISABLE bit must be written to '1' in [CTRL\\_REG9 \(23h\)](#), while for magnetometer the I2C\_DISABLE bit must be written to '1' in [CTRL\\_REG3\\_M \(22h\)](#).

### 5.1.1 I<sup>2</sup>C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I<sup>2</sup>C embedded inside the LSM9DS1 behaves like a slave device and the following protocol must be adhered to. In the I<sup>2</sup>C of the accelerometer and gyroscope sensor, after the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The 7 LSb represent the actual register address while the [CTRL\\_REG8 \(22h\)](#) (IF\_ADD\_INC) bit defines the address increment. In the I<sup>2</sup>C of the magnetometer sensor, after the START condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted. The 7 LSb represent the actual register address while the MSB enables the address auto increment. The SUB (register address) is automatically increased to allow multiple data read/write.

**Table 15. Transfer when master is writing one byte to slave**

|        |    |         |     |     |     |      |     |    |
|--------|----|---------|-----|-----|-----|------|-----|----|
| Master | ST | SAD + W |     | SUB |     | DATA |     | SP |
| Slave  |    |         | SAK |     | SAK |      | SAK |    |

**Table 16. Transfer when master is writing multiple bytes to slave**

|        |    |         |     |     |     |      |     |      |     |    |
|--------|----|---------|-----|-----|-----|------|-----|------|-----|----|
| Master | ST | SAD + W |     | SUB |     | DATA |     | DATA |     | SP |
| Slave  |    |         | SAK |     | SAK |      | SAK |      | SAK |    |

**Table 17. Transfer when master is receiving (reading) one byte of data from slave**

|        |    |         |     |     |     |    |         |     |      |      |    |
|--------|----|---------|-----|-----|-----|----|---------|-----|------|------|----|
| Master | ST | SAD + W |     | SUB |     | SR | SAD + R |     |      | NMAK | SP |
| Slave  |    |         | SAK |     | SAK |    |         | SAK | DATA |      |    |

**Table 18. Transfer when master is receiving (reading) multiple bytes of data from slave**

|        |    |       |     |     |     |    |       |     |      |     |      |     |      |      |    |
|--------|----|-------|-----|-----|-----|----|-------|-----|------|-----|------|-----|------|------|----|
| Master | ST | SAD+W |     | SUB |     | SR | SAD+R |     |      | MAK |      | MAK |      | NMAK | SP |
| Slave  |    |       | SAK |     | SAK |    |       | SAK | DATA |     | DATA |     | DATA |      |    |

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed

some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

#### Default address:

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes. If the bit is '0' (Write) the master will transmit to the slave with direction unchanged. [Table 19](#) and [Table 20](#) explain how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

**Table 19. Accelerometer and gyroscope SAD+Read/Write patterns**

| Command | SAD[6:1] | SAD[0] = SA0 | R/W | SAD+R/W        |
|---------|----------|--------------|-----|----------------|
| Read    | 110101   | 0            | 1   | 11010101 (D5h) |
| Write   | 110101   | 0            | 0   | 11010100 (D4h) |
| Read    | 110101   | 1            | 1   | 11010111 (D7h) |
| Write   | 110101   | 1            | 0   | 11010110 (D6h) |

**Table 20. Magnetic sensor SAD+Read/Write patterns**

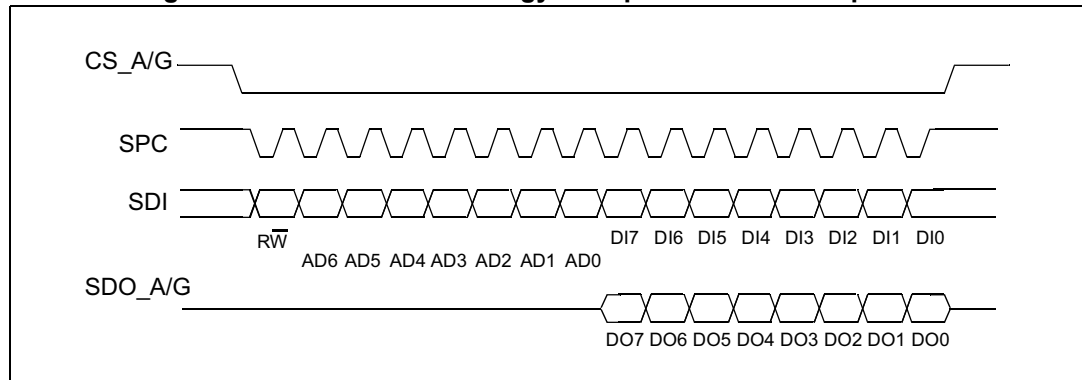
| Command | SAD[6:2] | SAD[1] = SDO/SA1 | SAD[0] | R/W | SAD+R/W        |
|---------|----------|------------------|--------|-----|----------------|
| Read    | 00111    | 0                | 0      | 1   | 00111001 (39h) |
| Write   | 00111    | 0                | 0      | 0   | 00111000 (38h) |
| Read    | 00111    | 1                | 0      | 1   | 00111101 (3Dh) |
| Write   | 00111    | 1                | 0      | 0   | 00111100 (3Ch) |

## 5.2 Accelerometer and gyroscope SPI bus interface

The LSM9DS1 accelerometer and gyroscope SPI is a bus slave. The SPI allows to write and read the registers of the device.

The Serial Interface connects to applications using 4 wires: **CS\_A/G**, **SPC**, **SDI** and **SDO\_A/G**.

**Figure 16. Accelerometer and gyroscope read and write protocol**



**CS\_A/G** is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS\_A/G** is high (no transmission). **SDI** and **SDO\_A/G** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS\_A/G** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS\_A/G**.

**bit 0:**  $\overline{RW}$  bit. When 0, the data **DI(7:0)** is written into the device. When 1, the data **DO(7:0)** from the device is read. In latter case, the chip will drive **SDO\_A/G** at the start of bit 8.

**bit 1-7:** address **AD(6:0)**. This is the address field of the indexed register.

**bit 8-15:** data **DI(7:0)** (write mode). This is the data that is written into the device (MSb first).

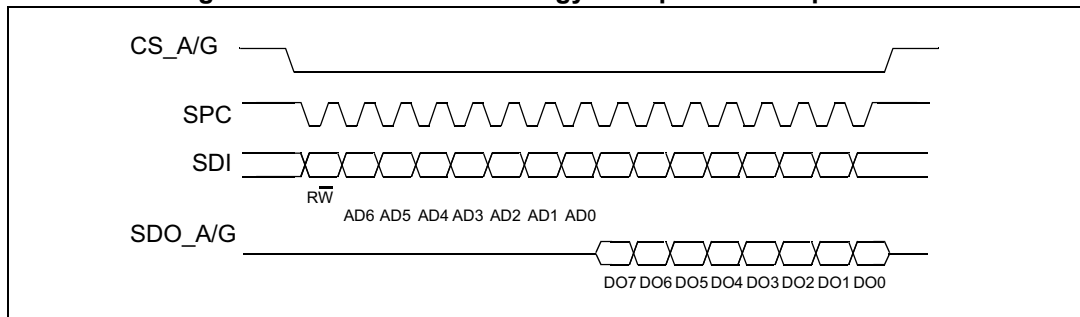
**bit 8-15:** data **DO(7:0)** (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the [CTRL\\_REG8 \(22h\)](#) (**IF\_ADD\_INC**) bit is '0' the address used to read/write data remains the same for every block. When the [CTRL\\_REG8 \(22h\)](#) (**IF\_ADD\_INC**) bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO\_A/G** remain unchanged.

### 5.2.1 SPI read

**Figure 17. Accelerometer and gyroscope SPI read protocol**



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

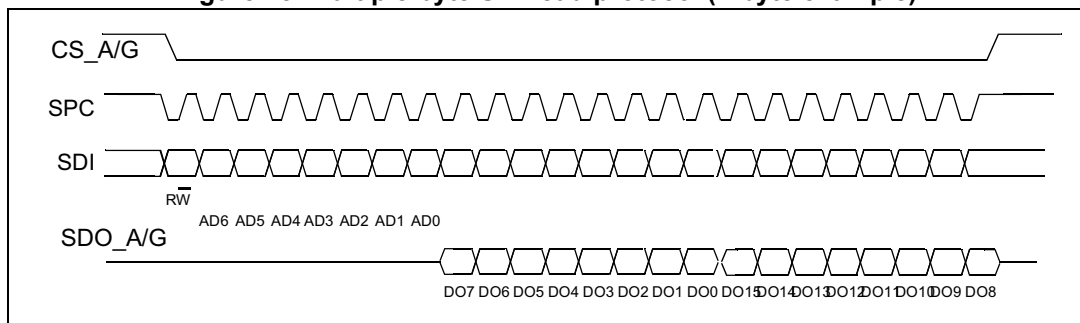
**bit 0:** READ bit. The value is 1.

**bit 1-7:** address  $AD[6:0]$ . This is the address field of the indexed register.

**bit 8-15:** data  $DO[7:0]$  (read mode). This is the data that will be read from the device (MSb first).

**bit 16-...** : data  $DO[...-8]$ . Further data in multiple byte reads.

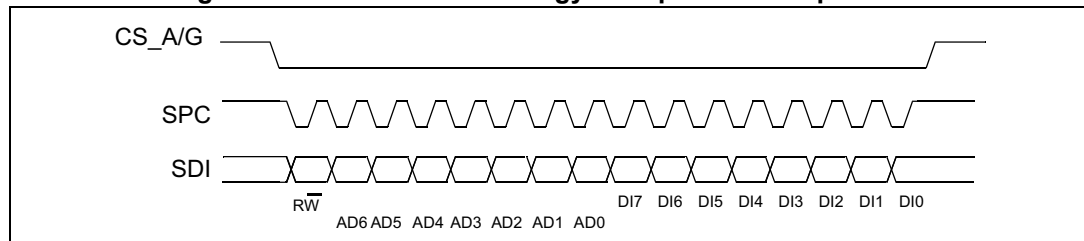
**Figure 18. Multiple byte SPI read protocol (2-byte example)**





### 5.2.2 SPI write

**Figure 19. Accelerometer and gyroscope SPI write protocol**



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

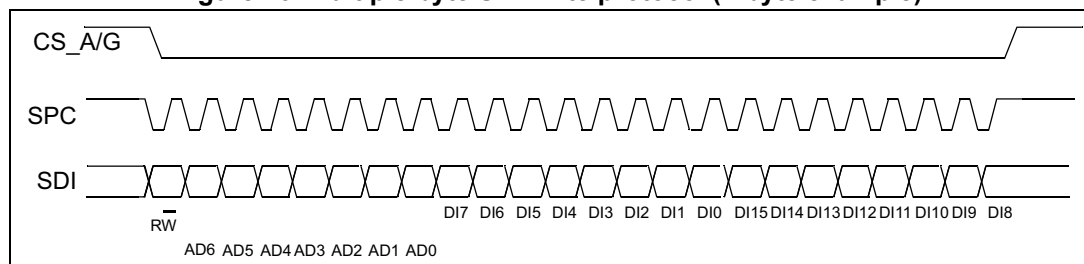
**bit 0:** WRITE bit. The value is 0.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

**bit 16-...** : data DI(...-8). Further data in multiple byte writes.

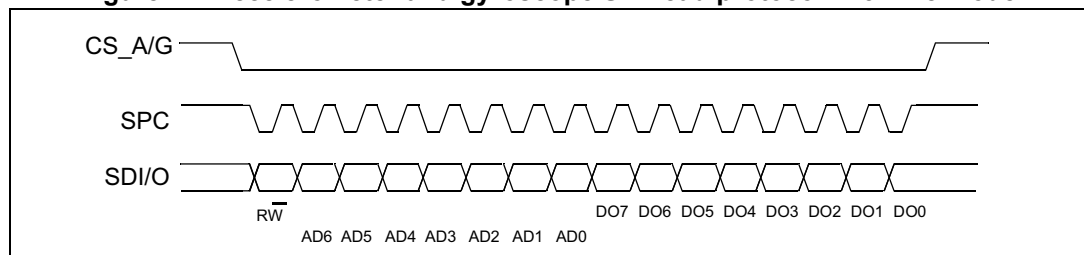
**Figure 20. Multiple byte SPI write protocol (2-byte example)**



### 5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the [CTRL\\_REG8 \(22h\)](#)(SIM) bit equal to '1' (SPI serial interface mode selection).

**Figure 21. Accelerometer and gyroscope SPI read protocol in 3-wire mode**



The SPI read command is performed with 16 clock pulses:

**bit 0:** READ bit. The value is 1.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

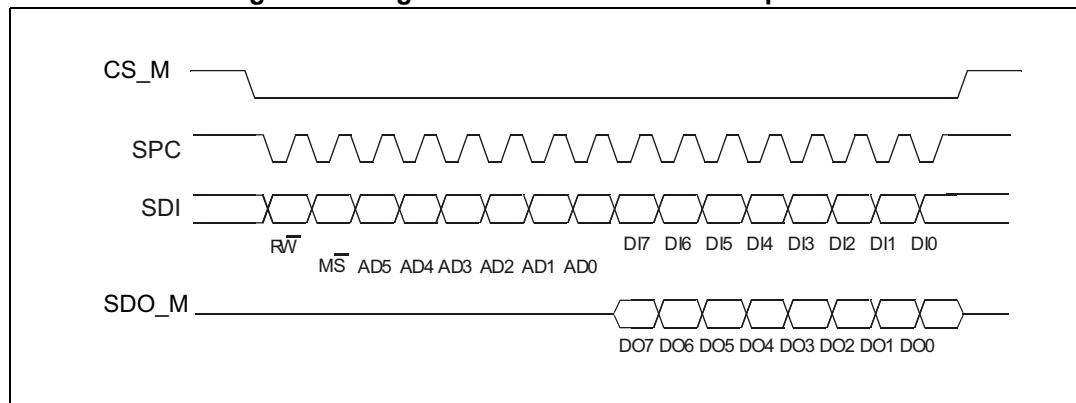
A multiple read command is also available in 3-wire mode.

### 5.3 Magnetic sensor SPI bus interface

The LSM9DS1 magnetic sensor SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface connects to applications using 4 wires: **CS\_M**, **SPC**, **SDI** and **SDO\_M**.

**Figure 22. Magnetic sensor read and write protocol**



**CS\_M** is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS\_M** is high (no transmission). **SDI** and **SDO\_M** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS\_M** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS\_M**.

**bit 0:**  $\overline{RW}$  bit. When 0, the data **DI(7:0)** is written into the device. When 1, the data **DO(7:0)** from the device is read. In latter case, the chip will drive **SDO\_M** at the start of bit 8.

**bit 1:**  $\overline{MS}$  bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

**bit 2-7:** address **AD(5:0)**. This is the address field of the indexed register.

**bit 8-15:** data **DI(7:0)** (write mode). This is the data that is written into the device (MSb first).

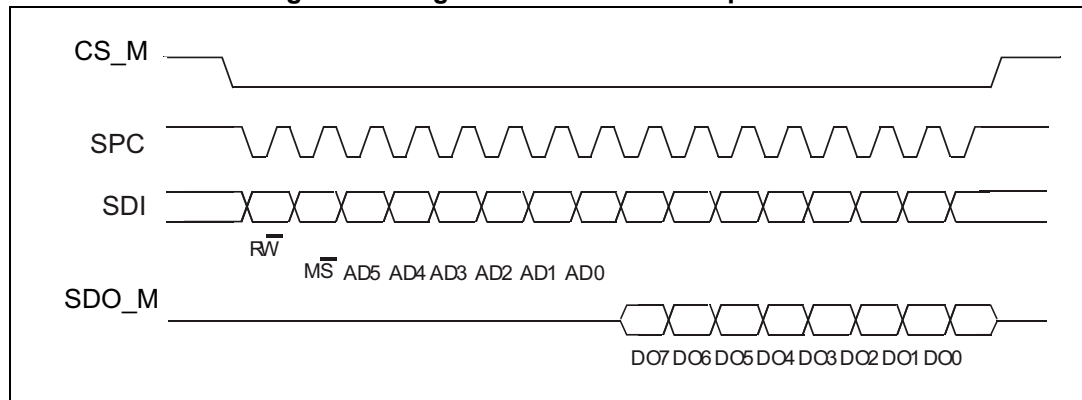
**bit 8-15:** data **DO(7:0)** (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the  $\overline{MS}$  bit is '0', the address used to read/write data remains the same for every block. When the  $\overline{MS}$  bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO\_M** remain unchanged.

### 5.3.1 SPI read

Figure 23. Magnetic sensor SPI read protocol



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

**bit 0:** READ bit. The value is 1.

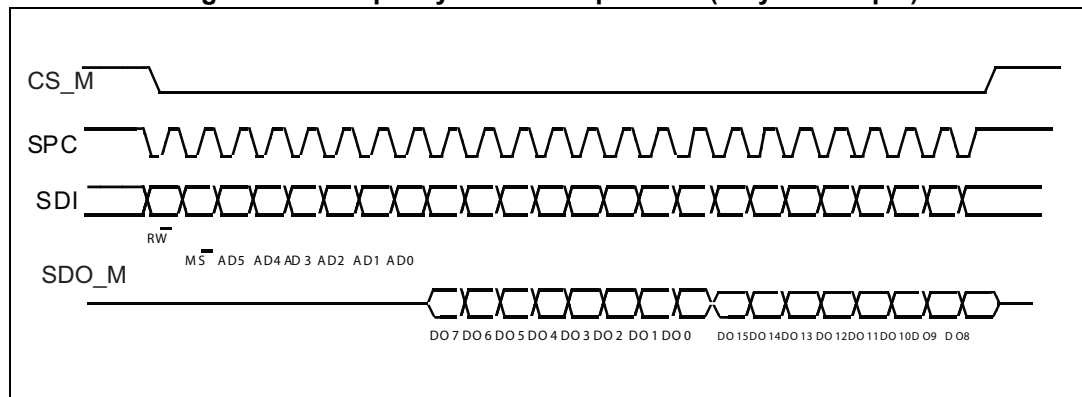
**bit 1:**  $\overline{MS}$  bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

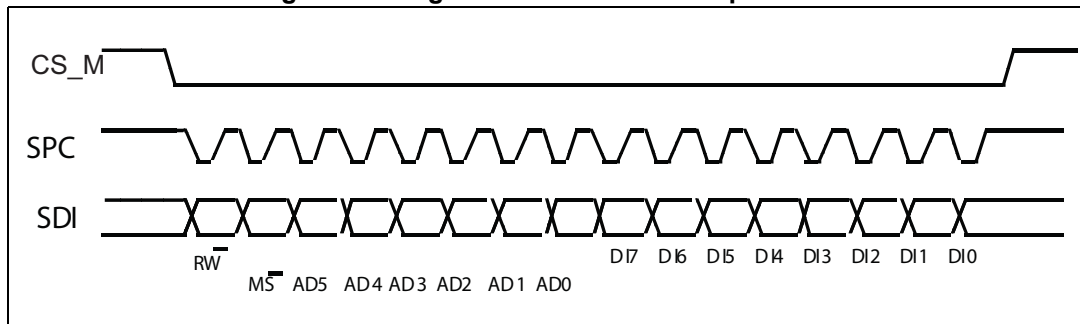
**bit 16-...** : data DO(...-8). Further data in multiple byte reads.

Figure 24. Multiple byte SPI read protocol (2-byte example)



### 5.3.2 SPI write

Figure 25. Magnetic sensor SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

**bit 0:** WRITE bit. The value is 0.

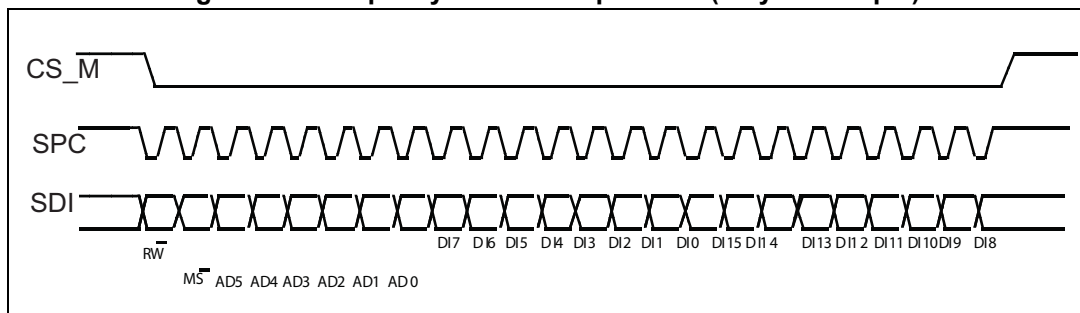
**bit 1:**  $\overline{MS}$  bit. When 0, does not increment the address; when 1, increments the address in multiple writes.

**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

**bit 16-...** : data DI(...-8). Further data in multiple byte writes.

Figure 26. Multiple byte SPI write protocol (2-byte example)

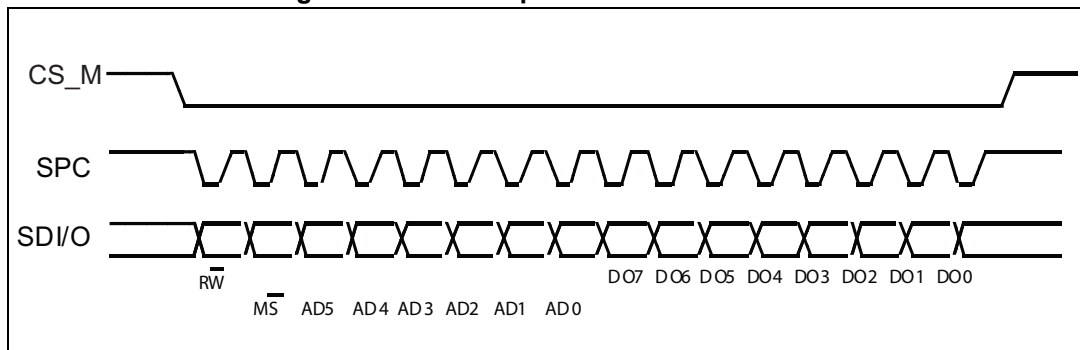


### 5.3.3 SPI read in 3-wire mode

3-wire mode is entered by setting the SIM bit to '1' (SPI serial interface mode selection) in [CTRL\\_REG3\\_M \(22h\)](#).

When 3-wire mode is used, the SDO\_M pin has to be connected to GND or Vdd\_IO.

**Figure 27. SPI read protocol in 3-wire mode**



The SPI read command is performed with 16 clock pulses:

**bit 0:** READ bit. The value is 1.

**bit 1:**  $\overline{MS}$  bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

## 6 Register mapping

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

**Table 21. Accelerometer and gyroscope register address map**

| Name             | Type | Register address |          | Default  | Note     |
|------------------|------|------------------|----------|----------|----------|
|                  |      | Hex              | Binary   |          |          |
| Reserved         | --   | 00-03            | --       | --       | Reserved |
| ACT_THS          | r/w  | 04               | 00000100 | 00000000 |          |
| ACT_DUR          | r/w  | 05               | 00000101 | 00000000 |          |
| INT_GEN_CFG_XL   | r/w  | 06               | 00000110 | 00000000 |          |
| INT_GEN_THS_X_XL | r/w  | 07               | 00000111 | 00000000 |          |
| INT_GEN_THS_Y_XL | r/w  | 08               | 00001000 | 00000000 |          |
| INT_GEN_THS_Z_XL | r/w  | 09               | 00001001 | 00000000 |          |
| INT_GEN_DUR_XL   | r/w  | 0A               | 00001010 | 00000000 |          |
| REFERENCE_G      | r/w  | 0B               | 00001011 | 00000000 |          |
| INT1_CTRL        | r/w  | 0C               | 00001100 | 00000000 |          |
| INT2_CTRL        | r/w  | 0D               | 00001101 | 00000000 |          |
| Reserved         | --   | 0E               | --       | --       | Reserved |
| WHO_AM_I         | r    | 0F               | 00001111 | 01101000 |          |
| CTRL_REG1_G      | r/w  | 10               | 00010000 | 00000000 |          |
| CTRL_REG2_G      | r/w  | 11               | 00010001 | 00000000 |          |
| CTRL_REG3_G      | r/w  | 12               | 00010010 | 00000000 |          |
| ORIENT_CFG_G     | r/w  | 13               | 00010011 | 00000000 |          |
| INT_GEN_SRC_G    | r    | 14               | 00010100 | output   |          |
| OUT_TEMP_L       | r    | 15               | 00010101 | output   |          |
| OUT_TEMP_H       | r    | 16               | 00010110 | output   |          |
| STATUS_REG       | r    | 17               | 00010111 | output   |          |
| OUT_X_L_G        | r    | 18               | 00011000 | output   |          |
| OUT_X_H_G        | r    | 19               | 00011001 | output   |          |
| OUT_Y_L_G        | r    | 1A               | 00011010 | output   |          |
| OUT_Y_H_G        | r    | 1B               | 00011011 | output   |          |
| OUT_Z_L_G        | r    | 1C               | 00011100 | output   |          |
| OUT_Z_H_G        | r    | 1D               | 00011101 | output   |          |
| CTRL_REG4        | r/w  | 1E               | 00011110 | 00111000 |          |
| CTRL_REG5_XL     | r/w  | 1F               | 00011111 | 00111000 |          |

Table 21. Accelerometer and gyroscope register address map (continued)

| Name             | Type | Register address |          | Default  | Note     |
|------------------|------|------------------|----------|----------|----------|
|                  |      | Hex              | Binary   |          |          |
| CTRL_REG6_XL     | r/w  | 20               | 00100000 | 00000000 |          |
| CTRL_REG7_XL     | r/w  | 21               | 00100001 | 00000000 |          |
| CTRL_REG8        | r/w  | 22               | 00100010 | 00000100 |          |
| CTRL_REG9        | r/w  | 23               | 00100011 | 00000000 |          |
| CTRL_REG10       | r/w  | 24               | 00100100 | 00000000 |          |
| Reserved         | --   | 25               | --       | --       | Reserved |
| INT_GEN_SRC_XL   | r    | 26               | 00100110 | output   |          |
| STATUS_REG       | r    | 27               | 00100111 | output   |          |
| OUT_X_L_XL       | r    | 28               | 00101000 | output   |          |
| OUT_X_H_XL       | r    | 29               | 00101001 | output   |          |
| OUT_Y_L_XL       | r    | 2A               | 00101010 | output   |          |
| OUT_Y_H_XL       | r    | 2B               | 00101011 | output   |          |
| OUT_Z_L_XL       | r    | 2C               | 00101100 | output   |          |
| OUT_Z_H_XL       | r    | 2D               | 00101101 | output   |          |
| FIFO_CTRL        | r/w  | 2E               | 00101110 | 00000000 |          |
| FIFO_SRC         | r    | 2F               | 00101111 | output   |          |
| INT_GEN_CFG_G    | r/w  | 30               | 00110000 | 00000000 |          |
| INT_GEN_THS_XH_G | r/w  | 31               | 00110001 | 00000000 |          |
| INT_GEN_THS_XL_G | r/w  | 32               | 00110010 | 00000000 |          |
| INT_GEN_THS_YH_G | r/w  | 33               | 00110011 | 00000000 |          |
| INT_GEN_THS_YL_G | r/w  | 34               | 00110100 | 00000000 |          |
| INT_GEN_THS_ZH_G | r/w  | 35               | 00110101 | 00000000 |          |
| INT_GEN_THS_ZL_G | r/w  | 36               | 00110110 | 00000000 |          |
| INT_GEN_DUR_G    | r/w  | 37               | 00110111 | 00000000 |          |
| Reserved         | r    | 38-7F            | --       | --       | Reserved |

Table 22. Magnetic sensor register address map

| Name             | Type | Register address |           | Default  | Comment   |
|------------------|------|------------------|-----------|----------|---|
|                  |      | Hex              | Binary    |          |   |
| Reserved         |      | 00 - 04          | --        | --       | Reserved  |
| OFFSET_X_REG_L_M | r/w  | 05               |           | 00000000 | Offset in order to compensate environmental effects |
| OFFSET_X_REG_H_M | r/w  | 06               |           | 00000000 |   |
| OFFSET_Y_REG_L_M | r/w  | 07               |           | 00000000 |   |
| OFFSET_Y_REG_H_M | r/w  | 08               |           | 00000000 |   |
| OFFSET_Z_REG_L_M | r/w  | 09               |           | 00000000 |   |
| OFFSET_Z_REG_H_M | r/w  | 0A               |           | 00000000 |   |
| Reserved         |      | 0B - 0E          | --        | --       | Reserved  |
| WHO_AM_I_M       | r    | 0F               | 0000 1111 | 00111101 | Magnetic Who I am ID                                |
| Reserved         |      | 10 - 1F          | --        | --       | Reserved  |
| CTRL_REG1_M      | r/w  | 20               | 0010 0000 | 00010000 | Magnetic control registers                          |
| CTRL_REG2_M      | r/w  | 21               | 0010 0001 | 00000000 |   |
| CTRL_REG3_M      | r/w  | 22               | 0010 0010 | 00000011 |   |
| CTRL_REG4_M      | r/w  | 23               | 0010 0011 | 00000000 |   |
| CTRL_REG5_M      | r/w  | 24               | 0010 0100 | 00000000 |   |
| Reserved         |      | 25 - 26          | --        | --       | Reserved  |
| STATUS_REG_M     | r    | 27               | 0010 0111 | Output   |   |
| OUT_X_L_M        | r    | 28               | 0010 1000 | Output   | Magnetic output registers                           |
| OUT_X_H_M        | r    | 29               | 0010 1001 | Output   |   |
| OUT_Y_L_M        | r    | 2A               | 0010 1010 | Output   |   |
| OUT_Y_H_M        | r    | 2B               | 0010 1011 | Output   |   |
| OUT_Z_L_M        | r    | 2C               | 0010 1100 | Output   |   |
| OUT_Z_H_M        | r    | 2D               | 0010 1101 | Output   |   |
| Reserved         | r    | 2E-2F            | --        | --       | Reserved  |
| INT_CFG_M        | rw   | 30               | 00110000  | 00001000 | Magnetic interrupt configuration register           |
| INT_SRC_M        | r    | 31               | 00110001  | 00000000 | Magnetic interrupt generator status register        |
| INT_THS_L_M      | r    | 32               | 00110010  | 00000000 | Magnetic interrupt generator threshold              |
| INT_THS_H_M      | r    | 33               | 00110011  | 00000000 |   |

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

To guarantee proper behavior of the device, all registers addresses not listed in the above table must not be accessed and the content stored on those registers must not be changed.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.



## 7 Accelerometer and gyroscope register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

### 7.1 ACT\_THS (04h)

Activity threshold register.

**Table 23. ACT\_THS register**

|                   |           |           |           |           |           |           |           |
|-------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| SLEEP_ON_INACT_EN | ACT_THS_6 | ACT_THS_5 | ACT_THS_4 | ACT_THS_3 | ACT_THS_2 | ACT_THS_1 | ACT_THS_0 |
|-------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|

**Table 24. ACT\_THS register description**

|                   |  |
|-------------------|--|
| SLEEP_ON_INACT_EN | Gyroscope operating mode during inactivity. Default value: 0<br>(0: gyroscope in power-down; 1: gyroscope in sleep mode) |
| ACT_THS [6:0]     | Inactivity threshold. Default value: 000 0000  |

### 7.2 ACT\_DUR (05h)

Inactivity duration register.

**Table 25. ACT\_DUR register**

|           |           |           |           |           |           |           |           |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| ACT_DUR_7 | ACT_DUR_6 | ACT_DUR_5 | ACT_DUR_4 | ACT_DUR_3 | ACT_DUR_2 | ACT_DUR_1 | ACT_DUR_0 |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|

**Table 26. ACT\_DUR register description**

|               |   |
|---------------|---|
| ACT_DUR [7:0] | Inactivity duration. Default value: 0000 0000 |
|---------------|---|

### 7.3 INT\_GEN\_CFG\_XL (06h)

Linear acceleration sensor interrupt generator configuration register.

**Table 27. INT\_GEN\_CFG\_XL register**

|        |    |         |         |         |         |         |         |
|--------|----|---------|---------|---------|---------|---------|---------|
| AOI_XL | 6D | ZHIE_XL | ZLIE_XL | YHIE_XL | YLIE_XL | XHIE_XL | XLIE_XL |
|--------|----|---------|---------|---------|---------|---------|---------|

**Table 28. INT\_GEN\_CFG\_XL register description**

|         |  |
|---------|--|
| AOI_XL  | AND/OR combination of accelerometer's interrupt events. Default value: 0<br>(0: OR combination; 1: AND combination)  |
| 6D      | 6-direction detection function for interrupt. Default value: 0<br>(0: disabled; 1: enabled)  |
| ZHIE_XL | Enable interrupt generation on accelerometer's Z-axis high event. Default value: 0<br>(0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold) |
| ZLIE_XL | Enable interrupt generation on accelerometer's Z-axis low event. Default value: 0<br>(0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)   |
| YHIE_XL | Enable interrupt generation on accelerometer's Y-axis high event. Default value: 0<br>(0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold) |
| YLIE_XL | Enable interrupt generation on accelerometer's Y-axis low event. Default value: 0<br>(0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)   |
| XHIE_XL | Enable interrupt generation on accelerometer's X-axis high event. Default value: 0<br>(0: disable interrupt request; 1: interrupt request on measured acceleration value higher than preset threshold) |
| XLIE_XL | Enable interrupt generation on accelerometer's X-axis low event. Default value: 0<br>(0: disable interrupt request; 1: interrupt request on measured acceleration value lower than preset threshold)   |

## 7.4 INT\_GEN\_THS\_X\_XL (07h)

Linear acceleration sensor interrupt threshold register.

**Table 29. INT\_GEN\_THS\_X\_XL register**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| THS_XL_<br>X7 | THS_XL_<br>X6 | THS_XL_<br>X5 | THS_XL_<br>X4 | THS_XL_<br>X3 | THS_XL_<br>X2 | THS_XL_<br>X1 | THS_XL_<br>X0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

**Table 30. INT\_GEN\_THS\_X\_XL register description**

|                |  |
|----------------|--|
| THS_XL_X [7:0] | X-axis interrupt threshold. Default value: 0000 0000 |
|----------------|--|

## 7.5 INT\_GEN\_THS\_Y\_XL (08h)

Linear acceleration sensor interrupt threshold register.

**Table 31. INT\_GEN\_THS\_Y\_XL register**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| THS_XL_<br>Y7 | THS_XL_<br>Y6 | THS_XL_<br>Y5 | THS_XL_<br>Y4 | THS_XL_<br>Y3 | THS_XL_<br>Y2 | THS_XL_<br>Y1 | THS_XL_<br>Y0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

**Table 32. INT\_GEN\_THS\_Y\_XL register description**

|                |  |
|----------------|--|
| THS_XL_Y [7:0] | Y-axis interrupt threshold. Default value: 0000 0000 |
|----------------|--|

## 7.6 INT\_GEN\_THS\_Z\_XL (09h)

Linear acceleration sensor interrupt threshold register.

**Table 33. INT\_GEN\_THS\_Z\_XL register**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| THS_XL_Z<br>7 | THS_XL_Z<br>6 | THS_XL_Z<br>5 | THS_XL_Z<br>4 | THS_XL_Z<br>3 | THS_XL_Z<br>2 | THS_XL_Z<br>1 | THS_XL_Z<br>0 |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|

**Table 34. INT\_GEN\_THS\_Z\_XL register description**

|                |  |
|----------------|--|
| THS_XL_Z [7:0] | Z-axis interrupt threshold. Default value: 0000 0000 |
|----------------|--|

## 7.7 INT\_GEN\_DUR\_XL (0Ah)

Linear acceleration sensor interrupt duration register.

**Table 35. INT\_GEN\_DUR\_XL register**

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| WAIT_XL | DUR_XL6 | DUR_XL5 | DUR_XL4 | DUR_XL3 | DUR_XL2 | DUR_XL1 | DUR_XL0 |
|---------|---------|---------|---------|---------|---------|---------|---------|

**Table 36. INT\_GEN\_DUR\_XL register description**

|              |  |
|--------------|--|
| WAIT_XL      | Wait function enabled on duration counter. Default value: 0<br>(0: wait function off; 1: wait for DUR_XL [6:0] samples before exiting interrupt) |
| DUR_XL [6:0] | Enter/exit interrupt duration value. Default value: 000 0000   |

## 7.8 REFERENCE\_G (0Bh)

Angular rate sensor reference value register for digital high-pass filter (r/w).

**Table 37. REFERENCE\_G register**

|        |        |        |        |        |        |        |        |
|--------|--------|--------|--------|--------|--------|--------|--------|
| REF7_G | REF6_G | REF5_G | REF4_G | REF3_G | REF2_G | REF1_G | REF0_G |
|--------|--------|--------|--------|--------|--------|--------|--------|

**Table 38. REFERENCE\_G register description**

|             |   |
|-------------|---|
| REF_G [7:0] | Reference value for gyroscope's digital high-pass filter (r/w).<br>Default value: 0000 0000 |
|-------------|---|

## 7.9 INT1\_CTRL (0Ch)

INT1\_A/G pin control register.

**Table 39. INT1\_CTRL register**

|           |            |           |          |          |           |             |              |
|-----------|------------|-----------|----------|----------|-----------|-------------|--------------|
| INT1_IG_G | INT1_IG_XL | INT1_FSS5 | INT1_OVR | INT1_FTH | INT1_Boot | INT1_DRDY_G | INT1_DRDY_XL |
|-----------|------------|-----------|----------|----------|-----------|-------------|--------------|

**Table 40. INT1\_CTRL register description**

|             |   |
|-------------|---|
| INT1_IG_G   | Gyroscope interrupt enable on INT 1_A/G pin. Default value: 0<br>(0: disabled; 1: enabled)        |
| INT_IG_XL   | Accelerometer interrupt generator on INT 1_A/G pin. Default value: 0<br>(0: disabled; 1: enabled) |
| INT_FSS5    | FSS5 interrupt enable on INT 1_A/G pin. Default value: 0<br>(0: disabled; 1: enabled)             |
| INT_OVR     | Overflow interrupt on INT 1_A/G pin. Default value: 0<br>(0: disabled; 1: enabled)                |
| INT_FTH     | FIFO threshold interrupt on INT 1_A/G pin. Default value: 0<br>(0: disabled; 1: enabled)          |
| INT_Boot    | Boot status available on INT 1_A/G pin. Default value: 0<br>(0: disabled; 1: enabled)             |
| INT_DRDY_G  | Gyroscope data ready on INT 1_A/G pin. Default value: 0<br>(0: disabled; 1: enabled)              |
| INT_DRDY_XL | Accelerometer data ready on INT 1_A/G pin. Default value: 0<br>(0: disabled; 1: enabled)          |

## 7.10 INT2\_CTRL (0Dh)

INT2\_A/G pin control register.

**Table 41. INT2\_CTRL register**

|                |   |               |          |          |                        |                 |                  |
|----------------|---|---------------|----------|----------|------------------------|-----------------|------------------|
| INT2_IN<br>ACT | 0 | INT2_<br>FSS5 | INT2_OVR | INT2_FTH | INT2_<br>DRDY_<br>TEMP | INT2_<br>DRDY_G | INT2_<br>DRDY_XL |
|----------------|---|---------------|----------|----------|------------------------|-----------------|------------------|

**Table 42. INT2\_CTRL register description**

|                    |   |
|--------------------|---|
| INT2_INACT         | Inactivity interrupt output signal. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupt events have been generated) |
| INT2_FSS5          | FSS5 interrupt enable on INT2_A/G pin. Default value: 0<br>(0: disabled; 1: enabled)  |
| INT2_OVR           | Overflow interrupt on INT2_A/G pin. Default value: 0<br>(0: disabled; 1: enabled)   |
| INT2_FTH           | FIFO threshold interrupt on INT2_A/G pin. Default value: 0<br>(0: disabled; 1: enabled)   |
| INT2_<br>DRDY_TEMP | Temperature data ready on INT2_A/G pin. Default value: 0<br>(0: disabled; 1: enabled)   |
| INT2_DRDY_G        | Gyroscope data ready on INT2_A/G pin. Default value: 0<br>(0: disabled; 1: enabled)   |
| INT2_DRDY_XL       | Accelerometer data ready on INT2_A/G pin. Default value: 0<br>(0: disabled; 1: enabled)   |

## 7.11 WHO\_AM\_I (0Fh)

Who\_AM\_I register.

**Table 43. WHO\_AM\_I register**

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|

## 7.12 CTRL\_REG1\_G (10h)

Angular rate sensor Control Register 1.

**Table 44. CTRL\_REG1\_G register**

|        |        |        |       |       |                  |       |       |
|--------|--------|--------|-------|-------|------------------|-------|-------|
| ODR_G2 | ODR_G1 | ODR_G0 | FS_G1 | FS_G0 | 0 <sup>(1)</sup> | BW_G1 | BW_G0 |
|--------|--------|--------|-------|-------|------------------|-------|-------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 45. CTRL\_REG1\_G register description**

|             |   |
|-------------|---|
| ODR_G [2:0] | Gyroscope output data rate selection. Default value: 000<br>(Refer to <a href="#">Table 46</a> and <a href="#">Table 47</a> ) |
| FS_G [1:0]  | Gyroscope full-scale selection. Default value: 00<br>(00: 245 dps; 01: 500 dps; 10: Not Available; 11: 2000 dps)              |
| BW_G [1:0]  | Gyroscope bandwidth selection. Default value: 00  |

ODR\_G [2:0] are used to set ODR selection when both the accelerometer and gyroscope are activated. BW\_G [1:0] are used to set gyroscope bandwidth selection.

The following table summarizes all frequencies available for each combination of the ODR\_G / BW\_G bits after LPF1 (see [Table 46](#)) and LPF2 (see [Table 47](#)) when both the accelerometer and gyroscope are activated. For more details regarding signal processing please refer to [Figure 28](#).

**Table 46. ODR and BW configuration setting (after LPF1)**

| ODR_G2 | ODR_G1 | ODR_G0 | ODR [Hz]   | Cutoff [Hz] <sup>(1)</sup> |
|--------|--------|--------|------------|----------------------------|
| 0      | 0      | 0      | Power-down | n.a.                       |
| 0      | 0      | 1      | 14.9       | 5                          |
| 0      | 1      | 0      | 59.5       | 19                         |
| 0      | 1      | 1      | 119        | 38                         |
| 1      | 0      | 0      | 238        | 76                         |
| 1      | 0      | 1      | 476        | 100                        |
| 1      | 1      | 0      | 952        | 100                        |
| 1      | 1      | 1      | n.a.       | n.a.                       |

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

Table 47. ODR and BW configuration setting (after LPF2)

| ODR_G [2:0] | BW_G [1:0] | ODR [Hz]   | Cutoff [Hz] <sup>(1)</sup> |
|-------------|------------|------------|----------------------------|
| 000         | 00         | Power-down | n.a.                       |
| 000         | 01         | Power-down | n.a.                       |
| 000         | 10         | Power-down | n.a.                       |
| 000         | 11         | Power-down | n.a.                       |
| 001         | 00         | 14.9       | n.a.                       |
| 001         | 01         | 14.9       | n.a.                       |
| 001         | 10         | 14.9       | n.a.                       |
| 001         | 11         | 14.9       | n.a.                       |
| 010         | 00         | 59.5       | 16                         |
| 010         | 01         | 59.5       | 16                         |
| 010         | 10         | 59.5       | 16                         |
| 010         | 11         | 59.5       | 16                         |
| 011         | 00         | 119        | 14                         |
| 011         | 01         | 119        | 31                         |
| 011         | 10         | 119        | 31                         |
| 011         | 11         | 119        | 31                         |
| 100         | 00         | 238        | 14                         |
| 100         | 01         | 238        | 29                         |
| 100         | 10         | 238        | 63                         |
| 100         | 11         | 238        | 78                         |
| 101         | 00         | 476        | 21                         |
| 101         | 01         | 476        | 28                         |
| 101         | 10         | 476        | 57                         |
| 101         | 11         | 476        | 100                        |
| 110         | 00         | 952        | 33                         |
| 110         | 01         | 952        | 40                         |
| 110         | 10         | 952        | 58                         |
| 110         | 11         | 952        | 100                        |
| 111         | 00         | n.a.       | n.a.                       |
| 111         | 01         | n.a.       | n.a.                       |
| 111         | 10         | n.a.       | n.a.                       |
| 111         | 11         | n.a.       | n.a.                       |

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

## 7.13 CTRL\_REG2\_G (11h)

Angular rate sensor Control Register 2.

**Table 48. CTRL\_REG2\_G register**

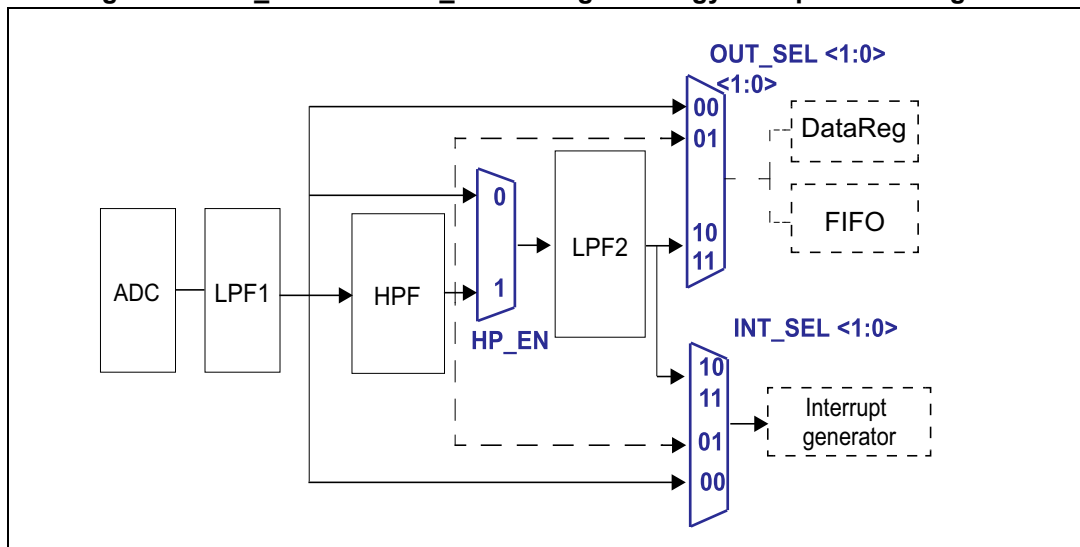
|                  |                  |                  |                  |          |          |          |          |
|------------------|------------------|------------------|------------------|----------|----------|----------|----------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | INT_SEL1 | INT_SEL0 | OUT_SEL1 | OUT_SEL0 |
|------------------|------------------|------------------|------------------|----------|----------|----------|----------|

1. These bits must be set to '0' for the correct operation of the device

**Table 49. CTRL\_REG2\_G register description**

|               |   |
|---------------|---|
| INT_SEL [1:0] | INT selection configuration. Default value: 00<br>(Refer to <a href="#">Figure 28</a> ) |
| OUT_SEL [1:0] | Out selection configuration. Default value: 00<br>(Refer to <a href="#">Figure 28</a> ) |

**Figure 28. INT\_SEL and OUT\_SEL configuration gyroscope block diagram**



## 7.14 CTRL\_REG3\_G (12h)

Angular rate sensor Control Register 3.

**Table 50. CTRL\_REG3\_G register**

|         |       |                  |                  |         |         |         |         |
|---------|-------|------------------|------------------|---------|---------|---------|---------|
| LP_mode | HP_EN | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | HPCF3_G | HPCF2_G | HPCF1_G | HPCF0_G |
|---------|-------|------------------|------------------|---------|---------|---------|---------|

1. These bits must be set to '0' for the correct operation of the device

**Table 51. CTRL\_REG3\_G register description**

|              |   |
|--------------|---|
| LP_mode      | Low-power mode enable. Default value: 0<br>(0: Low-power disabled; 1: Low-power enabled)                            |
| HP_EN        | High-pass filter enable. Default value: 0<br>(0: HPF disabled; 1: HPF enabled, refer to <a href="#">Figure 28</a> ) |
| HPCF_G [3:0] | Gyroscope high-pass filter cutoff frequency selection. Default value: 0000<br>Refer to <a href="#">Table 52</a> .   |

**Table 52. Gyroscope high-pass filter cutoff frequency configuration [Hz]<sup>(1)</sup>**

| HPCF_G [3:0] | ODR= 14.9 Hz | ODR= 59.5 Hz | ODR= 119 Hz | ODR= 238 Hz | ODR= 476 Hz | ODR= 952 Hz |
|--------------|--------------|--------------|-------------|-------------|-------------|-------------|
| 0000         | 1            | 4            | 8           | 15          | 30          | 57          |
| 0001         | 0.5          | 2            | 4           | 8           | 15          | 30          |
| 0010         | 0.2          | 1            | 2           | 4           | 8           | 15          |
| 0011         | 0.1          | 0.5          | 1           | 2           | 4           | 8           |
| 0100         | 0.05         | 0.2          | 0.5         | 1           | 2           | 4           |
| 0101         | 0.02         | 0.1          | 0.2         | 0.5         | 1           | 2           |
| 0110         | 0.01         | 0.05         | 0.1         | 0.2         | 0.5         | 1           |
| 0111         | 0.005        | 0.02         | 0.05        | 0.1         | 0.2         | 0.5         |
| 1000         | 0.002        | 0.01         | 0.02        | 0.05        | 0.1         | 0.2         |
| 1001         | 0.001        | 0.005        | 0.01        | 0.02        | 0.05        | 0.1         |

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

## 7.15 ORIENT\_CFG\_G (13h)

Angular rate sensor sign and orientation register.

**Table 53. ORIENT\_CFG\_G register**

|                  |                  |         |         |         |          |          |          |
|------------------|------------------|---------|---------|---------|----------|----------|----------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | SignX_G | SignY_G | SignZ_G | Orient_2 | Orient_1 | Orient_0 |
|------------------|------------------|---------|---------|---------|----------|----------|----------|

1. These bits must be set to '0' for the correct operation of the device.

**Table 54. ORIENT\_CFG\_G register description**

|              |  |
|--------------|--|
| SignX_G      | Pitch axis (X) angular rate sign. Default value: 0<br>(0: positive sign; 1: negative sign) |
| SignY_G      | Roll axis (Y) angular rate sign. Default value: 0<br>(0: positive sign; 1: negative sign)  |
| SignZ_G      | Yaw axis (Z) angular rate sign. Default value: 0<br>(0: positive sign; 1: negative sign)   |
| Orient [2:0] | Directional user orientation selection. Default value: 000                                 |

## 7.16 INT\_GEN\_SRC\_G (14h)

Angular rate sensor interrupt source register.

**Table 55. INT\_GEN\_SRC\_G register**

|   |      |      |      |      |      |      |      |
|---|------|------|------|------|------|------|------|
| 0 | IA_G | ZH_G | ZL_G | YH_G | YL_G | XH_G | XL_G |
|---|------|------|------|------|------|------|------|



**Table 56. INT\_GEN\_SRC\_G register description**

|      |   |
|------|---|
| IA_G | Interrupt active. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupts have been generated) |
| ZH_G | Yaw (Z) high. Default value: 0<br>(0: no interrupt, 1: Z high event has occurred)   |
| ZL_G | Yaw (Z) low. Default value: 0<br>(0: no interrupt; 1: Z low event has occurred)   |
| YH_G | Roll (Y) high. Default value: 0<br>(0: no interrupt, 1: Y high event has occurred)  |
| YL_G | Roll (Y) low. Default value: 0<br>(0: no interrupt, 1: Y low event has occurred)  |
| XH_G | Pitch (X) high. Default value: 0<br>(0: no interrupt, 1: X high event has occurred)                                       |
| XL_G | Pitch (X) low. Default value: 0<br>(0: no interrupt, 1: X low event has occurred)   |

## 7.17 OUT\_TEMP\_L (15h), OUT\_TEMP\_H (16h)

Temperature data output register. L and H registers together express a 16-bit word in two's complement right-justified.

**Table 57. OUT\_TEMP\_L register**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Temp7 | Temp6 | Temp5 | Temp4 | Temp3 | Temp2 | Temp1 | Temp0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

**Table 58. OUT\_TEMP\_H register**

|        |        |        |        |        |        |       |       |
|--------|--------|--------|--------|--------|--------|-------|-------|
| Temp11 | Temp11 | Temp11 | Temp11 | Temp11 | Temp10 | Temp9 | Temp8 |
|--------|--------|--------|--------|--------|--------|-------|-------|

**Table 59. OUT\_TEMP register description**

|             |   |
|-------------|---|
| Temp [11:0] | Temperature sensor output data.<br>The value is expressed as two's complement sign extended on the MSB. |
|-------------|---|

## 7.18 STATUS\_REG (17h)

Status register.

**Table 60. STATUS\_REG register**

|   |       |      |       |             |     |     |      |
|---|-------|------|-------|-------------|-----|-----|------|
| 0 | IG_XL | IG_G | INACT | BOOT_STATUS | TDA | GDA | XLDA |
|---|-------|------|-------|-------------|-----|-----|------|

**Table 61. STATUS\_REG register description**

|             |  |
|-------------|--|
| IG_XL       | Accelerometer interrupt output signal. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupt events have been generated) |
| IG_G        | Gyroscope interrupt output signal. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupt events have been generated)     |
| INACT       | Inactivity interrupt output signal. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupt events have been generated)    |
| BOOT_STATUS | Boot running flag signal. Default value: 0<br>(0: no boot running; 1: boot running)  |
| TDA         | Temperature sensor new data available. Default value: 0<br>(0: new data is not yet available; 1: new data is available)                              |
| GDA         | Gyroscope new data available. Default value: 0<br>(0: a new set of data is not yet available; 1: a new set of data is available)                     |
| XLDA        | Accelerometer new data available. Default value: 0<br>(0: a new set of data is not yet available; 1: a new set of data is available)                 |

### 7.19 OUT\_X\_G (18h - 19h)

Angular rate sensor pitch axis (X) angular rate output register. The value is expressed as a 16-bit word in two's complement.

### 7.20 OUT\_Y\_G (1Ah - 1Bh)

Angular rate sensor roll axis (Y) angular rate output register. The value is expressed as a 16-bit word in two's complement.

### 7.21 OUT\_Z\_G (1Ch - 1Dh)

Angular rate sensor Yaw axis (Z) angular rate output register. The value is expressed as a 16-bit word in two's complement.

### 7.22 CTRL\_REG4 (1Eh)

Control register 4.

**Table 62. CTRL\_REG4 register**

|                  |                  |       |       |       |                  |         |        |
|------------------|------------------|-------|-------|-------|------------------|---------|--------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | Zen_G | Yen_G | Xen_G | 0 <sup>(1)</sup> | LIR_XL1 | 4D_XL1 |
|------------------|------------------|-------|-------|-------|------------------|---------|--------|

1. These bits must be set to '0' for the correct operation of the device.

**Table 63. CTRL\_REG4 register description**

|         |  |
|---------|--|
| Zen_G   | Gyroscope's Yaw axis (Z) output enable. Default value: 1<br>(0: Z-axis output disabled; 1: Z-axis output enabled)  |
| Yen_G   | Gyroscope's roll axis (Y) output enable. Default value: 1<br>(0: Y-axis output disabled; 1: Y-axis output enabled)   |
| Xen_G   | Gyroscope's pitch axis (X) output enable. Default value: 1<br>(0: X-axis output disabled; 1: X-axis output enabled)  |
| LIR_XL1 | Latched Interrupt. Default value: 0<br>(0: interrupt request not latched; 1: interrupt request latched)  |
| 4D_XL1  | 4D option enabled on Interrupt. Default value: 0<br>(0: interrupt generator uses 6D for position recognition; 1: interrupt generator uses 4D for position recognition) |

## 7.23 CTRL\_REG5\_XL (1Fh)

Linear acceleration sensor Control Register 5.

**Table 64. CTRL\_REG5\_XL register**

|       |       |        |        |        |                  |                  |                  |
|-------|-------|--------|--------|--------|------------------|------------------|------------------|
| DEC_1 | DEC_0 | Zen_XL | Yen_XL | Xen_XL | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|-------|-------|--------|--------|--------|------------------|------------------|------------------|

1. These bits must be set to '0' for the correct operation of the device.

**Table 65. CTRL\_REG5\_XL register description**

|            |  |
|------------|--|
| DEC_ [0:1] | Decimation of acceleration data on OUT REG and FIFO. Default value: 00<br>(00: no decimation;<br>01: update every 2 samples;<br>10: update every 4 samples;<br>11: update every 8 samples) |
| Zen_XL     | Accelerometer's Z-axis output enable. Default value: 1<br>(0: Z-axis output disabled; 1: Z-axis output enabled)  |
| Yen_XL     | Accelerometer's Y-axis output enable. Default value: 1<br>(0: Y-axis output disabled; 1: Y-axis output enabled)  |
| Xen_XL     | Accelerometer's X-axis output enable. Default value: 1<br>(0: X-axis output disabled; 1: X-axis output enabled)  |

## 7.24 CTRL\_REG6\_XL (20h)

Linear acceleration sensor Control Register 6.

**Table 66. CTRL\_REG6\_XL register**

|         |         |         |        |        |             |        |        |
|---------|---------|---------|--------|--------|-------------|--------|--------|
| ODR_XL2 | ODR_XL1 | ODR_XL0 | FS1_XL | FS0_XL | BW_SCAL_ODR | BW_XL1 | BW_XL0 |
|---------|---------|---------|--------|--------|-------------|--------|--------|

**Table 67. CTRL\_REG6\_XL register description**

|              |   |
|--------------|---|
| ODR_XL [2:0] | Output data rate and power mode selection. default value: 000 (see <a href="#">Table 68</a> )   |
| FS_XL [1:0]  | Accelerometer full-scale selection. Default value: 00<br>(00: $\pm 2g$ ; 01: $\pm 16g$ ; 10: $\pm 4g$ ; 11: $\pm 8g$ )  |
| BW_SCAL_ODR  | Bandwidth selection. Default value: 0<br>(0: bandwidth determined by ODR selection:<br>- BW = 408 Hz when ODR = 952 Hz, 50 Hz, 10 Hz;<br>- BW = 211 Hz when ODR = 476 Hz;<br>- BW = 105 Hz when ODR = 238 Hz;<br>- BW = 50 Hz when ODR = 119 Hz;<br>1: bandwidth selected according to BW_XL [2:1] selection) |
| BW_XL [1:0]  | Anti-aliasing filter bandwidth selection. Default value: 00<br>(00: 408 Hz; 01: 211 Hz; 10: 105 Hz; 11: 50 Hz)  |

ODR\_XL [2:0] is used to set power mode and ODR selection. [Table 68](#) indicates all the frequencies available when only the accelerometer is activated.

**Table 68. ODR register setting (accelerometer only mode)**

| ODR_XL2 | ODR_XL1 | ODR_XL0 | ODR selection [Hz] |
|---------|---------|---------|--------------------|
| 0       | 0       | 0       | Power-down         |
| 0       | 0       | 1       | 10 Hz              |
| 0       | 1       | 0       | 50 Hz              |
| 0       | 1       | 1       | 119 Hz             |
| 1       | 0       | 0       | 238 Hz             |
| 1       | 0       | 1       | 476 Hz             |
| 1       | 1       | 0       | 952 Hz             |
| 1       | 1       | 1       | n.a.               |

## 7.25 CTRL\_REG7\_XL (21h)

Linear acceleration sensor Control Register 7.

**Table 69. CTRL\_REG7\_XL register**

|    |      |      |                  |                  |     |                  |       |
|----|------|------|------------------|------------------|-----|------------------|-------|
| HR | DCF1 | DCF0 | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | FDS | 0 <sup>(1)</sup> | HPIS1 |
|----|------|------|------------------|------------------|-----|------------------|-------|

1. These bits must be set to '0' for the correct operation of the device

**Table 70. CTRL\_REG7\_XL register description**

|          |  |
|----------|--|
| HR       | High resolution mode for accelerometer enable. Default value: 0<br>(0: disabled; 1: enabled). Refer to <a href="#">Table 71</a>  |
| DCF[1:0] | Accelerometer digital filter (high pass and low pass) cutoff frequency selection: the bandwidth of the high-pass filter depends on the selected ODR. Refer to <a href="#">Table 71</a> |
| FDS      | Filtered data selection. Default value: 0<br>(0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)  |
| HPIS1    | High-pass filter enabled for acceleration sensor interrupt function on Interrupt. Default value: 0<br>(0: filter bypassed; 1: filter enabled)  |

**Table 71. Low pass cutoff frequency in high resolution mode (HR = 1)**

| HR | CTRL_REG7 (DCF [1:0]) | LP cutoff freq. [Hz] |
|----|-----------------------|----------------------|
| 1  | 00                    | ODR/50               |
| 1  | 01                    | ODR/100              |
| 1  | 10                    | ODR/9                |
| 1  | 11                    | ODR/400              |

## 7.26 CTRL\_REG8 (22h)

Control register 8.

**Table 72. CTRL\_REG8 register**

|      |     |           |       |     |            |     |          |
|------|-----|-----------|-------|-----|------------|-----|----------|
| BOOT | BDU | H_LACTIVE | PP_OD | SIM | IF_ADD_INC | BLE | SW_RESET |
|------|-----|-----------|-------|-----|------------|-----|----------|

**Table 73. CTRL\_REG8 register description**

|            |   |
|------------|---|
| BOOT       | Reboot memory content. Default value: 0<br>(0: normal mode; 1: reboot memory content <sup>(1)</sup> )   |
| BDU        | Block data update. Default value: 0<br>(0: continuous update; 1: output registers not updated until MSB and LSB read)   |
| H_LACTIVE  | Interrupt activation level. Default value: 0<br>(0: interrupt output pins active high; 1: interrupt output pins active low)   |
| PP_OD      | Push-pull/open-drain selection on the INT1_A/G pin and INT2_A/G pin.<br>Default value: 0<br>(0: push-pull mode; 1: open-drain mode)                                       |
| SIM        | SPI serial interface mode selection. Default value: 0<br>(0: 4-wire interface; 1: 3-wire interface).  |
| IF_ADD_INC | Register address automatically incremented during a multiple byte access with a serial interface (I <sup>2</sup> C or SPI). Default value: 1<br>(0: disabled; 1: enabled) |
| BLE        | Big/Little Endian data selection. Default value 0<br>(0: data LSB @ lower address; 1: data MSB @ lower address)   |
| SW_RESET   | Software reset. Default value: 0<br>(0: normal mode; 1: reset device)<br>This bit is cleared by hardware after next flash boot.   |

1. Boot request is executed as soon as internal oscillator is turned-on. It is possible to set bit while in power-down mode, in this case it will be served at the next normal mode or sleep mode.

## 7.27 CTRL\_REG9 (23h)

Control register 9.

**Table 74. CTRL\_REG9 register**

|                  |         |                  |              |               |             |         |             |
|------------------|---------|------------------|--------------|---------------|-------------|---------|-------------|
| 0 <sup>(1)</sup> | SLEEP_G | 0 <sup>(1)</sup> | FIFO_TEMP_EN | DRDY_mask_bit | I2C_DISABLE | FIFO_EN | STOP_ON_FTH |
|------------------|---------|------------------|--------------|---------------|-------------|---------|-------------|

1. These bits must be set to '0' for the correct operation of the device

**Table 75. CTRL\_REG9 register description**

|               |  |
|---------------|--|
| SLEEP_G       | Gyroscope sleep mode enable. Default value: 0<br>(0: disabled; 1: enabled)   |
| FIFO_TEMP_EN  | Temperature data storage in FIFO enable. Default value: 0<br>(0: temperature data not stored in FIFO; 1: temperature data stored in FIFO)  |
| DRDY_mask_bit | Data available enable bit. Default value: 0<br>(0: DA timer disabled; 1: DA timer enabled)   |
| I2C_DISABLE   | Disable I <sup>2</sup> C interface. Default value: 0<br>(0: both I <sup>2</sup> C and SPI enabled; 1: I <sup>2</sup> C disabled, SPI only) |
| FIFO_EN       | FIFO memory enable. Default value: 0<br>(0: disabled; 1: enabled)  |
| STOP_ON_FTH   | Enable FIFO threshold level use. Default value: 0<br>(0: FIFO depth is not limited; 1: FIFO depth is limited to threshold level)           |

## 7.28 CTRL\_REG10 (24h)

Control register 10.

**Table 76. CTRL\_REG10 register**

|                  |                  |                  |                  |                  |      |                  |       |
|------------------|------------------|------------------|------------------|------------------|------|------------------|-------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | ST_G | 0 <sup>(1)</sup> | ST_XL |
|------------------|------------------|------------------|------------------|------------------|------|------------------|-------|

1. These bits must be set to '0' for the correct operation of the device

**Table 77. CTRL\_REG10 register description**

|       |  |
|-------|--|
| ST_G  | Angular rate sensor self-test enable. Default value: 0<br>(0: Self-test disabled; 1: Self-test enabled)        |
| ST_XL | Linear acceleration sensor self-test enable. Default value: 0<br>(0: Self-test disabled; 1: Self-test enabled) |

## 7.29 INT\_GEN\_SRC\_XL (26h)

Linear acceleration sensor interrupt source register.

**Table 78. INT\_GEN\_SRC\_XL register**

|   |       |       |       |       |       |       |       |
|---|-------|-------|-------|-------|-------|-------|-------|
| 0 | IA_XL | ZH_XL | ZL_XL | YH_XL | YL_XL | XH_XL | XL_XL |
|---|-------|-------|-------|-------|-------|-------|-------|

Table 79. INT\_GEN\_SRC\_XL register description

|       |  |
|-------|--|
| IA_XL | Interrupt active. Default value: 0.<br>(0: no interrupt has been generated; 1: one or more interrupts have been generated) |
| ZH_XL | Accelerometer's Z high event. Default value: 0<br>(0: no interrupt, 1: Z high event has occurred)                          |
| ZL_XL | Accelerometer's Z low event. Default value: 0<br>(0: no interrupt; 1: Z low event has occurred)                            |
| YH_XL | Accelerometer's Y high event. Default value: 0<br>(0: no interrupt, 1: Y high event has occurred)                          |
| YL_XL | Accelerometer's Y low event. Default value: 0<br>(0: no interrupt, 1: Y low event has occurred)                            |
| XH_XL | Accelerometer's X high event. Default value: 0<br>(0: no interrupt, 1: X high event has occurred)                          |
| XL_XL | Accelerometer's X low. event. Default value: 0<br>(0: no interrupt, 1: X low event has occurred)                           |

### 7.30 STATUS\_REG (27h)

Status register.

Table 80. STATUS\_REG register

|   |       |      |       |             |     |     |      |
|---|-------|------|-------|-------------|-----|-----|------|
| 0 | IG_XL | IG_G | INACT | BOOT_STATUS | TDA | GDA | XLDA |
|---|-------|------|-------|-------------|-----|-----|------|

Table 81. STATUS\_REG register description

|             |  |
|-------------|--|
| IG_XL       | Accelerometer interrupt output signal. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupt events have been generated) |
| IG_G        | Gyroscope interrupt output signal. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupt events have been generated)     |
| INACT       | Inactivity interrupt output signal. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupt events have been generated)    |
| BOOT_STATUS | Boot running flag signal. Default value: 0<br>(0: no boot running; 1: boot running)  |
| TDA         | Temperature sensor new data available. Default value: 0<br>(0: a new data is not yet available; 1: a new data is available)                          |
| GDA         | Gyroscope new data available. Default value: 0<br>(0: a new set of data is not yet available; 1: a new set of data is available)                     |
| XLDA        | Accelerometer new data available. Default value: 0<br>(0: a new set of data is not yet available; 1: a new set of data is available)                 |

**7.31 OUT\_X\_XL (28h - 29h)**

Linear acceleration sensor X-axis output register. The value is expressed as a 16-bit word in two's complement.

**7.32 OUT\_Y\_XL (2Ah - 2Bh)**

Linear acceleration sensor Y-axis output register. The value is expressed as a 16-bit word in two's complement.

**7.33 OUT\_Z\_XL (2Ch - 2Dh)**

Linear acceleration sensor Z-axis output register. The value is expressed as a 16-bit word in two's complement.

**7.34 FIFO\_CTRL (2Eh)**

FIFO control register.

**Table 82. FIFO\_CTRL register**

| FMODE2 | FMODE1 | FMODE0 | FTH4 | FTH3 | FTH2 | FTH1 | FTH0 |
|--------|--------|--------|------|------|------|------|------|
|--------|--------|--------|------|------|------|------|------|

**Table 83. FIFO\_CTRL register description**

|             |   |
|-------------|---|
| FMODE [2:0] | FIFO mode selection bits. Default value: 000<br>For further details refer to <a href="#">Table 84</a> . |
| FTH [4:0]   | FIFO threshold level setting. Default value: 0 0000   |

**Table 84. FIFO mode selection**

| FMODE2 | FMODE1 | FMODE0 | Mode  |
|--------|--------|--------|---|
| 0      | 0      | 0      | Bypass mode. FIFO turned off  |
| 0      | 0      | 1      | FIFO mode. Stops collecting data when FIFO is full.                               |
| 0      | 1      | 0      | Reserved  |
| 0      | 1      | 1      | Continuous mode until trigger is deasserted, then FIFO mode.                      |
| 1      | 0      | 0      | Bypass mode until trigger is deasserted, then Continuous mode.                    |
| 1      | 1      | 0      | Continuous mode. If the FIFO is full, the new sample overwrites the older sample. |



## 7.35 FIFO\_SRC (2Fh)

FIFO status control register.

**Table 85. FIFO\_SRC register**

| FTH | OV RN | FSS5 | FSS4 | FSS3 | FSS2 | FSS1 | FSS0 |
|-----|-------|------|------|------|------|------|------|
|-----|-------|------|------|------|------|------|------|

**Table 86. FIFO\_SRC register description**

|           |   |
|-----------|---|
| FTH       | FIFO threshold status.<br>(0: FIFO filling is lower than threshold level; 1: FIFO filling is equal or higher than threshold level)  |
| OV RN     | FIFO overrun status.<br>(0: FIFO is not completely filled; 1: FIFO is completely filled and at least one samples has been overwritten)<br>For further details refer to <a href="#">Table 87</a> . |
| FSS [5:0] | Number of unread samples stored into FIFO.<br>(000000: FIFO empty; 100000: FIFO full, 32 unread samples)<br>For further details refer to <a href="#">Table 87</a> .                               |

**Table 87. FIFO\_SRC example: OVR/FSS details**

| FTH    | OV RN | FSS5 | FSS4 | FSS3 | FSS2 | FSS1 | FSS0 | Description                              |
|--------|-------|------|------|------|------|------|------|--|
| 0      | 0     | 0    | 0    | 0    | 0    | 0    | 0    | FIFO empty                               |
| ...(1) | 0     | 0    | 0    | 0    | 0    | 0    | 1    | 1 unread sample                          |
| ...    |       |      |      |      |      |      |      |  |
| ...(1) | 0     | 1    | 0    | 0    | 0    | 0    | 0    | 32 unread samples                        |
| 1      | 1     | 1    | 0    | 0    | 0    | 0    | 0    | At least one sample has been overwritten |

1. When the number of unread samples in FIFO is greater than the threshold level set in register [FIFO\\_CTRL \(2Eh\)](#), FTH value is '1'.

## 7.36 INT\_GEN\_CFG\_G (30h)

Angular rate sensor interrupt generator configuration register.

**Table 88. INT\_GEN\_CFG\_G register**

| AOI_G | LIR_G | ZHIE_G | ZLIE_G | YHIE_G | YLIE_G | XHIE_G | XLIE_G |
|-------|-------|--------|--------|--------|--------|--------|--------|
|-------|-------|--------|--------|--------|--------|--------|--------|

**Table 89. INT\_GEN\_CFG\_G register description**

|        |  |
|--------|--|
| AOI_G  | AND/OR combination of gyroscope's interrupt events. Default value: 0<br>(0: OR combination; 1: AND combination)  |
| LIR_G  | Latch Gyroscope interrupt request. Default value: 0.<br>(0: interrupt request not latched; 1: interrupt request latched)   |
| ZHIE_G | Enable interrupt generation on gyroscope's yaw (Z) axis high event. Default value: 0<br>(0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold)   |
| ZLIE_G | Enable interrupt generation on gyroscope's yaw (Z) axis low event. Default value: 0<br>(0: disable interrupt request; 1: interrupt request on measured angular rate value lower than preset threshold)     |
| YHIE_G | Enable interrupt generation on gyroscope's roll (Y) axis high event. Default value: 0<br>(0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold)  |
| YLIE_G | Enable interrupt generation on gyroscope's roll (Y) axis low event. Default value: 0<br>(0: disable interrupt request; 1: interrupt request on measured angular rate value lower than preset threshold)    |
| XHIE_G | Enable interrupt generation on gyroscope's pitch (X) axis high event. Default value: 0<br>(0: disable interrupt request; 1: interrupt request on measured angular rate value higher than preset threshold) |
| XLIE_G | Enable interrupt generation on gyroscope's pitch (X) axis low event. Default value: 0.<br>(0: disable interrupt request; 1: interrupt request on measured angular rate value lower than preset threshold)  |

### 7.37 INT\_GEN\_THS\_X\_G (31h - 32h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

**Table 90. INT\_GEN\_THS\_XH\_G register**

|        |               |               |               |               |               |              |              |
|--------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|
| DCRM_G | THS_G_<br>X14 | THS_G_<br>X13 | THS_G_<br>X12 | THS_G_<br>X11 | THS_G_<br>X10 | THS_G_<br>X9 | THS_G_<br>X8 |
|--------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|

**Table 91. INT\_GEN\_THS\_XL\_G register**

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| THS_G_<br>X7 | THS_G_<br>X6 | THS_G_<br>X5 | THS_G_<br>X4 | THS_G_<br>X3 | THS_G_<br>X2 | THS_G_<br>X1 | THS_G_<br>X0 |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

**Table 92. INT\_GEN\_THS\_X\_G register description**

|                |  |
|----------------|--|
| DCRM_G         | Decrement or reset counter mode selection. Default value: 0<br>(0: Reset; 1: Decrement, as per counter behavior in <a href="#">Figure 29</a> and <a href="#">Figure 30</a> ) |
| THS_G_X [14:0] | Angular rate sensor interrupt threshold on pitch (X) axis.<br>Default value: 0000000 00000000  |

### 7.38 INT\_GEN\_THS\_Y\_G (33h - 34h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

**Table 93. INT\_GEN\_THS\_YH\_G register**

|                  |               |               |               |               |               |              |              |
|------------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|
| 0 <sup>(1)</sup> | THS_G_<br>Y14 | THS_G_<br>Y13 | THS_G_<br>Y12 | THS_G_<br>Y11 | THS_G_<br>Y10 | THS_G_<br>Y9 | THS_G_<br>Y8 |
|------------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 94. INT\_GEN\_THS\_YL\_G register**

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| THS_G_<br>Y7 | THS_G_<br>Y6 | THS_G_<br>Y5 | THS_G_<br>Y4 | THS_G_<br>Y3 | THS_G_<br>Y2 | THS_G_<br>Y1 | THS_G_<br>Y0 |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

**Table 95. INT\_GEN\_THS\_Y\_G register description**

|                |   |
|----------------|---|
| THS_G_Y [14:0] | Angular rate sensor interrupt threshold on roll (Y) axis.<br>Default value: 0000000 00000000. |
|----------------|---|

### 7.39 INT\_GEN\_THS\_Z\_G (35h - 36h)

Angular rate sensor interrupt generator threshold registers. The value is expressed as a 15-bit word in two's complement.

**Table 96. INT\_GEN\_THS\_ZH\_G register**

|                  |               |               |               |               |               |              |              |
|------------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|
| 0 <sup>(1)</sup> | THS_G_<br>Z14 | THS_G_<br>Z13 | THS_G_<br>Z12 | THS_G_<br>Z11 | THS_G_<br>Z10 | THS_G_<br>Z9 | THS_G_<br>Z8 |
|------------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|

1. This bit must be set to '0' for the correct operation of the device.

**Table 97. INT\_GEN\_THS\_ZL\_G register**

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| THS_G_<br>Z7 | THS_G_<br>Z6 | THS_G_<br>Z5 | THS_G_<br>Z4 | THS_G_<br>Z3 | THS_G_<br>Z2 | THS_G_<br>Z1 | THS_G_<br>Z0 |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|

**Table 98. INT\_GEN\_THS\_Z\_G register description**

|                |   |
|----------------|---|
| THS_G_Z [14:0] | Angular rate sensor interrupt thresholds on yaw (Z) axis.<br>Default value: 0000000 00000000. |
|----------------|---|

### 7.40 INT\_GEN\_DUR\_G (37h)

Angular rate sensor interrupt generator duration register.

**Table 99. INT\_GEN\_DUR\_G register**

|        |        |        |        |        |        |        |        |
|--------|--------|--------|--------|--------|--------|--------|--------|
| WAIT_G | DUR_G6 | DUR_G5 | DUR_G4 | DUR_G3 | DUR_G2 | DUR_G1 | DUR_G0 |
|--------|--------|--------|--------|--------|--------|--------|--------|

Table 100. INT\_GEN\_DUR\_G register description

|             |  |
|-------------|--|
| WAIT_G      | Exit from interrupt wait function enable. Default value: 0<br>(0: wait function off; 1: wait for DUR_G [6:0] samples before exiting interrupt) |
| DUR_G [6:0] | Enter/exit interrupt duration value. Default Value: 000 0000   |

The **DUR\_G [6:0]** bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

The **WAIT\_G** bit has the following meaning:

'0': the interrupt falls immediately if the signal crosses the selected threshold

'1': if the signal crosses the selected threshold, the interrupt falls after a number of samples equal to the value of the duration counter register.

For further details refer to [Figure 29](#) and [Figure 30](#).

Figure 29. Wait bit disabled

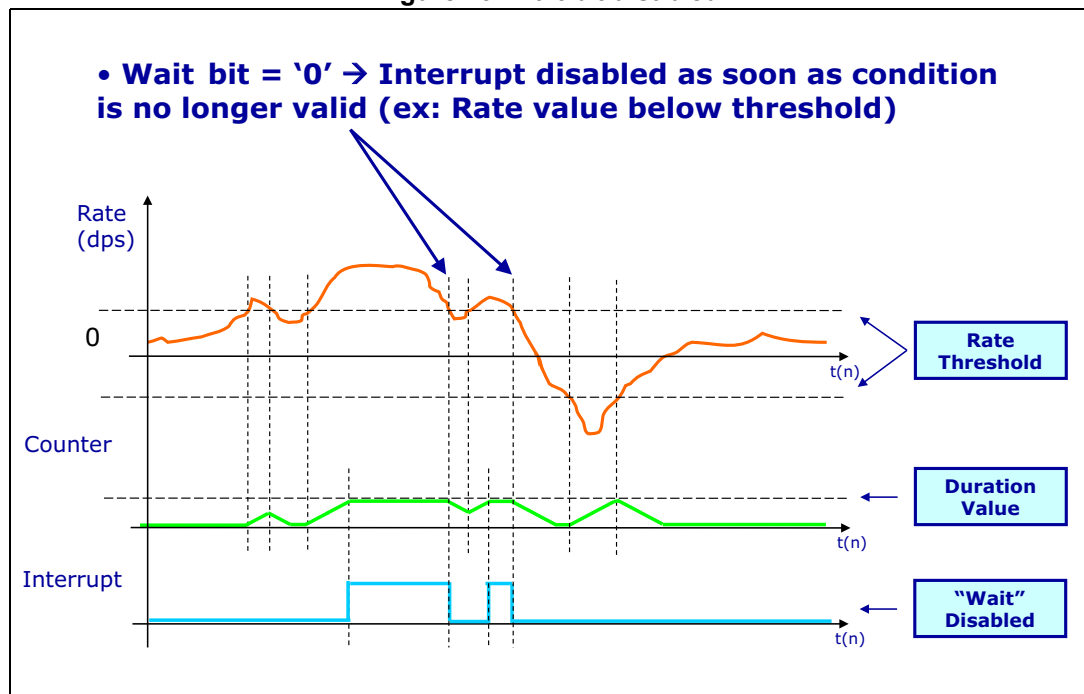
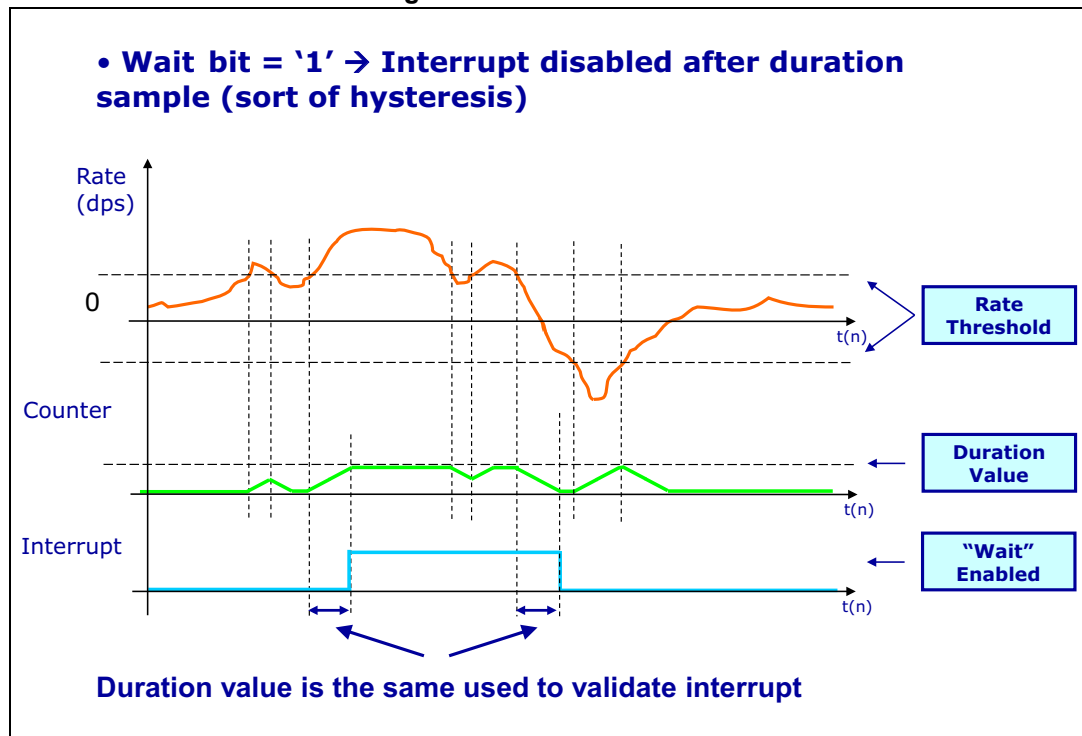


Figure 30. Wait bit enabled



## 8 Magnetometer register description

### 8.1 OFFSET\_X\_REG\_L\_M (05h), OFFSET\_X\_REG\_H\_M (06h)

This register is a 16-bit register and represents the X offset used to compensate environmental effects (data is expressed as two's complement). This value acts on the magnetic output data value in order to subtract the environmental offset.

Default value: 0

**Table 101. OFFSET\_X\_REG\_L\_M register**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OFXM7 | OFXM6 | OFXM5 | OFXM4 | OFXM3 | OFXM2 | OFXM1 | OFXM0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

**Table 102. OFFSET\_X\_REG\_H\_M register**

|        |        |        |        |        |        |       |       |
|--------|--------|--------|--------|--------|--------|-------|-------|
| OFXM15 | OFXM14 | OFXM13 | OFXM12 | OFXM11 | OFXM10 | OFXM9 | OFXM8 |
|--------|--------|--------|--------|--------|--------|-------|-------|

### 8.2 OFFSET\_Y\_REG\_L\_M (07h), OFFSET\_Y\_REG\_H\_M (08h)

This register is a 16-bit register and represents the Y offset used to compensate environmental effects (data is expressed as two's complement). This value acts on the magnetic output data value in order to subtract the environmental offset.

Default value: 0

**Table 103. OFFSET\_Y\_REG\_L\_M register**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OFYM7 | OFYM6 | OFYM5 | OFYM4 | OFYM3 | OFYM2 | OFYM1 | OFYM0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

**Table 104. OFFSET\_Y\_REG\_H\_M register**

|        |        |        |        |        |        |       |       |
|--------|--------|--------|--------|--------|--------|-------|-------|
| OFYM15 | OFYM14 | OFYM13 | OFYM12 | OFYM11 | OFYM10 | OFYM9 | OFYM8 |
|--------|--------|--------|--------|--------|--------|-------|-------|

### 8.3 OFFSET\_Z\_REG\_L\_M (09h), OFFSET\_Z\_REG\_H\_M (0Ah)

This register is a 16-bit register and represents the Z offset used to compensate environmental effects (data is expressed as two's complement). This value acts on the magnetic output data value in order to subtract the environmental offset.

Default value: 0.

**Table 105. OFFSET\_Z\_REG\_L\_M register**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OFZM7 | OFZM6 | OFZM5 | OFZM4 | OFZM3 | OFZM2 | OFZM1 | OFZM0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

**Table 106. OFFSET\_Z\_REG\_H\_M register**

|        |        |        |        |        |        |       |       |
|--------|--------|--------|--------|--------|--------|-------|-------|
| OFZM15 | OFZM14 | OFZM13 | OFZM12 | OFZM11 | OFZM10 | OFZM9 | OFZM8 |
|--------|--------|--------|--------|--------|--------|-------|-------|

## 8.4 WHO\_AM\_I\_M (0Fh)

Device identification register.

**Table 107. WHO\_AM\_I\_M register**

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
|---|---|---|---|---|---|---|---|

## 8.5 CTRL\_REG1\_M (20h)

**Table 108. CTRL\_REG1\_M register**

|           |     |     |     |     |     |          |    |
|-----------|-----|-----|-----|-----|-----|----------|----|
| TEMP_COMP | OM1 | OM0 | DO2 | DO1 | DO0 | FAST_ODR | ST |
|-----------|-----|-----|-----|-----|-----|----------|----|

**Table 109. CTRL\_REG1\_M register description**

|           |  |
|-----------|--|
| TEMP_COMP | Temperature compensation enable. Default value: 0<br>(0: temperature compensation disabled; 1: temperature compensation enabled) |
| OM[1:0]   | X and Y axes operative mode selection. Default value: 00<br>(Refer to <a href="#">Table 110</a> )                                |
| DO[2:0]   | Output data rate selection. Default value: 100<br>(Refer to <a href="#">Table 111</a> )  |
| FAST_ODR  | FAST_ODR enables data rates higher than 80 Hz. Default value: 0<br>(0: Fast_ODR disabled; 1: FAST_ODR enabled)                   |
| ST        | Self-test enable. Default value: 0<br>(0: self-test disabled; 1: self-test enabled)  |

**Table 110. X and Y axes operative mode selection**

| OM1 | OM0 | Operative mode for X and Y axes |
|-----|-----|---------------------------------|
| 0   | 0   | Low-power mode                  |
| 0   | 1   | Medium-performance mode         |
| 1   | 0   | High-performance mode           |
| 1   | 1   | Ultra-high performance mode     |

**Table 111. Output data rate configuration**

| DO2 | DO1 | DO0 | ODR [Hz] |
|-----|-----|-----|----------|
| 0   | 0   | 0   | 0.625    |
| 0   | 0   | 1   | 1.25     |
| 0   | 1   | 0   | 2.5      |
| 0   | 1   | 1   | 5        |
| 1   | 0   | 0   | 10       |
| 1   | 0   | 1   | 20       |
| 1   | 1   | 0   | 40       |
| 1   | 1   | 1   | 80       |

## 8.6 CTRL\_REG2\_M (21h)

**Table 112. CTRL\_REG2\_M register**

|                  |     |     |                  |        |          |                  |                  |
|------------------|-----|-----|------------------|--------|----------|------------------|------------------|
| 0 <sup>(1)</sup> | FS1 | FS0 | 0 <sup>(1)</sup> | REBOOT | SOFT_RST | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|------------------|-----|-----|------------------|--------|----------|------------------|------------------|

1. These bits must be set to '0' for the correct operation of the device.

**Table 113. CTRL\_REG2\_M register description**

|          |   |
|----------|---|
| FS[1:0]  | Full-scale configuration. Default value: 00<br>Refer to <a href="#">Table 114</a>                   |
| REBOOT   | Reboot memory content. Default value: 0<br>(0: normal mode; 1: reboot memory content)               |
| SOFT_RST | Configuration registers and user register reset function.<br>(0: default value; 1: reset operation) |

**Table 114. Full-scale selection**

| FS1 | FS0 | Full scale |
|-----|-----|------------|
| 0   | 0   | ± 4 gauss  |
| 0   | 1   | ± 8 gauss  |
| 1   | 0   | ± 12 gauss |
| 1   | 1   | ± 16 gauss |

## 8.7 CTRL\_REG3\_M (22h)

**Table 115. CTRL\_REG3\_M register**

|             |                  |    |                  |                  |     |     |     |
|-------------|------------------|----|------------------|------------------|-----|-----|-----|
| I2C_DISABLE | 0 <sup>(1)</sup> | LP | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | SIM | MD1 | MD0 |
|-------------|------------------|----|------------------|------------------|-----|-----|-----|

1. These bits must be set to '0' for the correct operation of the device.

**Table 116. CTRL\_REG3\_M register description**

|             |  |
|-------------|--|
| I2C_DISABLE | Disable I <sup>2</sup> C interface. Default value 0. (0: I <sup>2</sup> C enable; 1: I <sup>2</sup> C disable)   |
| LP          | Low-power mode configuration. Default value: 0<br>If this bit is '1', the DO[2:0] is set to 0.625 Hz and the system performs, for each channel, the minimum number of averages. Once the bit is set to '0', the magnetic data rate is configured by the DO bits in the <a href="#">CTRL_REG1_M (20h)</a> register. |
| SIM         | SPI Serial Interface mode selection. Default value: 0<br>(0: SPI only write operations enabled; 1: SPI read and write operations enable).  |
| MD[1:0]     | Operating mode selection. Default value: 11<br>Refer to <a href="#">Table 117</a> .  |



Table 117. System operating mode selection

| MD1 | MD0 | Mode                       |
|-----|-----|----------------------------|
| 0   | 0   | Continuous-conversion mode |
| 0   | 1   | Single-conversion mode     |
| 1   | 0   | Power-down mode            |
| 1   | 1   | Power-down mode            |

## 8.8 CTRL\_REG4\_M (23h)

Table 118. CTRL\_REG4\_M register

|                  |                  |                  |                  |      |      |     |                  |
|------------------|------------------|------------------|------------------|------|------|-----|------------------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | OMZ1 | OMZ0 | BLE | 0 <sup>(1)</sup> |
|------------------|------------------|------------------|------------------|------|------|-----|------------------|

1. These bits must be set to '0' for the correct operation of the device

Table 119. CTRL\_REG4\_M register description

|          |  |
|----------|--|
| OMZ[1:0] | Z-axis operative mode selection.<br>Default value: 00. Refer to <a href="#">Table 120</a> .                        |
| BLE      | Big/Little Endian data selection. Default value: 0<br>(0: data LSb at lower address; 1: data MSb at lower address) |

Table 120. Z-axis operative mode selection

| OMZ1 | OMZ0 | Operative mode for Z-axis   |
|------|------|-----------------------------|
| 0    | 0    | Low-power mode              |
| 0    | 1    | Medium-performance mode     |
| 1    | 0    | High-performance mode       |
| 1    | 1    | Ultra-high performance mode |

## 8.9 CTRL\_REG5\_M (24h)

Table 121. CTRL\_REG5\_M register

|           |     |                  |                  |                  |                  |                  |                  |
|-----------|-----|------------------|------------------|------------------|------------------|------------------|------------------|
| FAST_READ | BDU | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> |
|-----------|-----|------------------|------------------|------------------|------------------|------------------|------------------|

1. These bits must be set to '0' for the correct operation of the device.

Table 122. CTRL\_REG5\_M register description

|           |  |
|-----------|--|
| FAST_READ | FAST_READ allows reading the high part of DATA OUT only in order to increase reading efficiency. Default value: 0<br>(0: FAST_READ disabled; 1: FAST_READ enabled) |
| BDU       | Block data update for magnetic data. Default value: 0<br>(0: continuous update; 1: output registers not updated until MSB and LSB have been read)                  |

## 8.10 STATUS\_REG\_M (27h)

**Table 123. STATUS\_REG\_M register**

|       |     |     |     |       |     |     |     |
|-------|-----|-----|-----|-------|-----|-----|-----|
| ZYXOR | ZOR | YOR | XOR | ZYXDA | ZDA | YDA | XDA |
|-------|-----|-----|-----|-------|-----|-----|-----|

**Table 124. STATUS\_REG\_M register description**

|       |  |
|-------|--|
| ZYXOR | X, Y and Z-axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: a new set of data has overwritten the previous set)         |
| ZOR   | Z-axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: new data for the Z-axis has overwritten the previous data)           |
| YOR   | Y-axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: new data for the Y-axis has overwritten the previous data)           |
| XOR   | X-axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: new data for the X-axis has overwritten the previous data)           |
| ZYXDA | X, Y and Z-axis new data available. Default value: 0<br>(0: a new set of data is not yet available;<br>1: a new set of data is available)        |
| ZDA   | Z-axis new data available. Default value: 0<br>(0: new data for the Z-axis is not yet available;<br>1: new data for the Z-axis is available)     |
| YDA   | Y-axis new data available. Default value: 0<br>(0: new data for the Y-axis is not yet available;<br>1: new data for the Y-axis is available)     |
| XDA   | X-axis new data available. Default value: 0<br>(0: a new data for the X-axis is not yet available;<br>1: a new data for the X-axis is available) |

## 8.11 OUT\_X\_L\_M (28h), OUT\_X\_H\_M(29h)

Magnetometer X-axis data output. The value of the magnetic field is expressed as two's complement.

## 8.12 OUT\_Y\_L\_M (2Ah), OUT\_Y\_H\_M (2Bh)

Magnetometer Y-axis data output. The value of the magnetic field is expressed as two's complement.

## 8.13 OUT\_Z\_L\_M (2Ch), OUT\_Z\_H\_M (2Dh)

Magnetometer Z-axis data output. The value of the magnetic field is expressed as two's complement.

## 8.14 INT\_CFG\_M (30h)

**Table 125. INT\_CFG\_M register**

|      |      |      |                  |                  |     |     |     |
|------|------|------|------------------|------------------|-----|-----|-----|
| XIEN | YIEN | ZIEN | 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | IEA | IEL | IEN |
|------|------|------|------------------|------------------|-----|-----|-----|

1. This bit must be set to '0' for the correct operation of the device.

**Table 126. INT\_CFG\_M register description**

|      |  |
|------|--|
| XIEN | Enable interrupt generation on X-axis. Default value: 0<br>0: disable interrupt request; 1: enable interrupt request   |
| YIEN | Enable interrupt generation on Y-axis. Default value: 0<br>0: disable interrupt request; 1: enable interrupt request   |
| ZIEN | Enable interrupt generation on Z-axis. Default value: 0<br>0: disable interrupt request; 1: enable interrupt request   |
| IEA  | Interrupt active configuration on INT_MAG. Default value: 0<br>0: low; 1: high   |
| IEL  | Latch interrupt request. Default value: 0<br>0: interrupt request latched; 1: interrupt request not latched)<br>Once latched, the INT_M pin remains in the same state until <a href="#">INT_SRC_M (31h)</a> is read. |
| IEN  | Interrupt enable on the INT_M pin. Default value: 0<br>0: disable; 1: enable   |

## 8.15 INT\_SRC\_M (31h)

**Table 127. INT\_SRC\_M register**

|       |       |       |       |       |       |                     |     |
|-------|-------|-------|-------|-------|-------|---------------------|-----|
| PTH_X | PTH_Y | PTH_Z | NTH_X | NTH_Y | NTH_Z | MROI <sup>(1)</sup> | INT |
|-------|-------|-------|-------|-------|-------|---------------------|-----|

1. This functionality can be enabled only if the IEN bit in [INT\\_CFG\\_M \(30h\)](#) is enabled.

**Table 128. INT\_SRC\_M register description**

|       |   |
|-------|---|
| PTH_X | Value on X-axis exceeds the threshold on the positive side.<br>Default value: 0 |
| PTH_Y | Value on Y-axis exceeds the threshold on the positive side.<br>Default value: 0 |
| PTH_Z | Value on Z-axis exceeds the threshold on the positive side.<br>Default value: 0 |
| NTH_X | Value on X-axis exceeds the threshold on the negative side.<br>Default value: 0 |
| NTH_Y | Value on Y-axis exceeds the threshold on the negative side.<br>Default value: 0 |
| NTH_Z | Value on Z-axis exceeds the threshold on the negative side.<br>Default value: 0 |
| MROI  | Internal measurement range overflow on magnetic value.<br>Default value: 0      |
| INT   | This bit signals when the interrupt event occurs.                               |

8.16 INT\_THS\_L(32h), INT\_THS\_H(33h)

Interrupt threshold. Default value: 0.  
The value is expressed in 15-bit unsigned.  
Even if the threshold is expressed in absolute value, the device detects both positive and negative thresholds.

Table 129. INT\_THS\_L\_M register

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| THS7 | THS6 | THS5 | THS4 | THS3 | THS2 | THS1 | THS0 |
|------|------|------|------|------|------|------|------|

Table 130. INT\_THS\_H\_M register

|                  |       |       |       |       |       |      |      |
|------------------|-------|-------|-------|-------|-------|------|------|
| 0 <sup>(1)</sup> | THS14 | THS13 | THS12 | THS11 | THS10 | THS9 | THS8 |
|------------------|-------|-------|-------|-------|-------|------|------|

1. This bit must be set to '0' for the correct operation of the device.



## 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 9.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at [www.st.com/mems](http://www.st.com/mems).

### 9.2 LGA package information

Figure 31. LGA (3.5x3x1 mm) 24-lead package outline

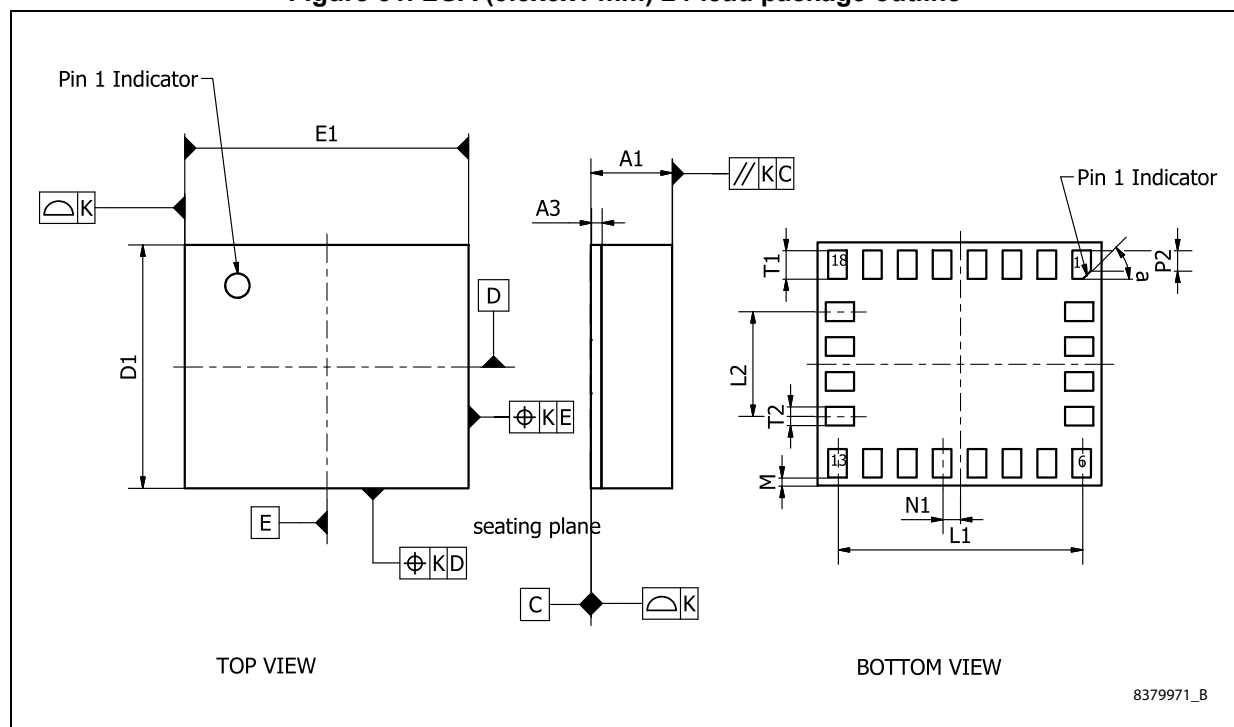


Table 131. LGA (3.5x3x1 mm) 24-lead package mechanical data

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A1   |       | 1.000 | 1.027 |
| A3   |       | 0.130 |       |
| D1   | 2.850 | 3.000 | 3.150 |
| E1   | 3.350 | 3.500 | 3.650 |
| L1   | 2.960 | 3.010 | 3.060 |
| L2   | 1.240 | 1.290 | 1.340 |
| N1   | 0.165 | 0.215 | 0.265 |
| P2   | 0.200 | 0.250 | 0.300 |
| a    |       | 45°   |       |
| T1   | 0.300 | 0.350 | 0.400 |
| T2   | 0.180 | 0.230 | 0.280 |
| K    |       | 0.050 |       |
| M    |       | 0.100 |       |

## 10 Revision history

**Table 132. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 18-Dec-2013 | 1        | Initial release  |
| 05-Nov-2014 | 2        | Datasheet status promoted from preliminary to production data<br>Added $\pm 16\text{ g}$ linear acceleration full scale throughout datasheet<br>Corrected typo in footnote 3, 4 and 5 of <a href="#">Table 2: Pin description</a><br>Updated <a href="#">Figure 15: LSM9DS1 electrical connections</a> and<br><a href="#">Section 4.1: External capacitors</a><br>Updated <a href="#">Table 117: System operating mode selection</a> |
| 12-Mar-2015 | 3        | Added FAST_ODR bit to <a href="#">CTRL_REG1_M (20h)</a><br>Added FAST_READ bit to <a href="#">CTRL_REG5_M (24h)</a>  |

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