Report for E-design 344

by

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E-Design report # 2

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Declaration

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Signature: Jonathan Frost .....

Date: 23/09/2019 .....

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Nomenclature

Constants

$g = \quad 9.81\,\mathrm{m/s^2}$

Variables

P	Power	[W]

Abbreviations

$op-amp$	operational amplifier
pp	peak-to-peak
PWM	phase width modulation

Chapter 1

Signal conditioning system design

1.1 System overview

The signal conditioning system consists of the voltage transducer, current transducer and the phase shift transducer. The voltage transducer takes it's input before the load. The current transducer takes it's input from after the load and before the sense resistor. The phase shift transducer takes inputs before the load and from the current transducer. The op-amps selected for the all the transducers are the TLC2722. The total number of op-amps used is minimised in the design to limit current draw from the voltage regulators. In Figure 1.1 below the voltage transducer is the orange block, the current transducer the green block and the phase transducer is the blue block, all of which share the same ground.

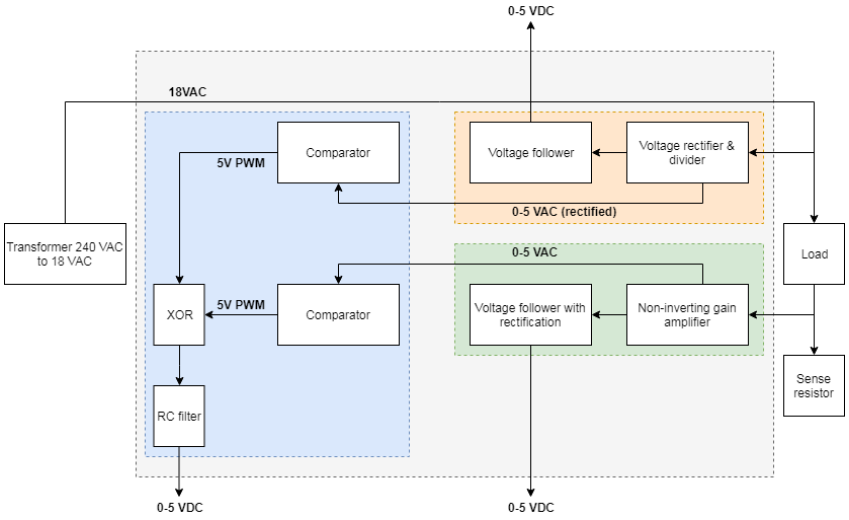


Figure 1.1: System diagram

Chapter 2

Voltage peak transducer

2.1 Theory and related work

The basic principle on which the voltage transducer is based, is the rectification of a diminished ratio of the input voltage, which is detected losslessly using a unity gain op-amp in conjunction with a specific push-pull diode configuration which charges a capacitor to a voltage sufficient enough to remain above 0V thereby alleviating the necessity of using a -5V for the negative terminal of the op-amp. This enables accurate measurement of the peak voltage over the load without surpassing the op-amp maximum ratings[1].

2.2 Design

To decrease the input voltage from an 18VAC to a 5VAC range which the TLC2722 op-amp can handle a voltage divider is used (R1 and R2) The voltage was taken 4.5V since the maximum input voltage of the TLC2272 is 4.85V[2].

$$28.28 \cdot \frac{R2}{R1 + R2} = 4.5V \tag{2.1}$$

Since the design was chosen to use a ground and 5V for op-amp rails negative and positive respectively, the input is rectified using diode D3 as seen in Figure 2.1. The drawback of this configuration is the voltage drop over D3. D2 is used in conjunction with D3 to force the current at the positive terminal of the op-amp to never go negative therefore not exceeding the minimum input of 0V[1]. Capacitor C2 charges during the positive cycle of the sinusoidal input, the value of C2 is small since the charge on the capacitor only had to be enough to stop the voltage at the positive terminal of the op-amp .

The second part of the circuit is the unity gain op-amp peak detector. The feedback loop to the negative terminal of the op-amp gives the system unity gain in conjunction with the peak detector diode D1 without losing voltage over D1. Capacitor C1 is part of the rectification in conjunction with D1. The value was chosen according to the time domain specifications. Using the time constant formula

$$\tau = RC \tag{2.2}$$

in combination with

$$10\tau = \frac{1}{2 \cdot f} \tag{2.3}$$

knowing R as 1.5MΩ, C was calculated to be 1µF.

In Figure 2.1 there is one component missing which is a grounded load resistor in parallel with C1, which is chosen to have a value of 1.5 MΩ to draw as little current from the output of the op-amp as possible and allow C1 to discharge to ground.

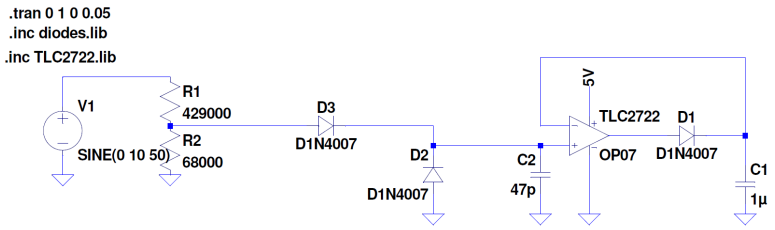


Figure 2.1: Voltage transducer

2.3 Simulation

The simulation performed as designed with the input voltage peak being replicated at the output of the transducer as seen in Figure 2.2.

2.4 Measurements

The following measurements in Table 2.1 are taken from the practical circuit of the voltage transducer where the voltage was simulated using a signal generator. Table 2.2 measurements were taken using voltage from the 18VAC transformer over each tested loaded mentioned in the table.

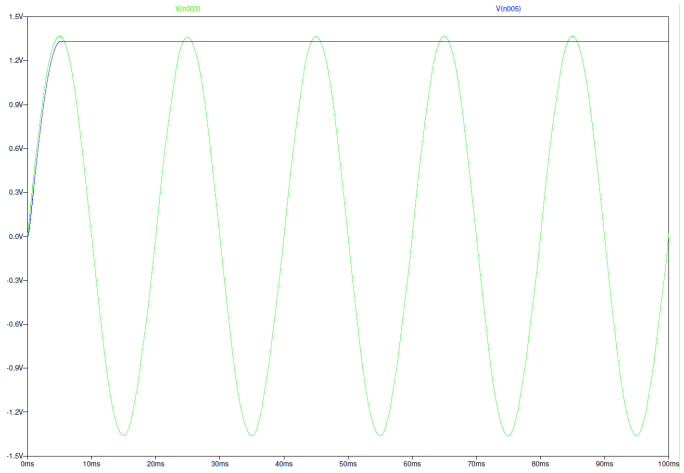


Figure 2.2: Voltage transducer input vs output

Table 2.1: Voltage transducer intermediate Unit-level tests

Emulated level	Signal generator calc.	Signal generator meas.	Analogue output	Deduced input	Difference
16.00V	2.536V	2.60V	2.54V	16.02V	20mV
21.00V	3.329V	3.40V	3.30V	20.82V	180mV
21.15V	3.352V	3.42V	3.36V	21.19V	40mV
21.30V	3.376V	3.44V	3.37V	21.26V	40mV
26.00V	4.121V	4.20V	4.67V	25.68V	320mV

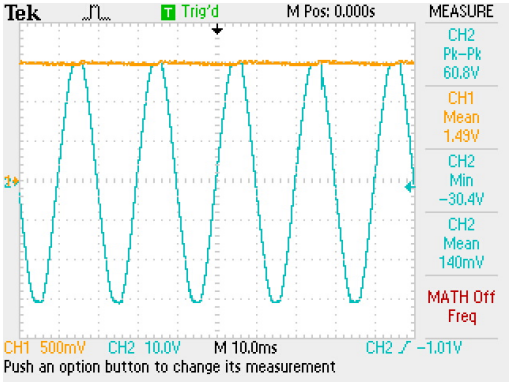
Table 2.2: Voltage transducer integrated test results

Measurement	Load R [Ω]	Load C [µF]	Measured input [V_peak]	Analogue output [VDC]	Deduced input [V_peak]	Difference [V]
No load	open	none	31.2V	4.56V	28.77V	2.75V
Full load	100	none	29.6V	4.44V	28.01V	1.59V
Mid range	1k	none	30.8V	4.51V	28.45V	2.35V

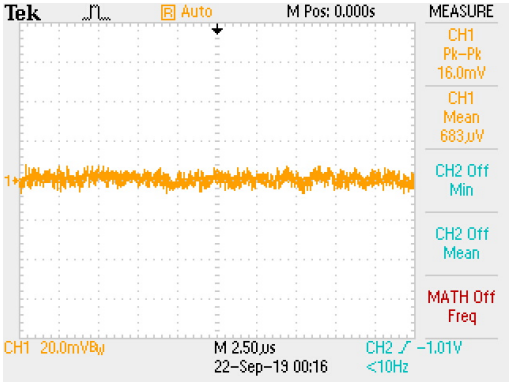
The notable mentions about the practical measurements are that for the unit-level tests, the differences between the actual peak input voltage and the peak detected by the transducer are inconsistent, however within acceptable tolerance levels. With regards to the integrated test results there is a very large discrepancy between the two. This flaw was only discovered late into testing and can be explained by the fact that the design only considered a maximum input peak of

20VAC (28.28 V peak) as specified in the updated assignment [3]. This was incorrectly assumed. It can be seen from the ***Measured input*** column that the actual peak input voltages were considerably higher.

With regard to the requirements, the transducer accepts all voltages within the specified range. The output range falls within 0 to 5V. The noise levels are extremely good ($16mV_{pp}$) as seen in Figure 2.3. From Table 2.1 it is apparent that with a small delta change in the input (150mV), the output changes with 0.01V correspondingly.



(a) AC input and analogue voltage output



(b) Noise on voltage output

Figure 2.3: Voltage transducer response

Chapter 3

Current peak transducer

3.1 Theory and related work

The current transducer works by taking a voltage over a small series resistor, Rsense, which is in series with the load. This voltage is then amplified using a voltage gain op-amp circuit. This AC voltage is then passed through a voltage follower op-amp circuit with a diode and capacitor for rectification and peak detection.

3.2 Design

The primary design phase was to gain the voltage over the Rsense resistor to values that would fall within the required 5V range. Given the maximum voltage over Rsense is the maximum current multiplied by the resistance value, we can calculate the gain factor to be

$$V_Rsense \cdot \frac{R1}{R2} = 4.2V \tag{3.1}$$

4.2V was chosen since the TLC2722 can not reliably output 5V according to the data sheet[2]. Given that the value of the sum of R1 and R2 is sufficiently high to limit current flow between terminals of the op-amps, values of R1 as 1kΩ and R2 as 470kΩ were chosen.

The next section of the circuit is the peak detector which follows the same logic as the voltage transducer in Section 2 and is in fact exactly the same which can compared between Figure 2.1 and Figure 3.1.

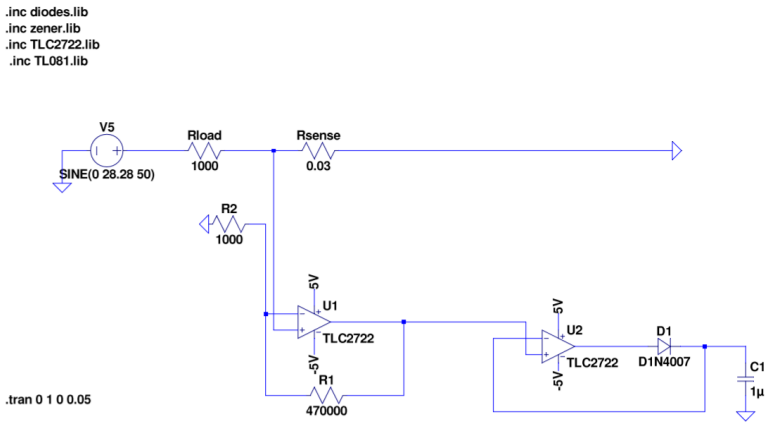


Figure 3.1: Current transducer

3.3 Simulation

In Figure 3.2 the sinusoidal current (blue) through the load is plotted alongside the output voltage of the transducer (green). Disregarding the 10mV ripple on the output voltage and only considering the average voltage, it is shown that when a negative 10mA change in the current was applied at time stamp 495ms (the change can be seen by comparing the 2nd and 3rd peak current values), the output voltage dropped from 4.00V to its new average value within 50ms with the new voltage value averaging 3.96V

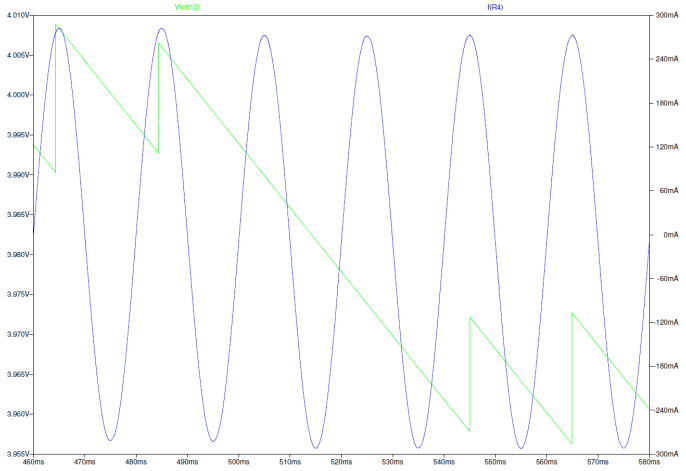


Figure 3.2: Current transducer response

3.4 Measurements

The Table 3.1 measurements are taken using a signal generator to simulate a current through Rsense, but since the signal generator can not produce a signal with small enough peak voltage, a simple temporary voltage divider was used at the input of the op-amp. Table 3.2 was tested using real load resistors as per Figure 3.1 with the 18VAC supply as per Figure 1.1

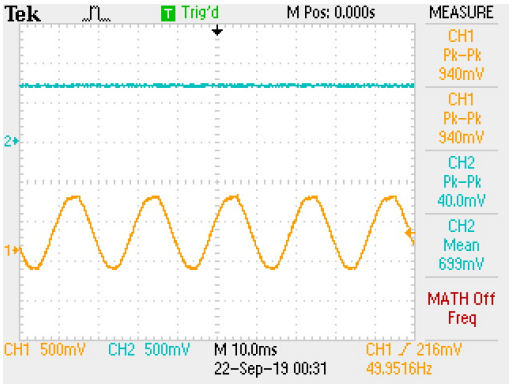
Table 3.1: Current transducer intermediate Unit-level tests

Emulated level 1	Signal generator calc. $[mV]$	Signal generator meas. $[mV]$	Analogue output $[VDC]$	Deduced input $[mA_{peak}]$	Difference $[mA]$
0	0	0	0	0	0
50	212	240	917mV	65	15
100	423	440	1.59V	112	12
101	427	448	1.60V	113	12
102	431	456	1.61V	114	12
200	846	880	2.96V	209	9
285	1025	1220	4.11V	291	6

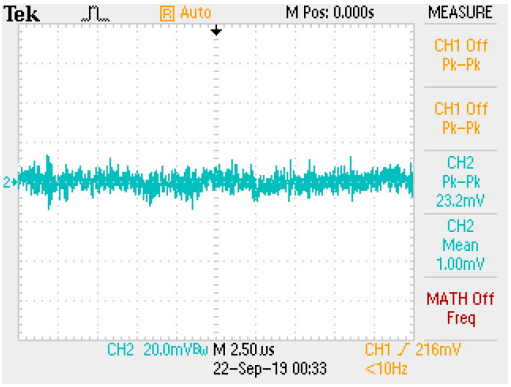
Table 3.2: Current transducer integrated test results

Test	Load R1 $[\Omega]$	Load R2 $[\Omega]$	Measured V_R $[mV_{peak}]$	Actual input $[mA_{peak}]$	Analogue output $[mVDC]$	Deduced input $[mA_{peak}]$	Difference $[mA]$
No load	open	none	0	0	227	16	16
Full load	100	none	9.15	305	4350	309	4
Mid range	1k	none	0.53	17.6	684	48.9	31.3
Mid $+\sigma$	1k	24k	1.28	42.6	777	55.1	12.5
Mid $+2\sigma$	1k	12k	1.01	33.6	737	52.2	18.6

From Table 3.1 it is apparent that the current transducer is precise, but not accurate. The precision can be seen by the small incremental changes in test current and the same small change in output voltage reflected by the deduced output. However since the circuit was designed with a peak input voltage of 28.28V (20VAC) there is an almost constant offset between the deduced input and the actual input. This problem can easily be rectified in software by applying a best fit curve and therefore is not detrimental.



(a) AC input current and analogue voltage output



(b) Noise on voltage output

With a small delta change in the input (1mA), there is a corresponding 0.01V output which falls within the system requirements. This can be seen in Table 3.1.

Chapter 4

Phase shift transducer

4.1 Theory and releated work

The phase transducer takes the voltage over the load and current through the load as inputs and outputs a continuous voltage level between 0 and 5V to represent the phase angle difference between the two. To achieve this, three parts of the circuit were designed.

Two PWM comparator circuits, (one for the current and one for the voltage) compare the input sinusoid to a reference voltage and deliver a 0 or 5V output depending on whether the sinusoid is in its negative or positive cycle respectively.

The second part of the circuit is a XOR which compares the two PWM outputs of the comparators and outputs its own PWM signal which is dependant on the phase difference between the two signals.

The final part of the circuit is a simple RC filter which takes the XOR output and transforms into a representative voltage depending on the duty cycle of the XOR output[4].

4.2 Design

Following the logic from section 4.1, the first step in the design process is to decrease the voltage input to manageable levels which was done with a simple voltage divider, which has a maximum output voltage peak of 5V for a peak input of 28.28V over the load (not shown in Figure 4.2). From here both the voltage input V2 and current input V1 are fed into a voltage divider circuit to decrease the input peaks of the sinusoidal signals (to not exceed the common mode input ratings of the TLC2272 given by equation 4.1)

$$V_{cm} = \frac{V_{in+} - V_{in-}}{2} \tag{4.1}$$

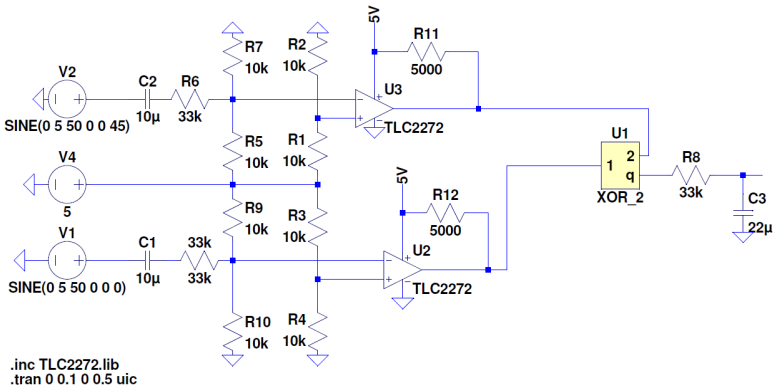


Figure 4.1: Phase shift transducer

and give a 2.5V DC offset so that the input to the op-amps would not drop below 0V since both U2 and U3 are using ground and 5V as negative and positive terminals respectively. Note how the voltage divider circuits are isolated from the inputs by capacitors C1 and C2 so that the superposition of the DC and the incoming sinusoids become the input into the negative terminal of the op-amps.

From here the signals are compared using an op-amp comparator circuit where the reference voltage is 2.5V at the positive terminal of the op-amps. This means that with a sinusoidal input (blue), whenever the input is above 2.5V the output will be pulled high (5V) and whenever it is below 2.5V it will be pulled to ground (red). This can be seen in Figure 4.1.

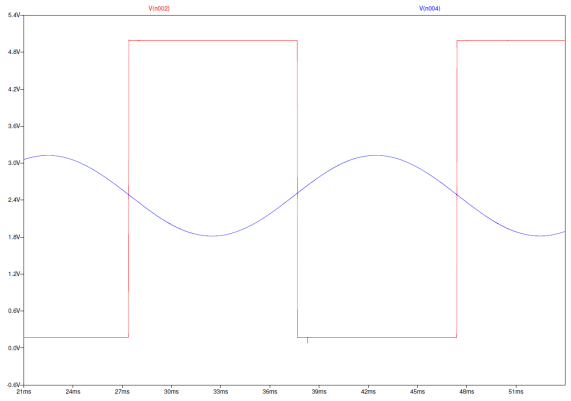


Figure 4.2: Intermediate PWM signal

Since both the voltage and current signals are handled in the same manor, applying both the signals to a logical XOR gate gives an output depending solely

on the phase difference of the PWM signals knowing that they are operating at a the same frequency of 50Hz.

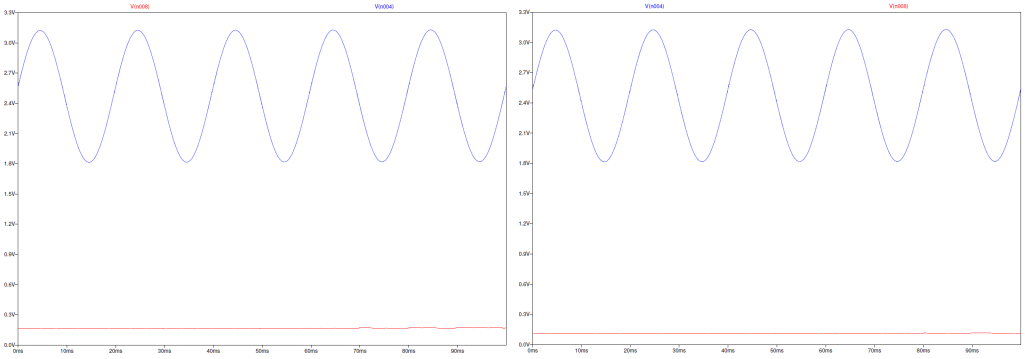
Lastly the PWM to voltage circuit needs to turn the combined output of the XOR into a distinct voltage representative of the phase difference. This is achieved by a simple RC low-pass filter [5]. Since we know the frequency of the signal to be 50Hz, we can easily calculate the required values for R8 and C3 (Figure 4.2) knowing that we need a cutoff frequency much less than 50Hz without the output ripple being too large[6]. With a 22µF chosen we can calculate R8 using the following equation:

$$f_c = \frac{1}{2\pi \cdot C3 \cdot R8} \tag{4.2}$$

R8 is calculated as 33kΩ.

4.3 Simulation

The simulation produced expected voltage outputs for the varying phase loads. In Figure 4.3 The blue line in both (a) and (b) represents the sinusoidal input to the negative terminal of the op-amp after R6. The red lines represent the voltage at the output over C3. The small change in output voltage can be seen by the lower redline in image (b). These results are similarly reflected numerically in Table 4.1.



(a) Mid range load (b) Mid $+\sigma$ load

Figure 4.3: Phase load simulation with nominal input levels

4.4 Measurements

The measurements in Table 4.1 are taken using various loads. The output is measured from the output of the RC filter as seen in Figure 4.2. To calculate the the

Table 4.1: Current transducer integrated test results

Test	Load R1 [Ω]	Load C [µF]	Measured shift [µS]	Applied shift [°]	Output level [mVDC]	Conversion [°]	Difference [°]
No phase shift	1k	none	0	0	67	3.4	3.4
Max phase shift	1k	3.3	2000	44.0	830	42.7	1.3
Mid range	1k	22	550	8.2	187	9.6	1.4
Mid $+\sigma$	1k	33	400	5.5	120	6.2	0.7
Mid $+2\sigma$	1k	47	300	3.9	98	5.0	1.1

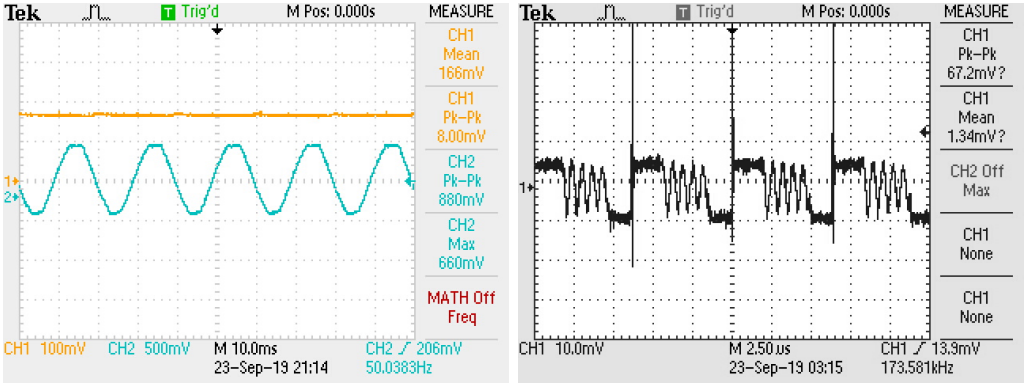
angle conversion given the output measured phase shift, the following formula is used

$$\Phi = \frac{V_{meas}}{5} \cdot 180^\circ \tag{4.3}$$

Where 5 is actually the maximum voltage output of the RC filter.

The output noise of the phase transducer is quite high with a V_{pp} of 67.2mV as seen in Figure 4.4 (b). This is not a huge problem since the DC value of the output can be averaged in software after passing through an ADC. However it would be more reliable if the noise was less significant. The noise will mostly affect the lower phase shift loads since the noise becomes a larger proportion of the signal and the DC value is therefore less distinguishable.

With a small delta input change in the phase angle difference, there is a corresponding change which falls within the 1° range which is fortunate. The actual change can be seen in Table 4.1 since there was no single degree change test, but if the ***Applied shift*** column is compared to the ***Conversion*** the difference between load test angles is consisted across both columns.



(a) Mid range measurement input and output

(b) Phase transducer AC coupled output noise

Figure 4.4: Phase response

Chapter 5

System tests

With the entire system working, the total current drawn by all the three circuits was recorded at 282.3 mA. The 5V rail was producing a fixed 5.12V with the negative rail suffering an output of only -3.6V. In Figure 5.1 the practical realisation of the circuit design on the PCB can be seen alongside the student card.

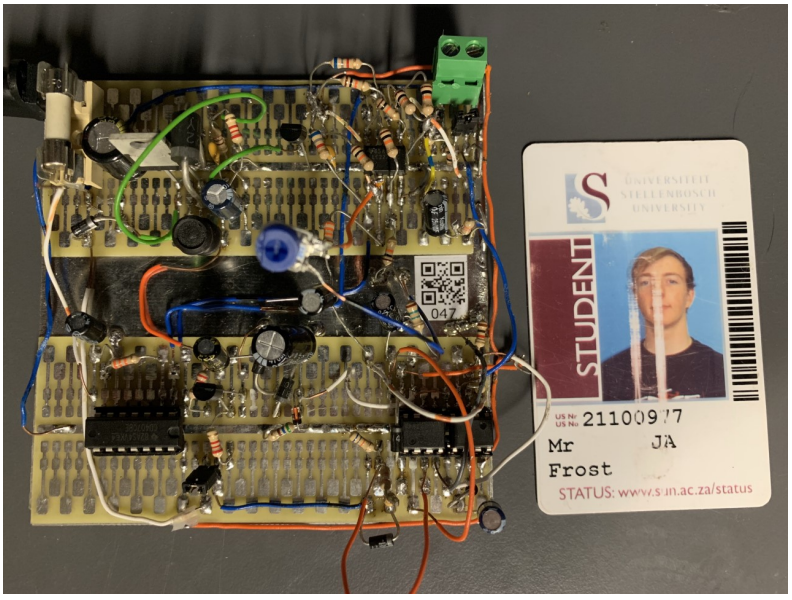


Figure 5.1: Practical realisation of circuit design

References

[1] Diodes Incorporated: 1n4007 datasheet. 2014.
Available at: https://www.diodes.com/assets/Datasheets/ds28002.pdf

[2] Texas instruments: Tlc227x, tlc227xa: Advanced lincmos rail-to-rail operational amplifiers. 2016.
Available at: https://learn.sun.ac.za/pluginfile.php/1690419/mod$_r esource/content/0/tlc2272.pd$

[3] Professor Booysen: E-design 344 assignment 2. 2019.
Available at: https://learn.sun.ac.za/pluginfile.php/1703870/mod$_r esource/content/9/E344_A ss2$

[4] Anon.: Sine wave to square wave schmitt-trigger. 2015.
Available at: https://electronics.stackexchange.com/questions/163253/sine-wave-to-square-wa

[5] Robert Keim: Low-pass filter a pwm signal into an analog voltage. 2016.
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[6] Stephen Woodward: Cancel pwm dac ripple with analog subtraction. 2017.
Available at: https://www.edn.com/design/analog/4459116/Cancel-PWM-DAC-ripple-with-analog-s

Appendix A: GitHub Activity Heatmap