Report for E-design 344

by

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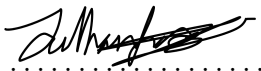
E-Design report # 1

July 2019

Declaration

By submitting this report electronically, I declare that the entirety of the work contained therein is my own, original work, that I am the sole author thereof (save to the extent explicitly otherwise stated), that reproduction and publication thereof by Stellenbosch University will not infringe any third party rights and that I have not previously in its entirety or in part submitted it for obtaining any qualifcation.

Signature: 
J. Frost

Date: 11/08/2019

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Nomenclature

Constants

g =	$9.81\,\mathrm{m/s^2}$	

Variables

P	Power	[W]
V	Voltage	[V]
R	Resistance	[R]

Notation

$I(x)$	Current through component x	[A]

Chapter 1

Power supply system design

1.1 System overview

The following figure is a flow diagram of the power supply system design.

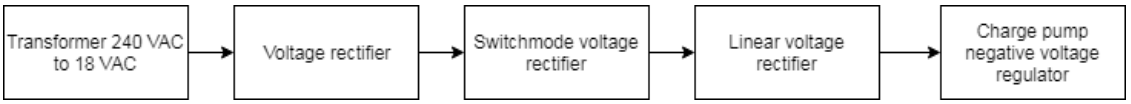


Figure 1.1: System diagram

1.2 Rationale

With the aim of trying to produce a stable 5 VDC output, with a sinusoidal 18 VAC input, rectifying the input first is a simple conclusion. Next comes the switchmode regulator which, serves the main purpose of stepping down the 18 V to 12 V, whilst cleaning a lot of noise caused by the rectification. The reason for putting the switchmode next was that it could output a 12 V signal which might come in use later for components which require a 12 V input. Next is the linear regulator which further steps down the voltage to 5 V and again reduces noise. Lastly the charge pump inverter was implemented at the end so there could be a negative 5 V rail for the future use of operational amplifiers.

Chapter 2

Rectifier

2.1 Theory and releated work

The voltage rectifier did not require a lot of theory or background research since the circuit design is trivial at most. The only source that was referred to was the datasheet for the 1N4007 diode [1].

2.2 Design

The design principle for the rectifier was relatively simple. Select the correct diode to rectify the negative component of the AC signal and note the voltage drop over the diode. Since the switchmode regulator requires a large input capacitor, there was no need for another capacitor on the output of the diode rectified signal. The value of C1 in figure 2.1 was taken from the design of the switchmode regulator in section 3.2 far surpassed the . The circuit was simulated with an arbitrary load of 1 kΩ.

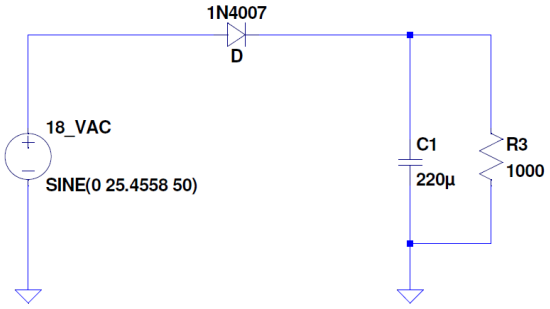


Figure 2.1: Rectifier circuit

2.3 Simulation

The simulation output was as expected, with the ripple voltage at 1.7 V. Figure 2.2 below was taken from the LTspice simulation of the circuit.

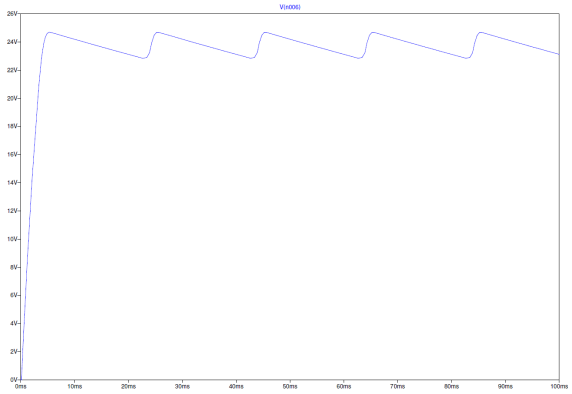


Figure 2.2: Rectifier ripple voltage

2.4 Measurements

The ripple voltage was measured as 8.8 VDC. This big difference to the simulation can be explained, since at the time of measuring the practical circuit, the charge pump and switchmode were already implemented as well. Since these two circuits have a lower combined input resistance than what what was tested in the simulation, the ripple voltage is much larger than that found in LTspice (1 kΩ input resistance). The following figure shows the measured results from the oscilloscope.

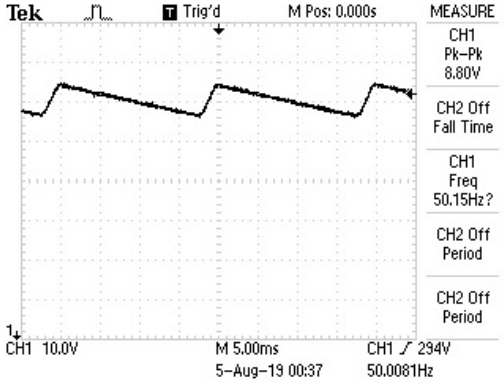


Figure 2.3: Rectifier circuit ripple measurement

Chapter 3

Switchmode regulation

3.1 Theory and related work

Once the switchmode was decided to be the next circuit component, as mentioned in section 1.2, certain choices had to be made with regards to the setup of the regulator. The datasheet proved very useful and was the only reading material referred to for theoretical background.[?]

3.2 Design

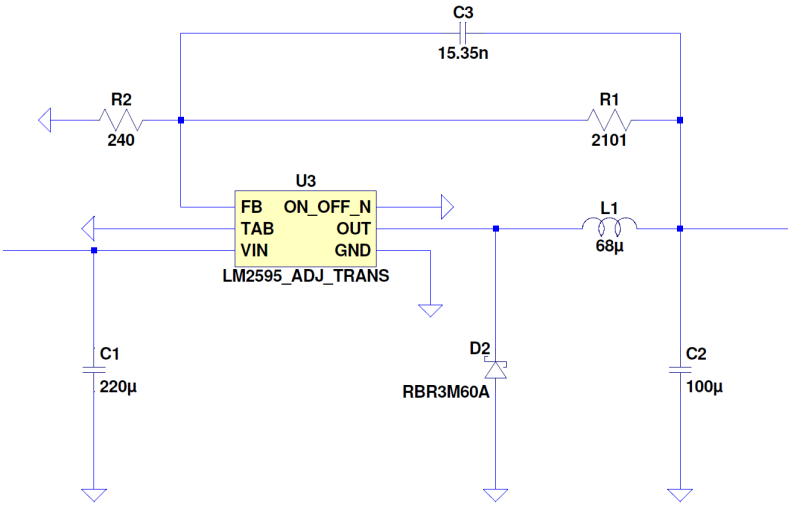


Figure 3.1: Switchmode regulator circuit

Firstly the mode of operation of the switchmode had to be chosen. I decided to choose a 12 VDC adjustable output for which the circuit design can be found in the datasheet of the LM2925 switchmode regulator[**?**]. This circuit design was replicated in my simulation and practical realisation of the circuit. Since the circuit design was taken straight from the datasheet motivations for circuit components are only mentioned where necessary however all calculations are shown.

The design process for this selected mode of operation is vaguely outlined in the datasheet. The next step in the design process was to select resistor values R1 and R2 which can be seen in figure 3.1. R1 was selected as recommended to be as close to 240 Ω as possible since the smaller R1 is the less noise in the output of your switchmode regulated voltage[**?**]. The value for R1 was chosen to be 270 Ω since this was the closest available resistor value. From here the calculation of R2 was made using the following equation

$$V_{out} = V_{ref} \cdot (1 + \frac{R_2}{R_1}) \tag{3.1}$$

Where V_{ref} is 1.23 V and the required V_{out} is 12 V. This gave a R2 value of 2364 Ω which was also rounded to the nearest available resistor value of 2200 Ω which was selected for R2. From here the next step was to select the inductor value L1. First a volt-microsecond constant was calculated using an equation from the datasheet[2].

$$E \cdot T = (V_{in} - V_{out} - V_{sat}) \cdot \frac{V_{out} + V_D}{V_{in} - V_{sat} + V_D} \cdot \frac{1000}{150kh_z} \tag{3.2}$$

Given this newly calculated constant and the maximum load current 1 A and inductor value of 68 mH was found from table 3 in the datasheet[**?**]. The next design consideration was for the output capacitor C2 which was selected from table 7 from the datasheet[2] to be 120 µA. The purpose for capacitor C3 is to provide voltage stabilty since the chosen output voltage was higher than 10 V[2]. It was calculated to be 15.35 nF using the simple equation 3.3 given in the datasheet[2].

$$C_{FF} = \frac{1}{31 \cdot 10^3 \cdot R_2} \tag{3.3}$$

The last design calculation was for the input capacitor C1. Its value was chosen with respect to the RMS value of the input current which is basically an evaluation of power. Since the maximum current would be 1 A, the corresponding input capacitor value according to the datasheet was 220 µF. The only further design was for the zener diode D2 which was provided in the list of components and therefore required no calculations.

3.3 Simulation

For the LTspice simulation of the switchmode circuit, the aim was to see if the 12 V output has minimally sufficient noise and had small enough current as to not over exert the transformer which can only safely supply approximately 100 mA. Figure 3.2 shows the output voltage over a dummy 100Ω load.

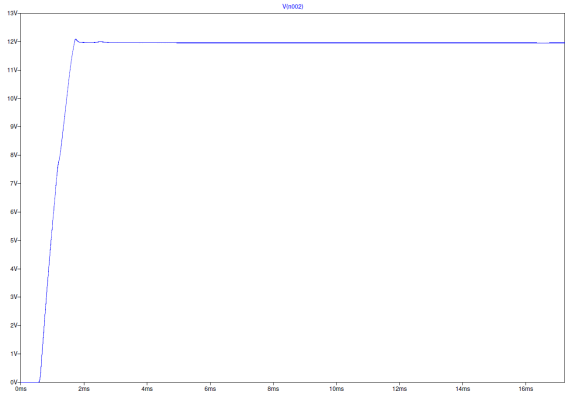


Figure 3.2: Switchmode output LTspice simulation

3.4 Measurements

The noise limitation requirement of the circuit could only be analysed by practical measurements. As seen in figure 3.3, the practical realisation of the switchmode regulator was successful with a noise level of less of roughly 69.6mV. The current draw from the 18 VAC transformer was well below the 100 mA guideline. The 12 VDC had a settling time of roughly 2 ms.

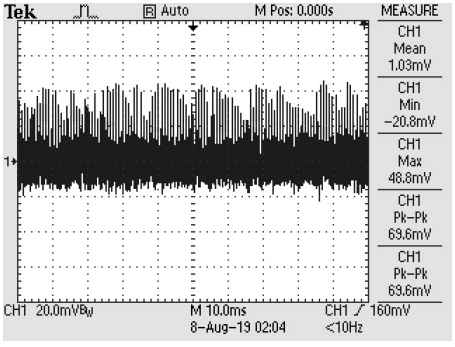


Figure 3.3: Switchmode output noise

Chapter 4

Linear regulation

4.1 Theory and releated work

The background work that was done for the linear regulator entailed referencing the previous semester's E-design module 314 in which we designed a 5 V linear regulator. The circuit design and basic principles were taken from this. The datasheet for the linear regulator was also briefly examined.[3]

4.2 Design

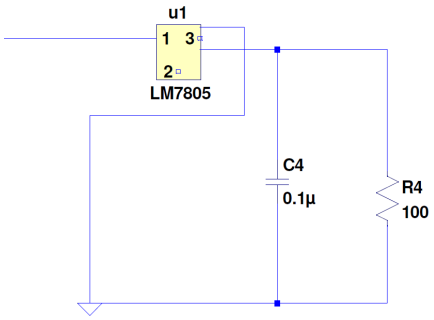


Figure 4.1: Linear regulator circuit

The linear regulator circuit design was taken form the recommended circuit in figure 2 of the datasheet[3]. The theory behind the design will therefore not be covered. May it be known that there was no input capacitor in the circuit design since due to the presence of C2 from chapter 3 in the switchmode regulator circuit.

The value for C4 was taken from the recommend value in the datasheet.[3] R4 was used to test the circuit in simulation.

4.3 Simulation

The simulation in LTspice was run with the both the rectifier and switchmode regulator connected prior to the linear regulator. The simulation's results were as expected.

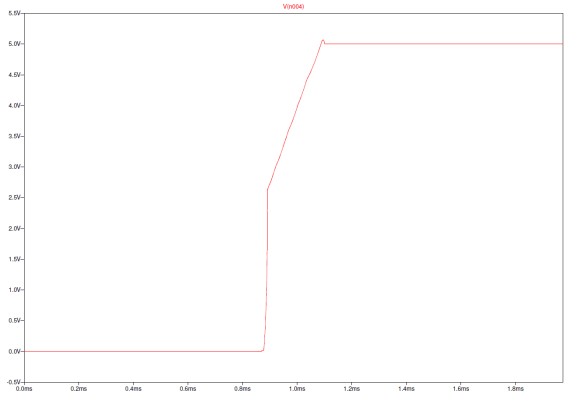
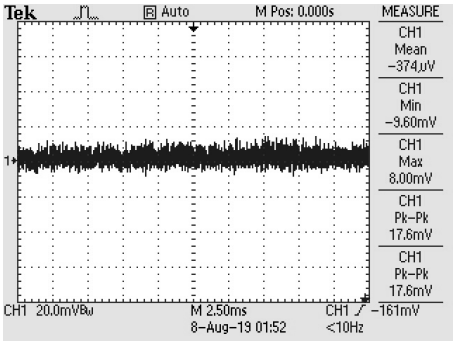


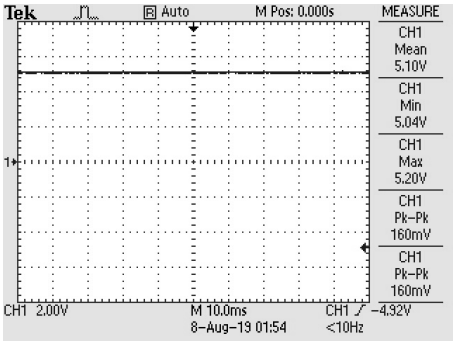
Figure 4.2: Linear regulator circuit

4.4 Measurements

The aims of the measurements of the practical linear regulator circuit, were to analyse and minimise noise, as well as output 5 VDC. As seen in figure 4.3 the



(a) 5V rail peak-to-peak noise



(b) Positive 5V rail

noise was recorded to be 17.6 mV peak-to-peak which is good although, not as accurate as expected. The FFT of the signal noise was analysed, but no significant frequency signature could be identified. However, a simple explanation could be that the various wires, which vary up to a few centimeters in length, could be receiving EM interference from the capacitors and more likely the inductor L1.

Chapter 5

Charge pump regulation

5.1 Theory and releated work

The first step of the preparation for designing the charge pump was finding out what a charge pump was and how it worked to create a negative 5 V rail. It was found that it is a simple principle of switching a signal to charge and discharge a combination of capacitors relative to ground to build up a negative voltage[4].

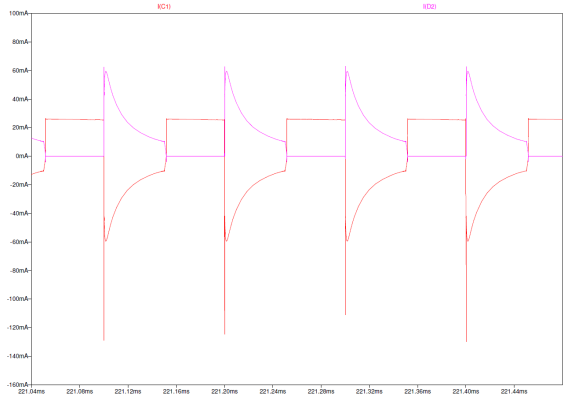


Figure 5.1: Current through C1 and D2 per charge pump cycle

The theory of the circuit design is one based on logic which entails the charging and discharging of C1 through D1 and C2 through D2. In figure 5.2 the theoretical logic can be seen for the diode configuration, which shows $I(C1)$ in red and in purple $I(D2)$. Per each 5 V pulse of the pulse train, C1 charges through D1 to ground. When the pulse goes low (0 V) C1 discharges into C1 giving an output voltage of -5 V after the diode voltage drops have been negated.

5.2 Design

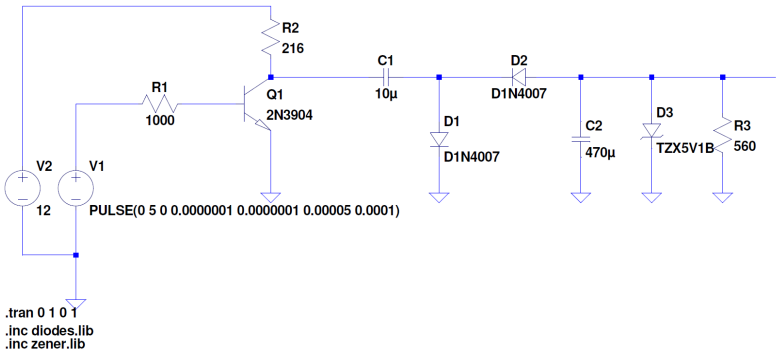


Figure 5.2: Charge pump circuit

The circuit layout in figure 5.1 became the final design for the charge pump after a few trial and error attempts.

R1, the base resistor for the 2N3904 transistor Q1, was implemented for the limitation of the base current caused by the simulated pulse train.

R2 was used to limit the current through Q1 accord to its power rating taken from the datasheet[5]. The absolute max colector current is 200 mA and so the R2 was designed to make the current 50 mA which, using ohm's law with the 12 V input from the switchmode regulator, gave a R2 value of 250 Ω, but it was further discovered that this current directly affects the output current and therefore it was minimised to 216 Ω since the output current needs to be large enough to supply multiple op-amps which require a maximum of 2.7 mA each.

Capacitor C1 had to be small enough to charge and discharge quickly with respect to the frequency of the input pulse train (which was chosen to be 10 kHz to avoid high frequency interference from other components). It had to create a smaller time constant than the period of the pulse train which is 100 µs. One tenth of this period was chosen giving 10 µF.

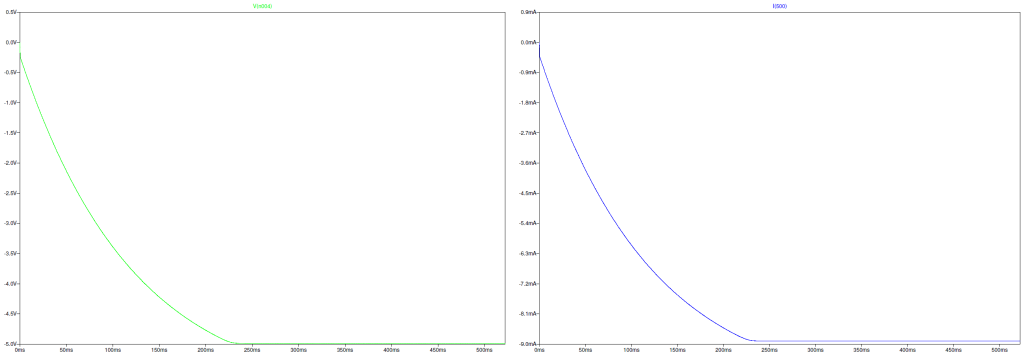
The diode configuration contains D1 and D2 1N4007 diodes which were supplied and therefore chosen by default.

Capacitor C2 had to be large enough to have no ripple effect on the output voltage as well as small enough to reach the desired output voltage within a realistic time frame. 470 µF was selected to create a time constant of 0.25 s which was deemed small enough. This value also created no noticeable ripple voltage in the output.

Zener diode D3 keeps the output voltage constant at -5 V. Load resistor R3 is used to approximate a load resistance that the charge pump will need to supply.

5.3 Simulation

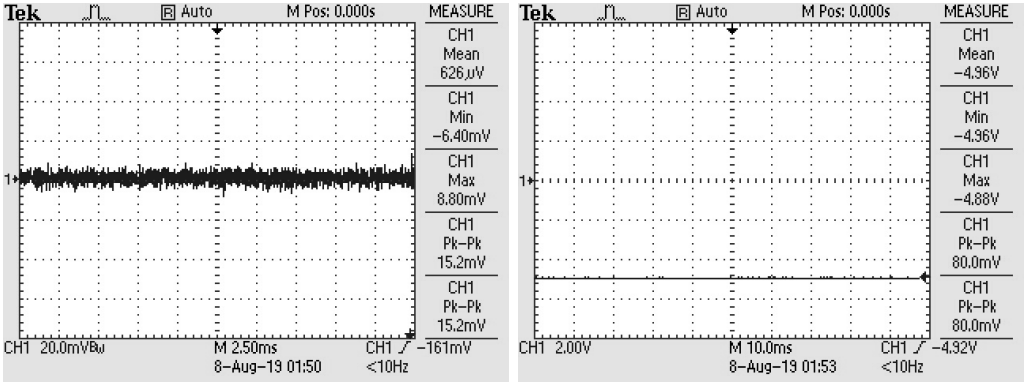
The 3 requirements of the charge pump were constant output of -5 V, sufficient output current and minimal output noise. The prior 2 of these 3 were simulated and tested for in LTspice. The output current was simulated at 9 mA. The output voltage was just large of -5 V.



(a) Output voltage (b) Output current

5.4 Measurements

The measurement of the output noise of the negative 5 V rail as seen in figure (a) is 15.2 mV peak-to-peak. This was as low as I could get my circuit to have although I would have liked less than 10 mV. The addition of bypass capacitors for certain frequencies were tested, but no success became of it. The rail sat at -4.96 V which was satisfactory.



(a) Negative 5V rail peak-to-peak noise (b) Negative 5V rail

Chapter 6

System test results

With all the circuits joined together as per figure 1.1 to create the entire power supply, there was no difference in the practical realisation of the circuit and the values that were recorded in each chapter of this report. No changes were made and the final build of the circuit can be seen in figure 6.1. All of the sub-circuits of the power supply are connected to the same ground.

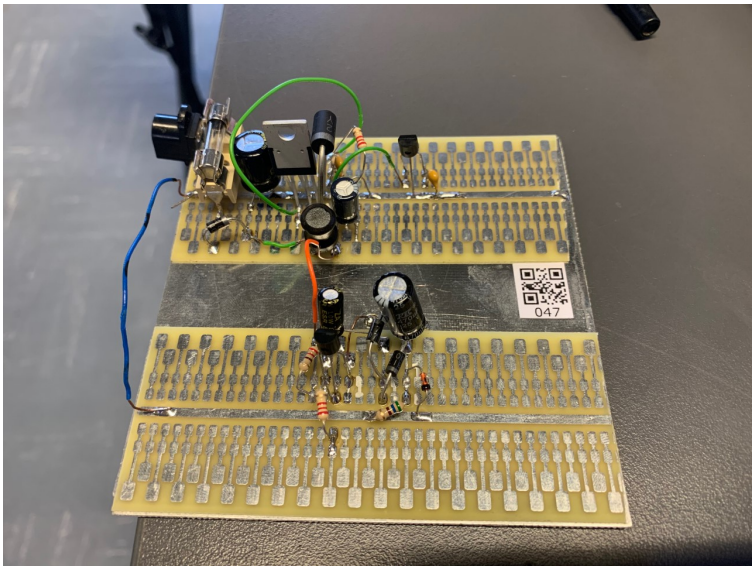


Figure 6.1: Practical circuit

References

[1] Diodes Incorporated: 1n4007 datasheet. 2014.
Available at: https://www.diodes.com/assets/Datasheets/ds28002.pdf

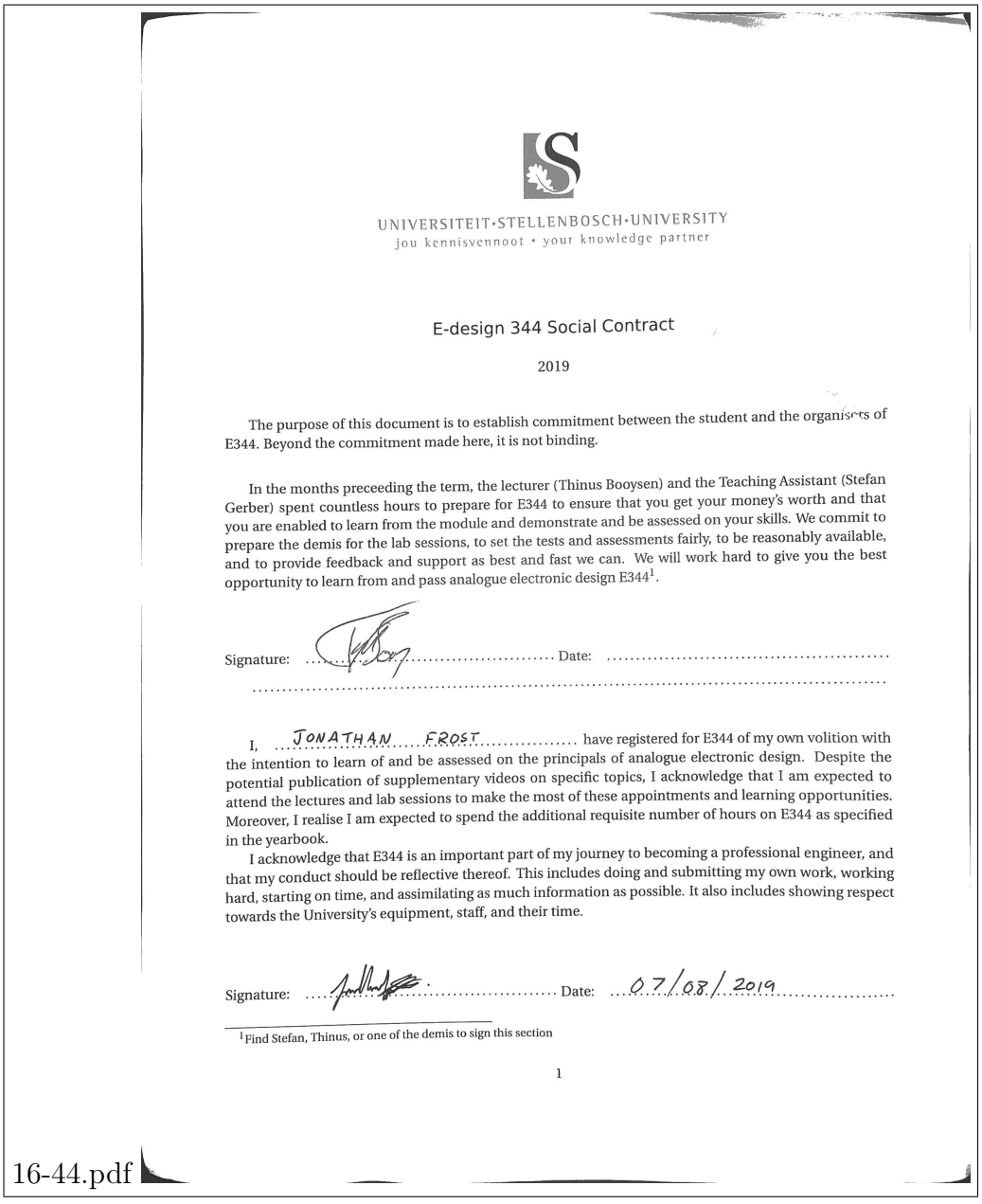
[2] Texas instruments: Lm2595 simple switcher power converter 150-khz 1-a step-down voltage regulator. 2016.
Available at: https://learn.sun.ac.za/pluginfile.php/1690421/mod$_r esource/content/0/lm2595.pd$

[3] Fairchild semiconductor corporation: Lm78lxxa 3-termnal 0.1 a positive voltage regulator. 2013.
Available at: https://learn.sun.ac.za/pluginfile.php/1690414/mod$_r esource/content/0/MC78L05$

[4] Lou Frenzel: The charge-pump option to ldo and inductor-based regulatorsv. 2016.
Available at: https://www.electronicdesign.com/power/charge-pump-option-ldo-and-inductor-ba

[5] ON semiconductor: General purpose transistors. 2012.
Available at: https://www.onsemi.com/pub/Collateral/2N3903-D.PDF

Appendix A: Social contract



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E-design 344 Social Contract

2019

The purpose of this document is to establish commitment between the student and the organisers of E344. Beyond the commitment made here, it is not binding.

In the months preceeding the term, the lecturer (Thinus Booysen) and the Teaching Assistant (Stefan Gerber) spent countless hours to prepare for E344 to ensure that you get your money's worth and that you are enabled to learn from the module and demonstrate and be assessed on your skills. We commit to prepare the demis for the lab sessions, to set the tests and assessments fairly, to be reasonably available, and to provide feedback and support as best and fast we can. We will work hard to give you the best opportunity to learn from and pass analogue electronic design E344[1].

Signature: ..... Date: .....

I, JONATHAN FROST have registered for E344 of my own volition with the intention to learn of and be assessed on the principals of analogue electronic design. Despite the potential publication of supplementary videos on specific topics, I acknowledge that I am expected to attend the lectures and lab sessions to make the most of these appointments and learning opportunities. Moreover, I realise I am expected to spend the additional requisite number of hours on E344 as specified in the yearbook.

I acknowledge that E344 is an important part of my journey to becoming a professional engineer, and that my conduct should be reflective thereof. This includes doing and submitting my own work, working hard, starting on time, and assimilating as much information as possible. It also includes showing respect towards the University's equipment, staff, and their time.

Signature: ..... Date: 07/08/2019

[1] Find Stefan, Thinus, or one of the demis to sign this section

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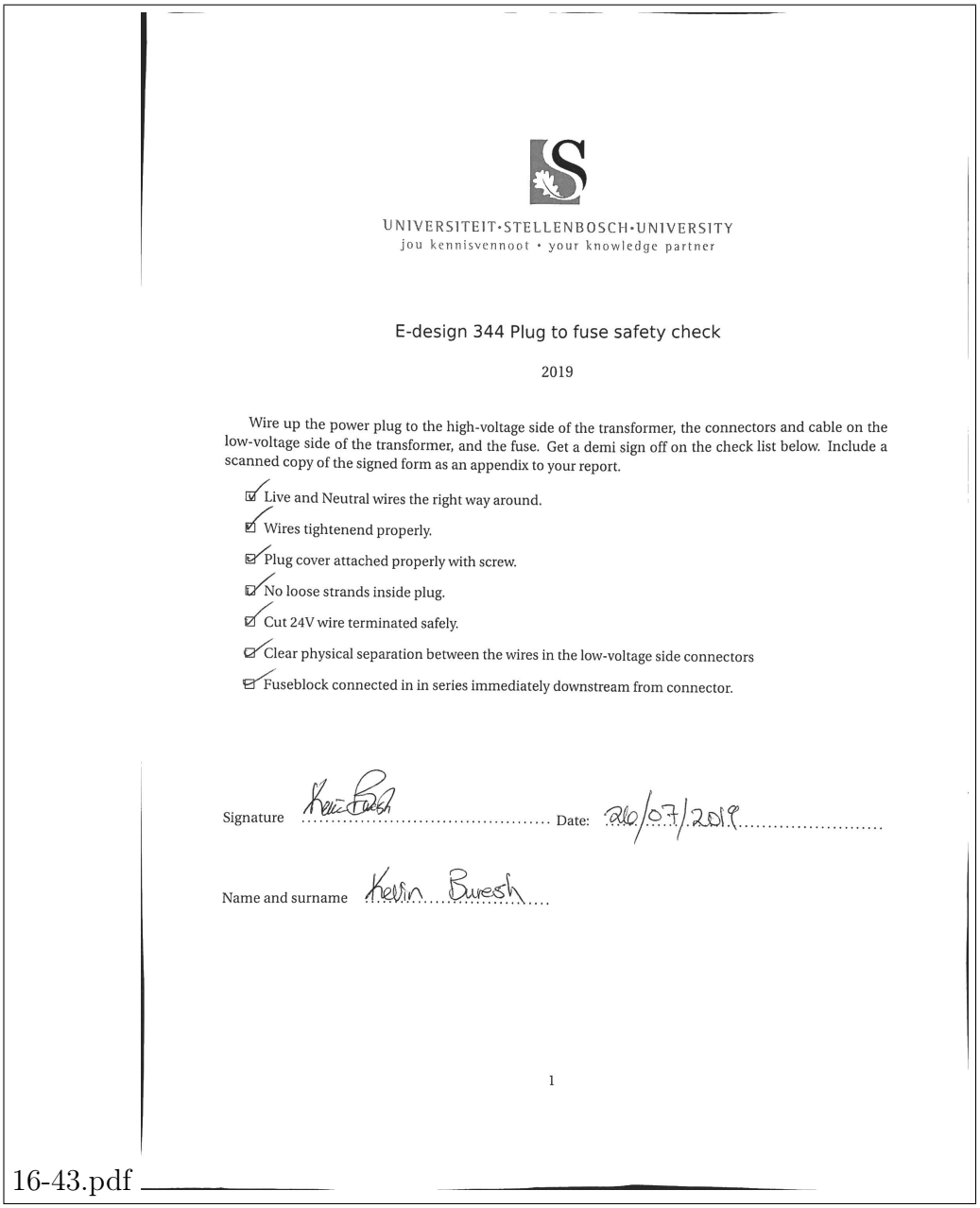
Appendix B: Wiring safety check



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E-design 344 Plug to fuse safety check

2019

Wire up the power plug to the high-voltage side of the transformer, the connectors and cable on the low-voltage side of the transformer, and the fuse. Get a demi sign off on the check list below. Include a scanned copy of the signed form as an appendix to your report.

- ☑ Live and Neutral wires the right way around.
- ☑ Wires tightenend properly.
- ☑ Plug cover attached properly with screw.
- ☑ No loose strands inside plug.
- ☑ Cut 24V wire terminated safely.
- ☑ Clear physical separation between the wires in the low-voltage side connectors
- ☑ Fuseblock connected in in series immediately downstream from connector.

Signature Kevin Buresh Date: 26/07/2019

Name and surname Kevin Buresh

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Appendix C: Screengrab of GitHub repo