ECE 3544: Digital Design I
Project 4 – Design and Synthesis of a Synchronous Finite State Machine

Student Name: **Jonathan Lemarroy**

Honor Code Pledge: I have neither given nor received unauthorized assistance on this assignment.

Jonathan Lemarroy

Grading: The design project will be graded on a 100 point basis, as shown below:

Manner of Presentation (30 points)

_____ / 5   Completed cover sheet included with report

_____ / 15   Organization: Clear, concise presentation of content; Use of appropriate, well-organized sections

_____ / 10   Mechanics: Spelling and grammar

Technical Merit (70 points)

_____ / 5   General discussion: *Did you describe the objectives in your own words? Did you discuss your other conclusions and the lessons you learned from the assignment?*

_____ / 10   Design discussion: *Did you discuss the approach you took to designing and implementing the modules that make up your system, and how you synthesized the system from its components?*

_____ / 5   System controller state diagram: *Does your state diagram model a system that performs the required tasks? Connect this discussion to your design discussion*.

_____ / 5   System block diagram: *Connect the system block diagram to your design discussion – specifically, to a discussion of how your system employed communicating state machines to implement the tasks required by the specification.*

_____ / 5   Testing discussion: *What was your approach to formulating your test benches? How did you verify the correctness of the modules you designed? What were the results of the test of your counter's accuracy? Did you comment on the significance of these results?*

_____ / 10   Supporting figures: *Waveforms showing correct operation of the top-level module.*

_____ / 30   Validation of the final design on the DE1-SoC board

_____   **Project Grade**

GTA Validation Instructions:

Program the FPGA on the DE1-SoC Nano board with the student's implementation of the stopwatch system. When the programming has successfully completed, perform the set of tests described in the table below. For each case, indicate whether or not the student' design demonstrates the behavior described.

Procedure and *Expected Result*	Correct Operation (**Yes** or **No**)
Press and release KEY3. *The Mode Indicator should show a steady, upper-case S. The stopwatch should read 0000.*	
Press and release KEY1. *The Mode Indicator should show a flashing, upper-case S, flashing at about 2 Hz. The stopwatch should start counting as a decimal time counter.*	
Using a clock that can count seconds, use the clock to measure ten seconds from when KEY1 was released in the previous step. At the end of ten seconds, press and release KEY0 to stop the timer. **Is the timer reasonably accurate?**	
Press and release KEY1. *The Mode Indicator should show a flashing, upper-case S. The stopwatch should continue counting from its previous value.*	
Press and release KEY1. *The Mode Indicator should show a flashing, upper case S. The stopwatch should hold the value of when KEY1 was released for about 5 seconds, and then go back to counting at the proper time of that value plus 5 seconds.*	
Press and release KEY2. *The Mode Indicator should show a flashing, upper case L. The stopwatch should continue counting with no interruption.*	
Press and release KEY1. *The Mode Indicator should show a flashing, upper case L. The stopwatch should hold the value of when KEY1 was released for about 5 seconds, and then go back to counting at the proper time of that value plus 5 seconds.*	
Using a clock that can count seconds, use the clock to measure 30 seconds from when KEY1 was released in the previous step. At the end of 30 seconds, press and release KEY1. *The Mode Indicator should show a flashing, upper case L. The stopwatch should hold a value of about 30 seconds for about 5 seconds, and then go back to counting at the proper time.*	
Press and release KEY2. *The Mode Indicator should show a flashing, upper-case S. The stopwatch should continue counting with no interruption.*	
Allow the stopwatch to continue running so that more than 1 minute elapses since the beginning of the test. *The stopwatch should roll-over at 1 minute from the value 0599 (0 minutes 59.9 seconds) to 1000 (1 minute 00.0 seconds).*	
Press and release KEY0. *The Mode Indicator should show a steady, upper-case S. The stopwatch should halt counting.*	
Press and release KEY0 again. *The Mode Indicator should show a steady, upper-case S. The stopwatch should read 0000.*	
Press and release KEY2. *The Mode Indicator should show a steady, upper-case L. The stopwatch should read 0000.*	

Purpose:

This assignment was made to gain experiences in designing and synthesizing large-scale synchronous systems using smaller finite state machines.

Project Description:

Design and synthesize a stopwatch using Verilog that has two modes split and lap, whose inputs are as seen in **Figure 1**.

Figure 1: Stopwatch I/O
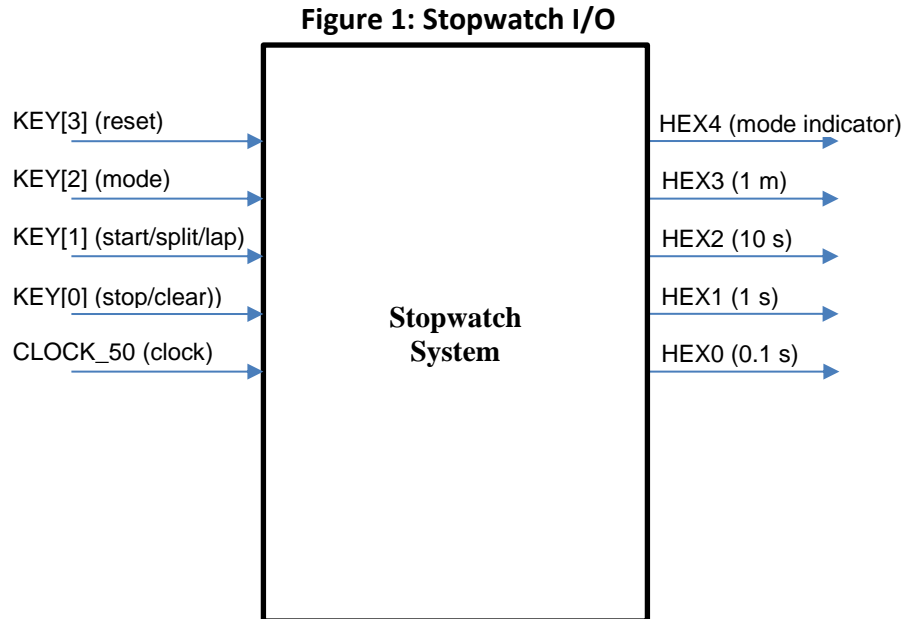
The split mode is the time calculated from when the timer began, whereas the lap mode is only the time measured for each lap. The stopwatch should be operated using in a manner which is found in **Figure 2**. And when the timer is running the mode indicator (HEX4) should be flashing every other second else be kept on.

Figure 2: States of Operation
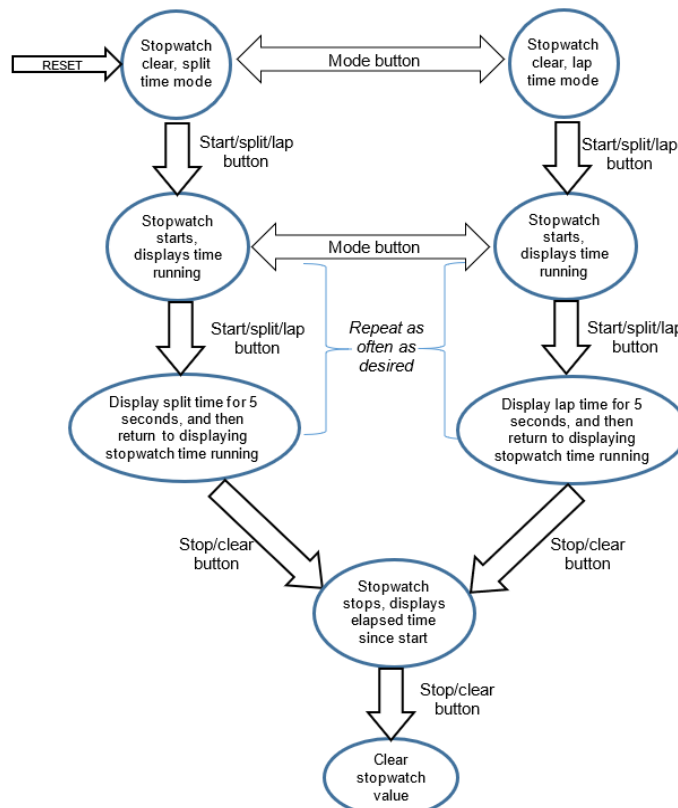
Technical Design:

Unfortunately, due to lack of time this project was not fully implemented (spent my break without a working computer). But the synchronous ten-minute timer portion of this was completed and has an included test bench for it.

Analysis & Conclusion:

Nothing to analyze or conclude.