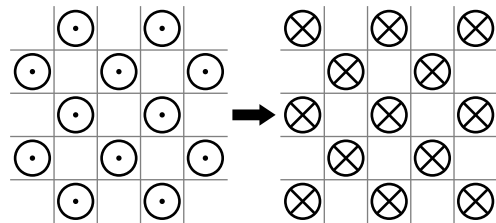


Input cycle A

(bit 0)

First
substep

Second
substep



Input cycle B

(bit 1)

First
substep

Second
substep

