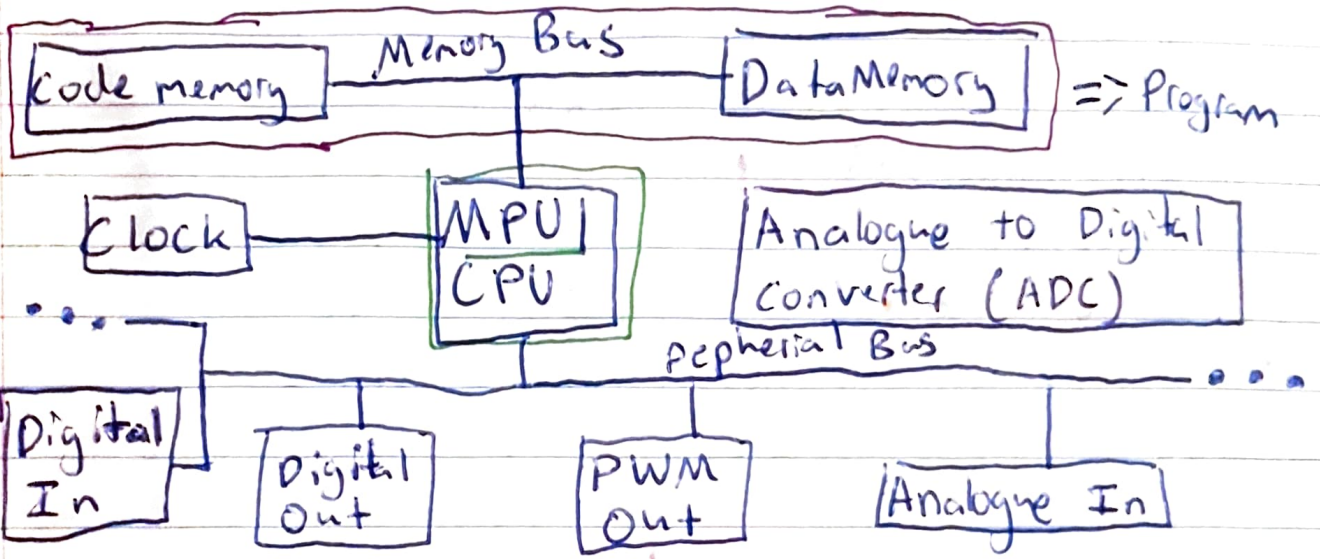
same - CPU = Central processing unit
- MPU = Microprocessor unit
- MCU = Microcontroller unit

2. Arm Intro

• Microcontroller (MCU) vs Microcomputer

(MCU) - Microcontroller = Microprocessor (MPU) + Memory + Perphenls
CPU

- Microcomputer = microcontroller on a single silicon chip



- PWM = Pulse width Modulation

• Progress of MPU and MCU

Our Processor

	Bus width	ROM/sRAM	Internal Peripherals
Tiva C-series	32	4GB + 32 kB	Timer/PWM, ADC, SPI, + ...

Speed (MIPS)	Type	Year (Manuf.)
80	MCU	2015

store firmware Instructions

- MIPS = Million Instructions per Second
- ROM = Read only Memory (Non volitile memory/stores permanetly)
- SRAM = Static Random-Access Memory (CPU cache) (stores until power off)
- DRAM = Dynamic RAM (Needs to be refreshed periodically)
- SPI = Serial Peripheral Interface (short distance communications)

(logical circuits) (capacitors)

• Arm Cortex-M4 Processor

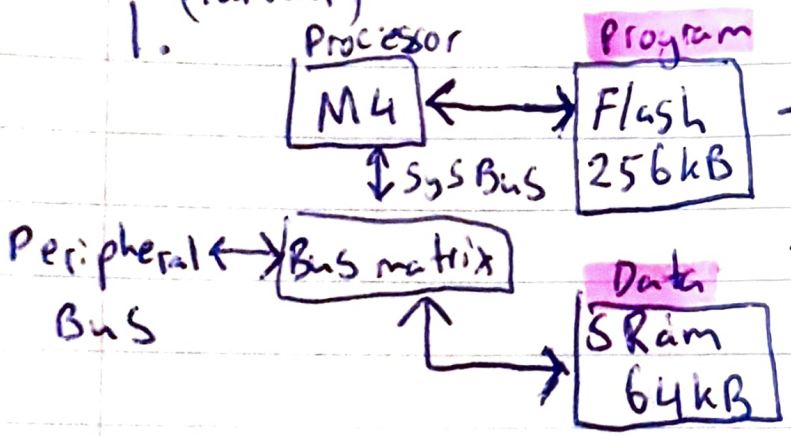
- M4 → like M3 (chip, not New)
- DSP = Digital signal Processing (supported) (contains ADC & DAC converter)
- FPU = Floating Point Unit (carries floating type instructions)
- Faster Floating point calculations
  - more efficient MIPS/mW

(compared to M3 chip)

• MCU Architecture

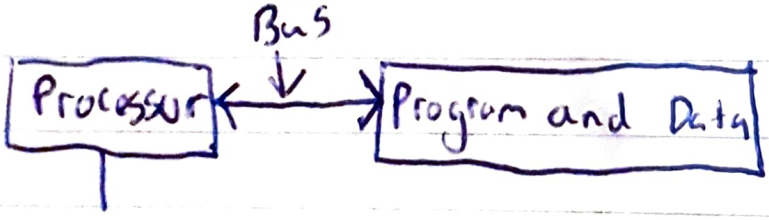
1. - Harvad Architecture (seperate storage)
2. - Von Neumann Architecture (shared storage)

1. (Harvad)



- Seperate storage for program and data.
- Read and Write concurrently

2. (Von Neumann)



- shared storage
- not concurrent

• Peripherial busses

- AHB = Advanced High-performance Bus (Better performance)
- APB = Advanced Peripheral Bus (legacy)

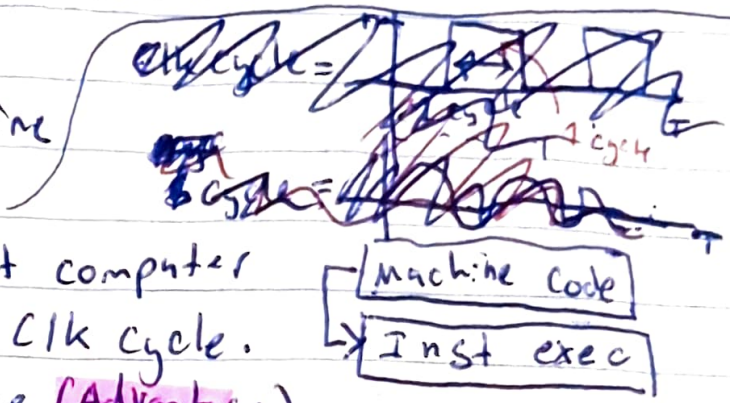
↑ old/Normal

- GPIOs = can either communicate with the AHB or APB.
- 12-Bit ADC = communicates with APB.

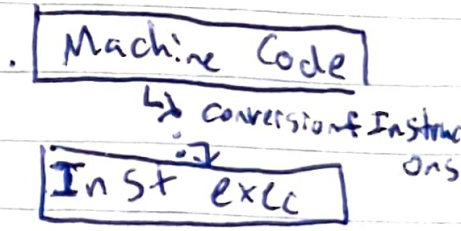
- **Arm Instruction Set** (Not testable

~~R.I.S.C VS~~

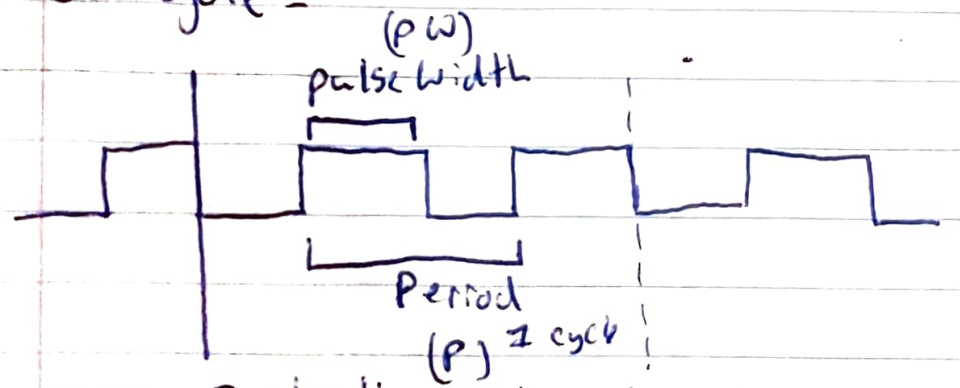
- Arm = Advanced RISC Machine



- **RISC vs CISC**
- RISC = Reduced Instruction Set computer
  - * - One Instruction for 1 Clk cycle.
    - large Code, less hardware (Advantage)
- CISC = Complex Instruction Set computer
  - * - One Instruction for several Clk cycles.
    - less Code, Complex hardware



- Clk cycle =



- ISC = Instruction Set Architecture