Noise in Digital Signals

ENCE361 Embedded Systems 1

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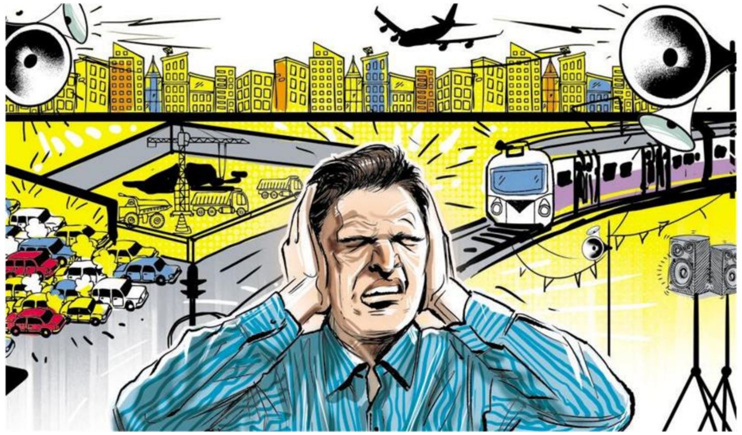
Where we’re going today

- **Sources of noise**
- Signal-to-noise ratio
- Noise margin and hardware interfacing
- Homework

Sources of Noise: Overview

- Definition of noise
  - Disturbance that are unwanted and unrelated to information content <u>in a digital signal</u>

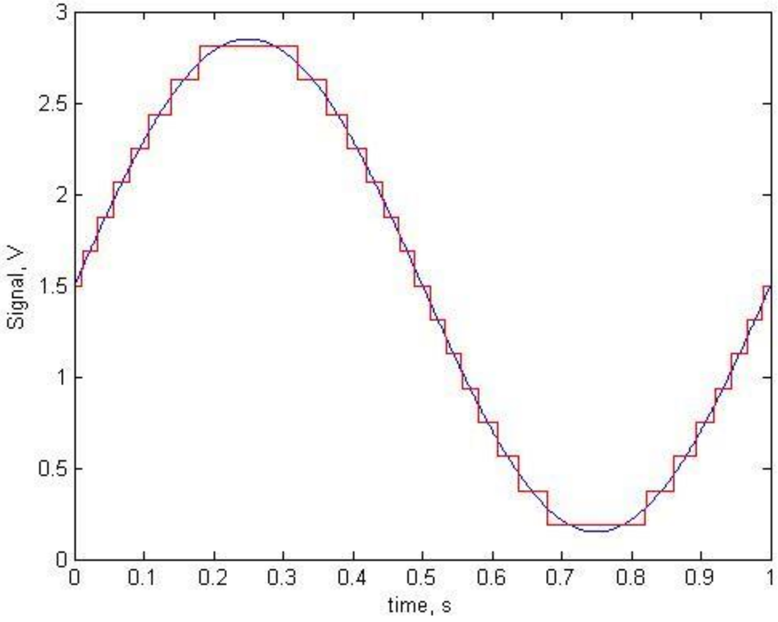
- Random noise vs. systematic error
  - Random noise is stochastic
    - Quantization error
    - Sampling jitter
    - Thermal effect in electronics
    - Interference from other signals
  - System noise is deterministic
    - Measurement offset
    - Non-linear response
    - <u>Generally can be calibrated</u>



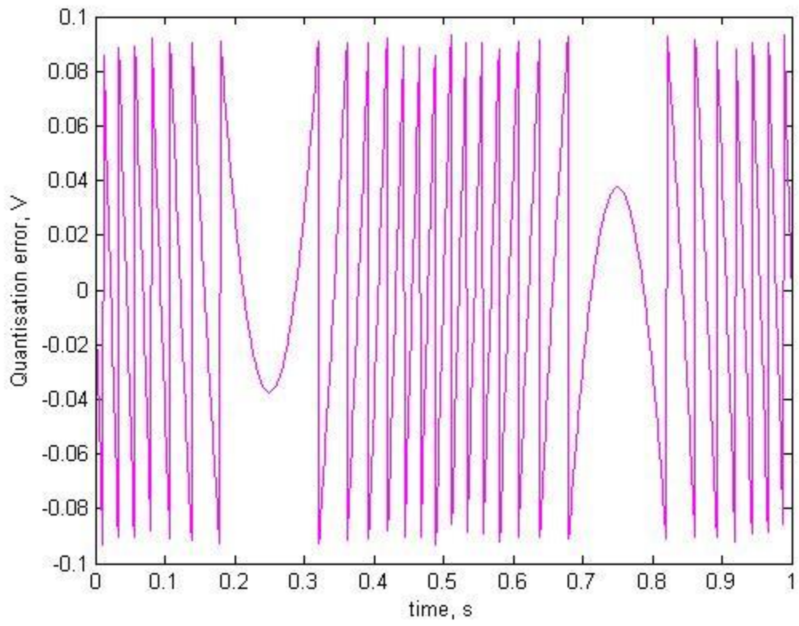
Quantization Error

- Quantization maps a sample value to one of the possible discrete values

Original signal vs. its **ZOH-sampled & quantised version**



Quantization error

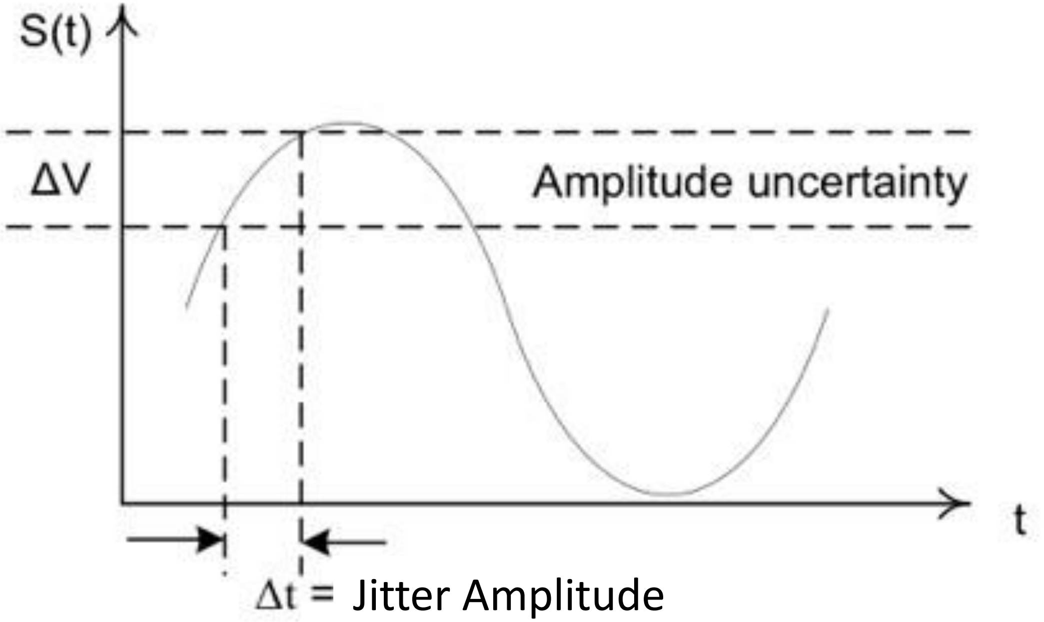


- 4-bit uniform quantization with 16 discrete values
- Quantization step Δ = 3/16 = 0.188 Volt

- Random error with maximum magnitude = Δ/2 = 0.094 Volt

Sampling Jitter

- Sampling jitter makes sampling interval no long uniform



- Effect of sampling jitter
  - Cause sampling amplitude uncertainty
  - Example:

  for a sinewave with amplitude A and frequency f Hz, maximum error magnitude is

  $$\Delta V = 2\pi f A \Delta t$$

  Derivation:

  $A sin(2\pi f t)$ has an instantaneous changing rate $2\pi f A cos(2\pi f t)$.

  Maximum amplitude change after sampling jitter is $2\pi f A cos(2\pi f t) \Delta t \leq 2\pi f A \Delta t$

Johnson Noise

- Thermal noise
  - Due to random thermal motion of charge carriers (usually electrons)
  - Occurs regardless of any applied voltage

- A resistor of resistance *R* generates thermal noise with a RMS voltage

$$v_n = \sqrt{4kTBR}$$

$v(t) = v(t+T)$ T = period

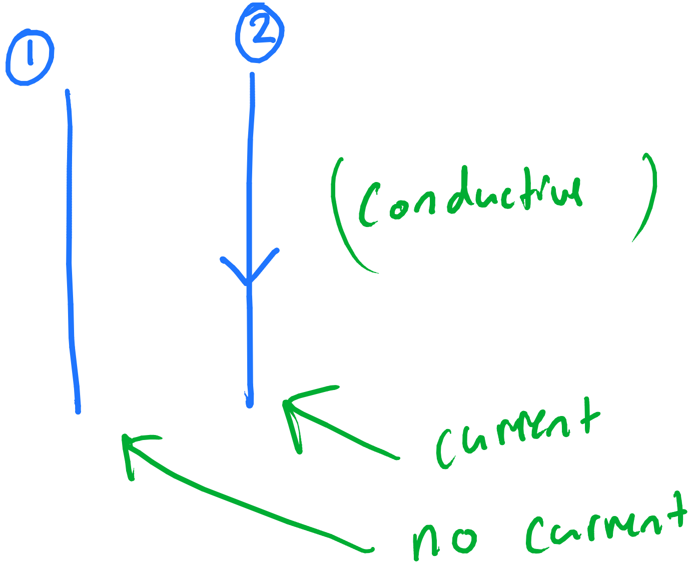
$$\left[\frac{1}{T}\int_0^T v^2(t)\,dt\right]^{1/2}$$

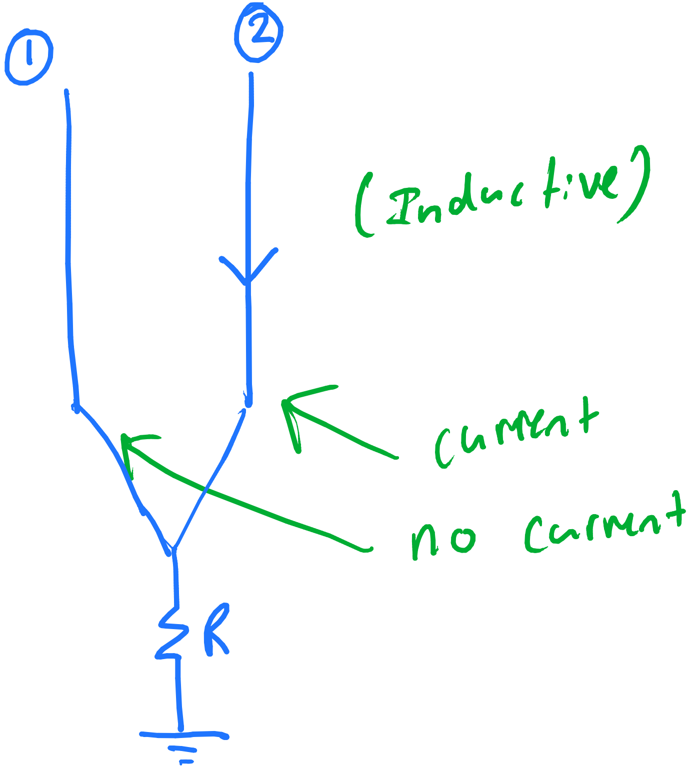
RMS voltage

  - $k = 1.38 \times 10^{-23} J/^{o}K$ Boltzmann's constant
  - T : absolute temperature in ^{o}K (Kelvin)
  - B: noise bandwidth in Hz
  - R: resistance in Ohm

Interference

- 3 sources of interference that could be present simultaneously
  - Conductive coupling: noise current caused by a changing voltage in a nearby circuit
    - Cross-talk between closely spaced circuits
  - Inductive coupling: noise voltage caused by a changing current in a nearby circuit
  - Resistive coupling: occurs when high-level signals share a wire with low-level signals
    - Direct coupling


1
2
(Conductive)
current
no current


1
2
(Inductive)
current
no current
R

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Signal-to-Noise Ratio (1)

- Signal-to-noise ratio (SNR)
  - Expressed in decibel (dB)

0 dB = noise power & signal power is the same

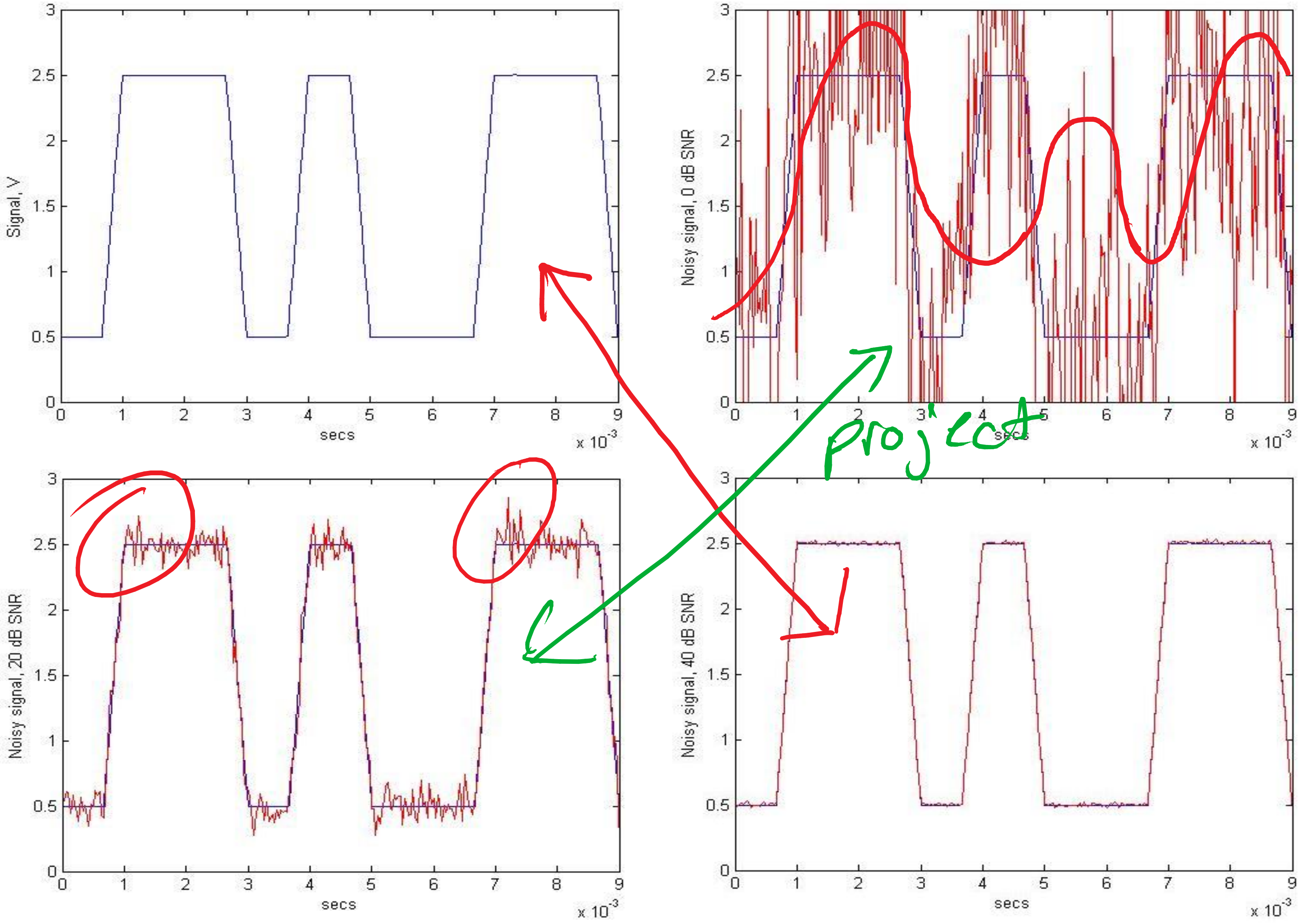
  - Definition 1: $SNR = 10\log\left(\frac{Average\ Signal\ Power}{Average\ Noise\ Power}\right)$
  - Definition 2: $SNR = 10\log\left(\frac{(Signal\ RMS\ Voltage)^2}{(Noise\ RMS\ Voltage)^2}\right) = 20\log\left(\frac{Signal\ RMS\ Voltage}{Noise\ RMS\ Voltage}\right)$

- Use of decibel (dB)
  - Logarithm used to better quantify very large or small values such as SNR

Signal-to-Noise Ratio (2)

"Clean" signal

SNR = 0 dB
Signal & noise have SAME power



SNR = 20 dB
Signal power is 100 times higher than noise power

SNR = 40 dB
Signal power is 100,00 times higher than noise power

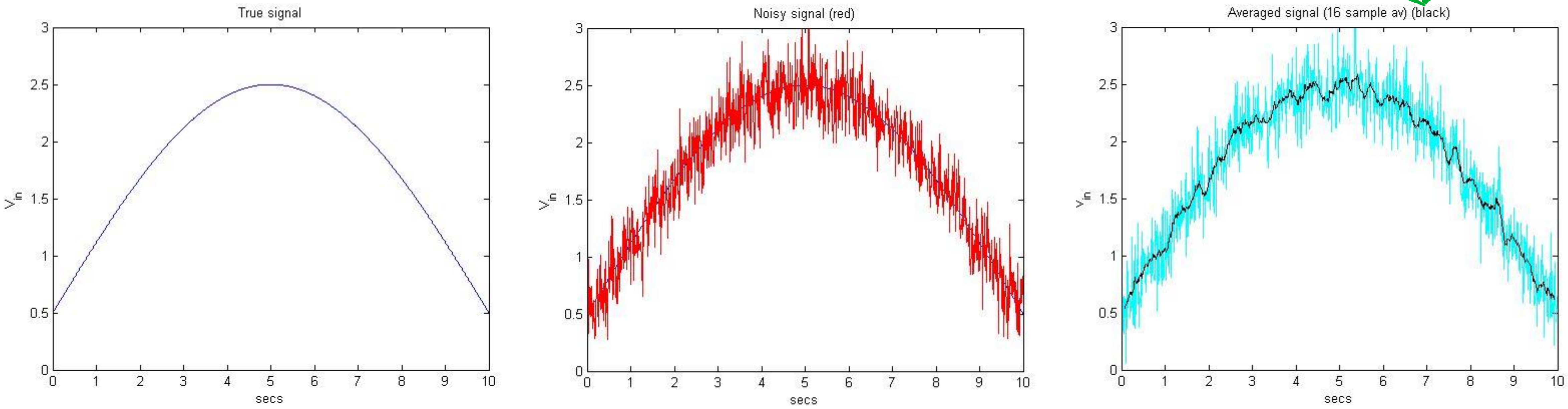
Signal Averaging Revisited (1)

- Digital signal conditioning via signal averaging (slide 15 in previous lecture)

$$z(nT_S) = \frac{1}{M}\sum_{m=0}^{M-1} y((n-m)T_S)$$

- Reduce noise power by a factor of $1/M$ for independent & identically distributed (i.i.d.) noise samples

***M*=16**



$\sin(2\pi \cancel{ft})$ $f = 2.5\,Hz$ $t = 0.01 \Rightarrow \frac{1}{2.5} \times 100 = 40$

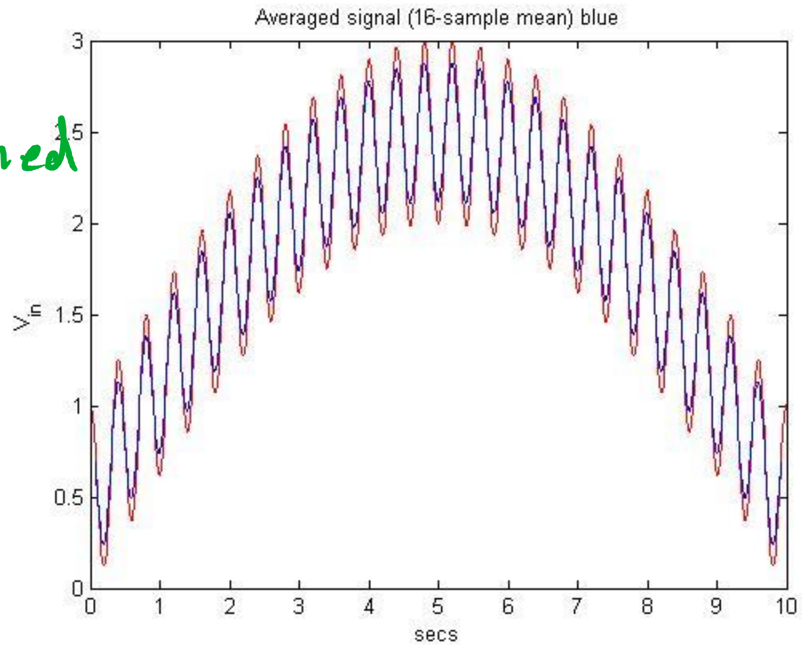
$M = 16$

Signal Averaging Revisited (2)

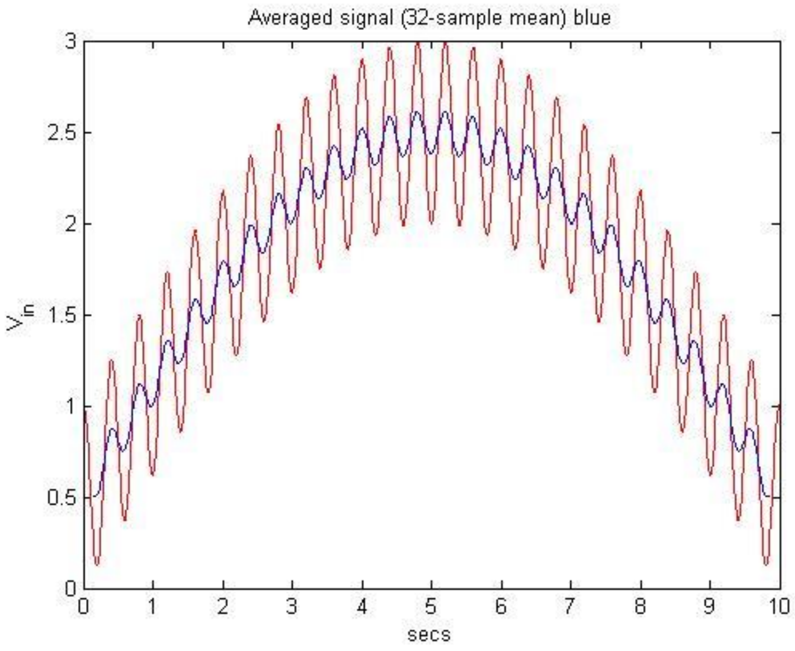
- If the noise is NOT random, the performance of signal averaging may depend on the noise period (in samples) and its relation to M

Red = corrupt
Blue = obtained

M=16



M=32



- Sample the signal at a sampling rate f_s= 100 Hz (T_s = 0.01s)
- The noise is a sinewave at 2.5Hz

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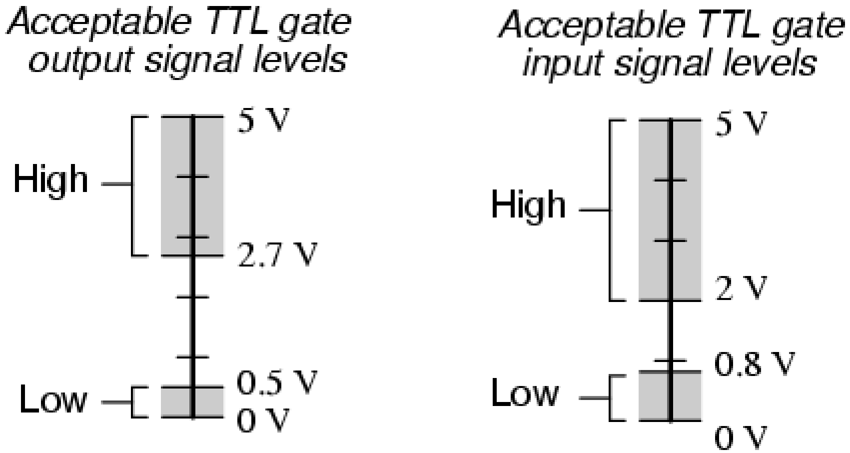
Noise Margin (1)

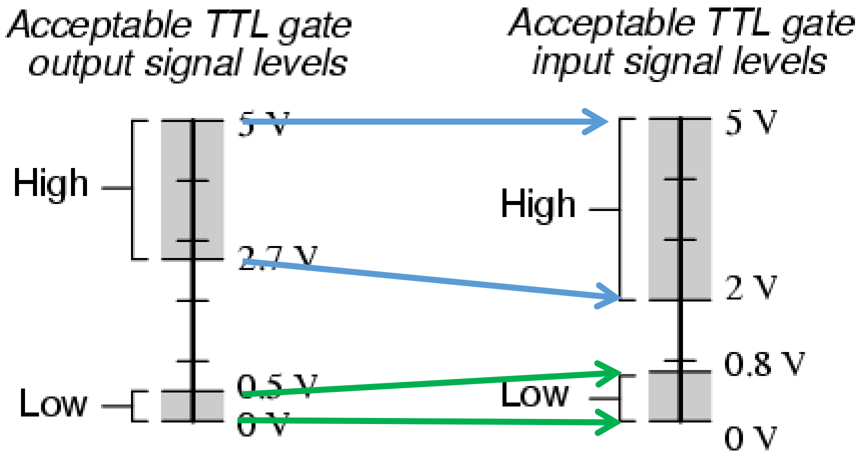
ttL = transitor to transitor logic

- Logic gate circuits output and input logic-1 ('High') and logic-0 ('Low')
  - Ideally, logic-1 is represented by full power supply voltage (say, 5 V)
  - Ideally, logic-0 is represented by zero voltage
- Ideal voltages are rarely attained in practice



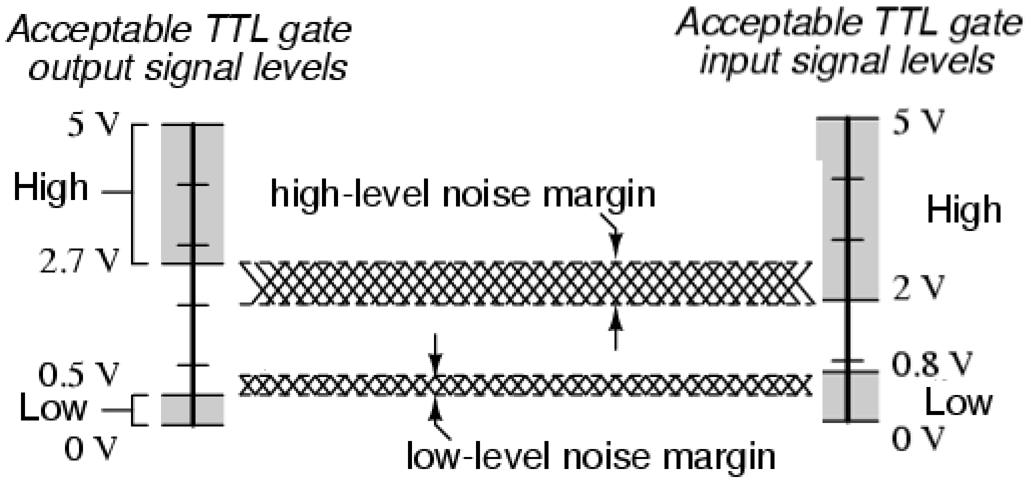
2.7-5 V: High
0-0.5 V: Low

2-5 V: High
0-0.7 V: Low
0.7-2 V: No certain response!

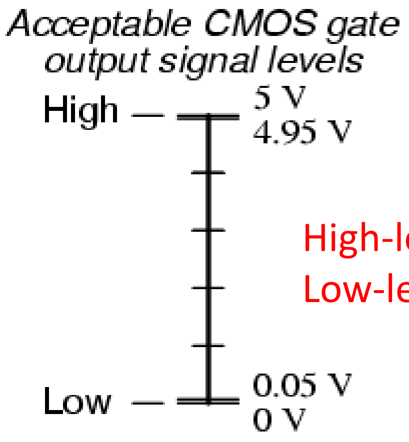


Connect a TTL output to a TTL input

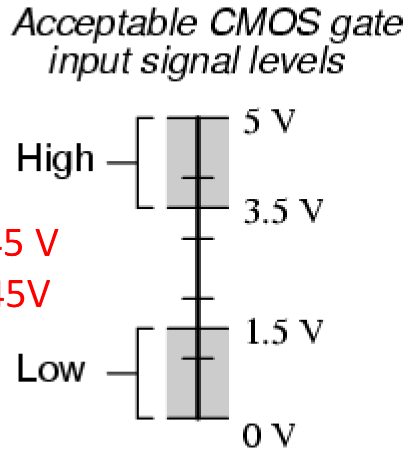
Noise Margin (2)



- High-level noise margin in TTL (transistor-transistor logic) = 2.7-2 = 0.7 V
- Low-level noise margin in TTL (transistor-transistor logic) = 0.8-0.5 = 0.3 V

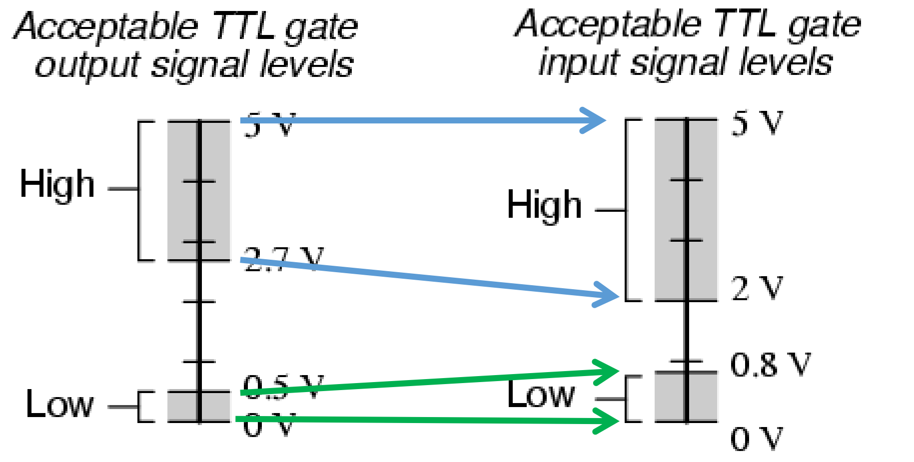


High-level noise margin =1.45 V
Low-level noise margin =1.45V

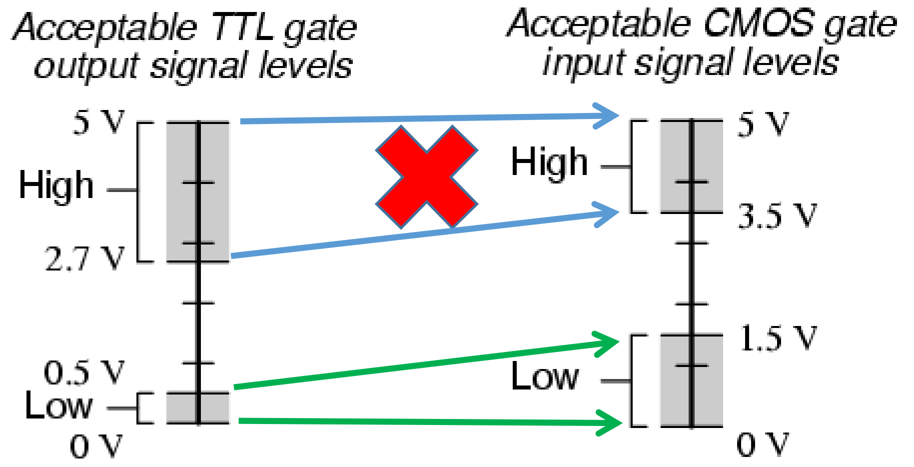


Hardware Interfacing

- Compatible hardware interfacing
  - High-level output range ⊂ High-level input range
  - Low-level output range ⊂ Low-level input range



- Incompatible hardware interfacing
  - Cause <u>uncertain response</u> at CMOS gate when TTL gate outputs logic-1 even without noise



https://www.allaboutcircuits.com/textbook/digital/chpt-3/logic-signal-voltage-levels/

Homework

1. A primary source of noise in resistors is due to thermal (Johnson) noise
   - What is the noise RMS voltage of a 1 MΩ resistor at 300° K over a 100 kHz bandwidth?
   - What is the noise RMS voltage of a 1 MΩ resistor in parallel with a 1 kΩ resistor at 300° K over a 100 kHz bandwidth?

2. In the example with SNR = 20 dB shown on slide 12, the average power of the signal is 0.9 W (ignoring the DC offset). What is the average power of the noise?

3. In slide 13, explain why the noise amplitude on the right (obtained via signal averaging with M=32) is significantly less than that on the left (obtained via signal averaging with M=16).