Terminology used in ENCE361

last altered 13.6.2016

Term(s)	Definition	
peripheral	A device which provides an external interface to the processor.	
interrupt service routine (ISR) interrupt handler	A function (void / void) which is designed to deal with a specific interrupt; the address of its first executable instruction is stored as the interrupt vector.	
interrupt vector table	The array in memory of the interrupt vectors (ISR addresses).	
interrupt latency	The time between an event and the commencement of the prologue for the ISR (worst case).	*
interrupt response time.	The time between an event and the start of execution of the user's ISR code (worst case).	*
interrupt recovery.	The time between an event and the return to the interrupted code (worst case).	*
pre-emption	The switch of execution to a higher priority task, including the handling of a high priority interrupt.	
priority	The importance associated with an interrupt or task, usually encoded as a number with lowest value meaning highest priority.	
interrupt request (IRQ)	The signal indicating an interrupt event has occurred.	
interrupt enable/disable	The mechanism for controlling whether an IRQ is acted upon.	
master enable/disable	A software function call which enables/disables all non-maskable interrupts.	
mask and masking	The name given to the action of setting or resetting a register bit which controls the enable/disable status for a specific interrupt.	
non-maskable interrupt	One of a small number of interrupts too important to be disabled, e.g., reset.	
foreground/background.	Foreground tasks are performed by ISRs; background tasks are all others.	*
context and context switch	The context is the state of the processor at a particular time and comprises the contents of several registers; a switch saves the current context on the stack or reloads a previous context from the stack.	
prologue/epilogue	Prologue: processing for a switch to an ISR; epilogue: processing for a return from an ISR. ["pro-" to put forth; "epi-" outer or after]	
tail chaining	On some architectures, switching from one ISR to another ISR can be achieved without fully restoring the context from the interrupted task.	
CPU load	The fraction of the processor's clock cycles that are required to maintain proper operation of the program under worst case conditions.	
buffer (circular/double/FIFO)	A region of memory (usually an array) used to provide temporary storage between a producer (of data) and a consumer (of data).	
producer/consumer model	The concept of passing data (usually asynchronously) between a producing process and a consuming process.	
atomicity and atomic	An action of the computer is atomic if it cannot be split, which usually means it cannot be interrupted; atomicity refers to that property.	
critical section	A section of computer code which needs to be made atomic (e.g., by disabling and re-enabling interrupts).	
(finite) state machine (FSM)	A process which transitions through a deterministic sequence of states which are finite in number.	
asynchronous/synchronous	The timing of a synchronous process is completely determined by a clock; all other processes are asynchronous.	
quadrature en/decoding	The encoding of a sequence with two bits such that only one bit changes at a time; the four states thus created allow position and direction to be decoded.	
debouncing	Ensuring that simple physical switches achieve a single state change per operation, e.g., a single push→release corresponds to a single ON→OFF.	

Term(s)	Definition	
zero-order hold circuit	An electronic circuit which takes the analogue voltage of an input at a particular time and holds it steady at the output.	
successive approximation converter	A binary search is performed to find the closest decimal value which corresponds to the input analogue voltage; the decimal value is converted into a voltage in order to compare it to the input.	
dual-slope converter	The input analogue voltage is used to control a counter circuit, such that the count value is proportional to the input voltage.	
aliasing	When an analogue signal is sampled at too low a rate, f_{s1} say, frequencies in the original signal greater than $f_{s1}/2$ will 'alias' as lower frequencies in the digital recording, thus distorting the information recorded.	
digital filtering	The process of converting one set of digital samples into another with different properties, e.g., only retaining the lower frequencies.	
input capture	The mode of use for a timer in which the time between input pin changes is measured by saving (capturing) the counter values each time the change occurs.	
output compare	The mode of use for a timer in which the counter counts down (or up, or up & down) generating a periodic waveform (PWM). The counter value is compared with a value in a register to determine when switching occurs.	
RTOS	A real-time operating system (RTOS) is designed to help software achieve a reliable, maintainable and precise embedded system; at its most basic it may simply consist of a kernel.	
kernel	The kernel is the core of the program, which may consist of a simple ever-lasting loop. At times when no foreground or background tasks are being executed, the kernel code is being executed.	*
datapath	The principal route for shifting data within the processor, usually comprising the data bus and its connections.	
instruction set architecture (ISA)	The format for the instructions for a processor family comprising the instruction format, the number of operands and the set of operations supported.	
opcode (operation code)	The field of bits within each instruction which defines the operation.	
operand	A quantity which is involved in executing an instruction, e.g. the destination and source registers or an offset address. Different ISAs are designed to fit from 0 to 3 operands within the instruction.	
instruction decoding	Using the opcode and other bits within the instruction to generate a set of control signals.	
status bits (condition codes)	A set of bits C, N, V, Z, which indicate information about the result of the last instruction involving the ALU. E.g., the Z bit is set if the operation result was zero. The bits are stored in the processor status register.	
status register (often processor status register - PSR)	Register containing status information essential to the processor operation, including the status bits C, N, V and Z.	
enable	A control input for a register or memory which enables a change to be made to that element.	
assembler	The name given to the language which directly maps to machine instructions; also the name of the program which converts the language statements into actual machine code.	
mnemonic	The abbreviated term indicating the instruction type in assembly language, e.g., LDR R1, [R11, #offset]. - 'LDR' is the mnemonic for 'load register'.	

Term(s)	Definition	
aliasing	The process whereby samples of a higher frequency sinewave are indistinguishable from those from a low frequency sinewave.	
sampling theorem	The principle stating that the sampling rate should be at least twice the highest frequency present in a sequence, thereby preventing aliasing.	
sampling aperture	The finite time required to practically sample an analogue signal; it is ideally as short as possible.	
zero-order hold	An electronic circuit within an analogue-digital converter (ADC) which holds the analogue sample value constant while the quantiser completes the conversion.	
quantisation step	The increase in voltage associated with unit change in the digitial output from an ADC.	
quantisation error	The difference between the actual analogue signal value and the quantized equivalent.	
sampling jitter	Variation in sample values caused by inaccuracies in sample timing.	
signal-to-noise ratio (SNR)	A measure of how "clean" a signal is; measured in deciBels (dB).	
root-mean-square (RMS)	A measure which allows the size of varying voltages to be compared.	
tristate buffer	An electronic circuit which can be controlled to transmit a logic level 0 or 1 as well as making the output 'high impedance' (switching the output off).	
read-modify-write	The sequence which allows a microcontroller to alter an individual bit (e.g., in a control register for a peripheral). It may require 3 machine instructions to complete on some microcontrollers.	
bit banding	The method employed in the Cortex-M3 architecture to make bit changes atomic: a set of addresses in memory space are reserved to allow a specific bit to be addressed.	
machine epsilon	The smallest possible increment in the mantissa (of a floating point format) that can be distinguished by the computer.	
odd/even parity	A method used to detect errors in transmission for a serial link: one or more parity bits are included such that the number of 1 bits over the data and parity bits combined is odd/even respectively.	

* The definitions of these terms differ; the definitions here apply to ENCE361.