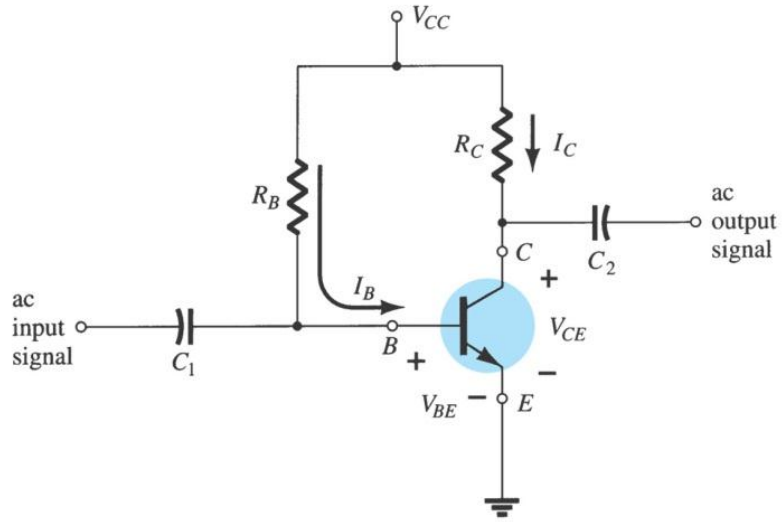
Introduction to Bipolar Junction Transistors
BJTs
& DC Biasing Circuits

(Chapter 3&4 , Boylestad & Nashelsky)

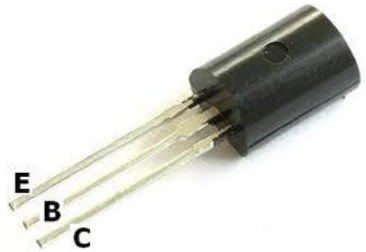
- Transistors types
- Principles of Operation
- Main configurations
- Current Voltage Characteristics
- Limits of operation
- Biasing and stability circuits
- Analysis of DC transistor circuits
- Transistor switching



BJT Common Emitter fixed bias configuration

Semiconductor Transistor Types

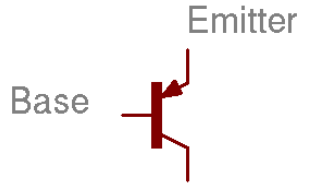
Chapter 3



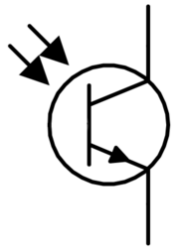
Bipolar Junction Transistors (BJT)

- npn transistor
- pnp transistor

NPN



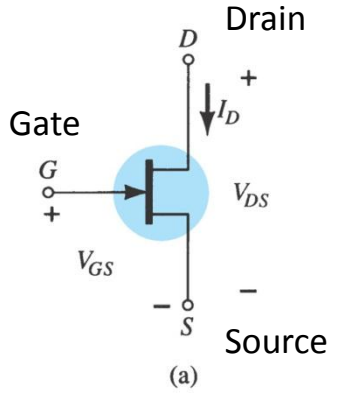
PNP



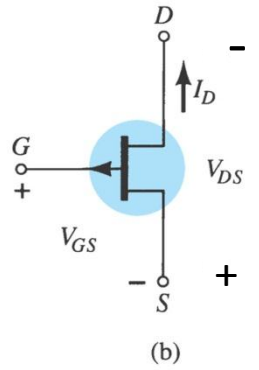
Phototransistor

Field Effect Transistors (FET)

- Junction FET
- Metal Oxide Semiconductor (MOS) Transistors
- Complementary MOS (CMOS)

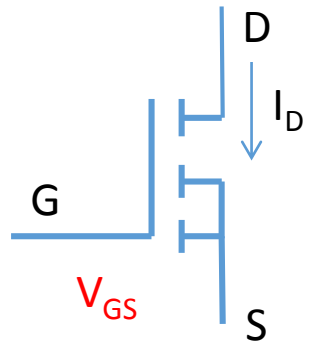


N Channel



P Channel

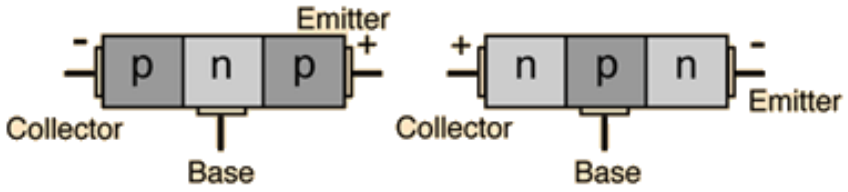
JFET

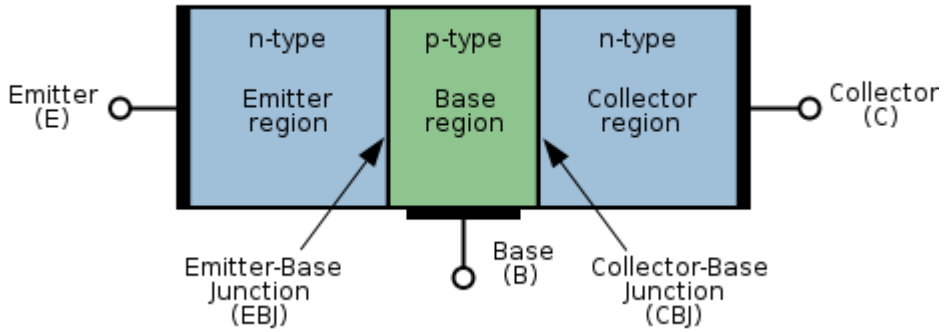


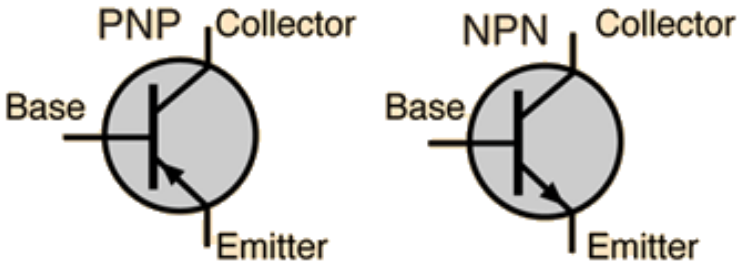
MOSFET

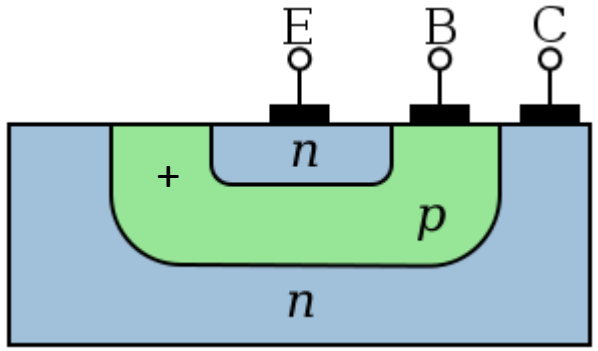
Bipolar Junction Transistor (BJT)

Conduction is *by electrons*(negative charged) *and holes*(positive charge)



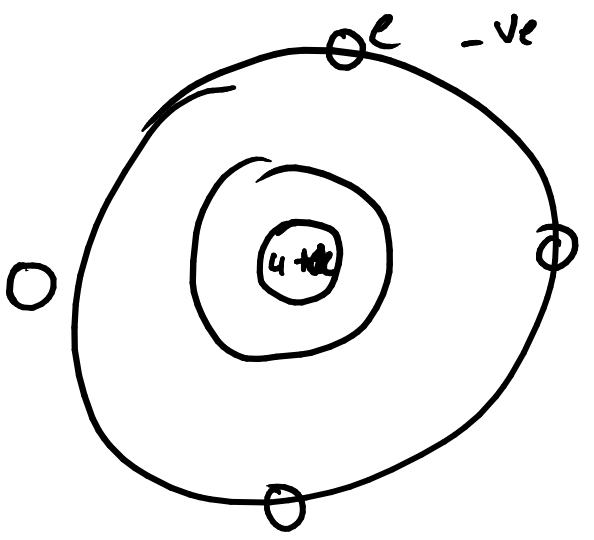






Cross section in a typical npn transistor, each region is different

Emitter heavily doped, Base lightly doped, Collector large area

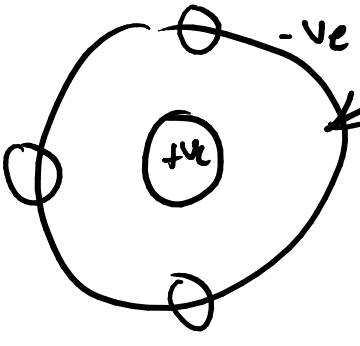


electrons

4 +ve
4 -ve

4 +ve
3 -ve

+ ve ion



add ⊖

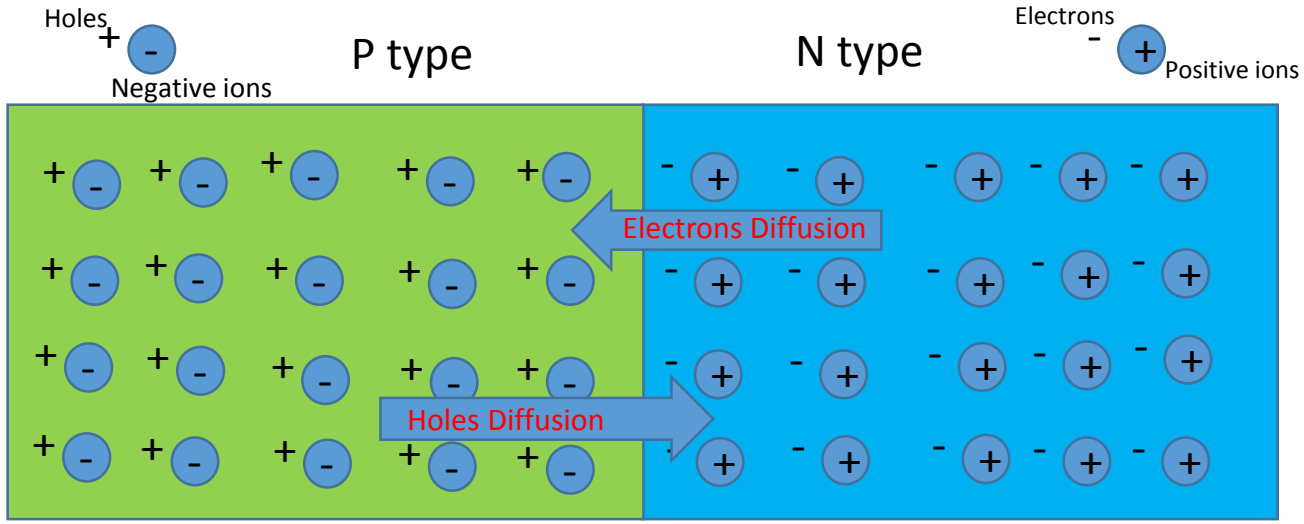
more - ve charge

⊕ -ve

-ve ions

P type, Majority are Holes

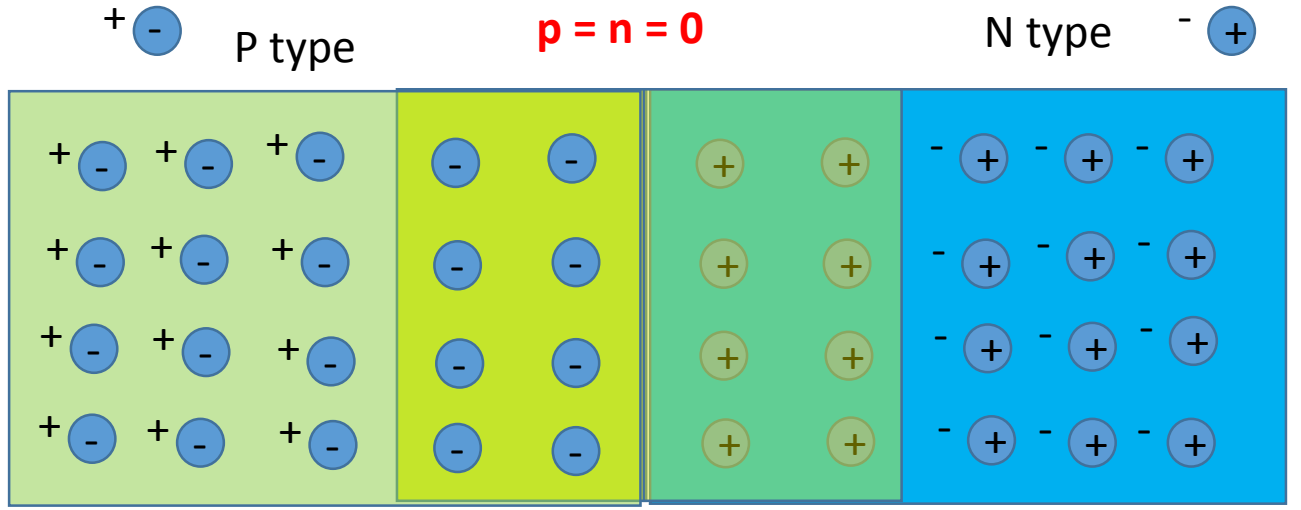
Minority are Electrons



Diffusion from High to Low concentration

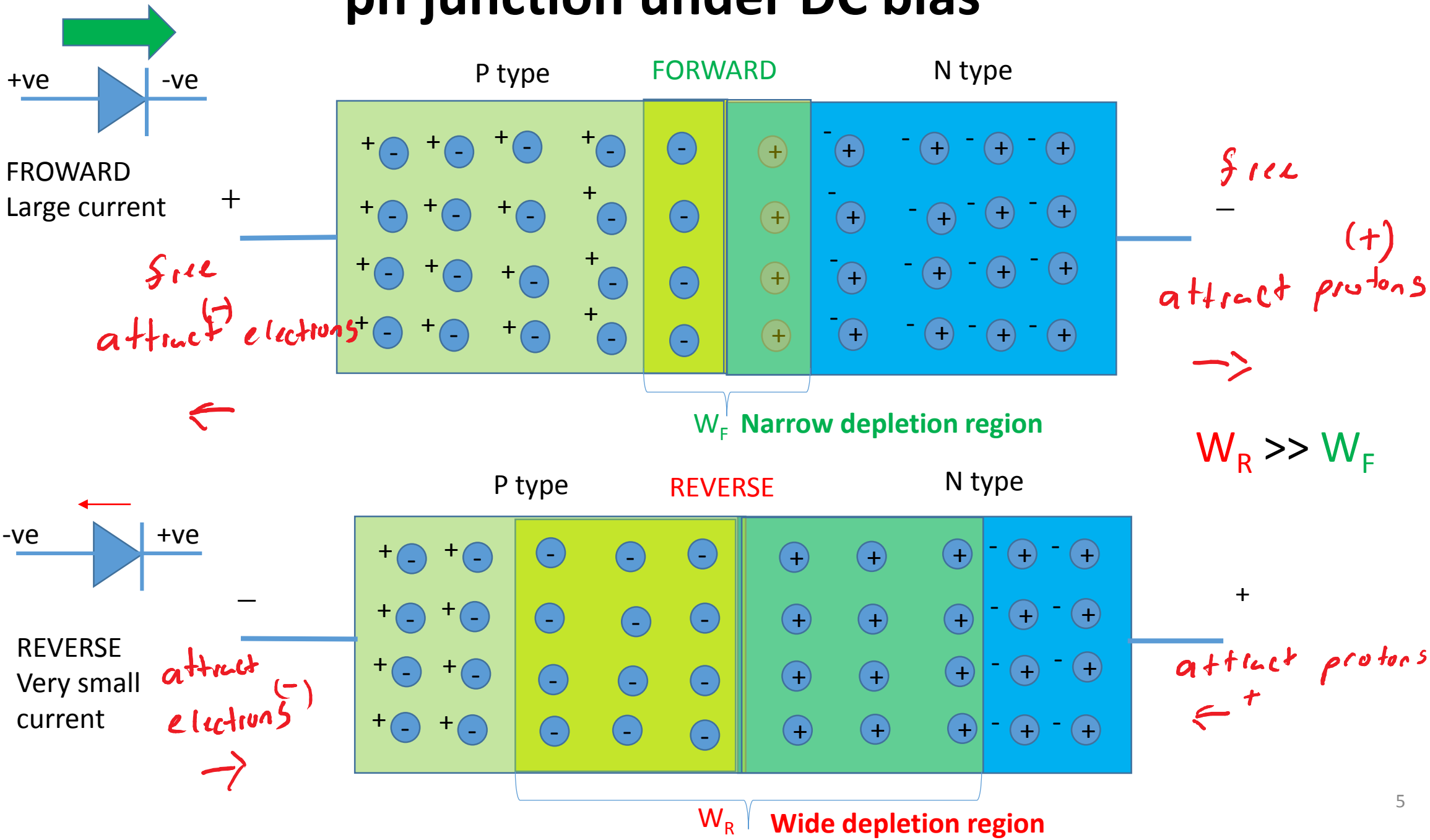
N type, Majority are Electrons

Minority are Holes

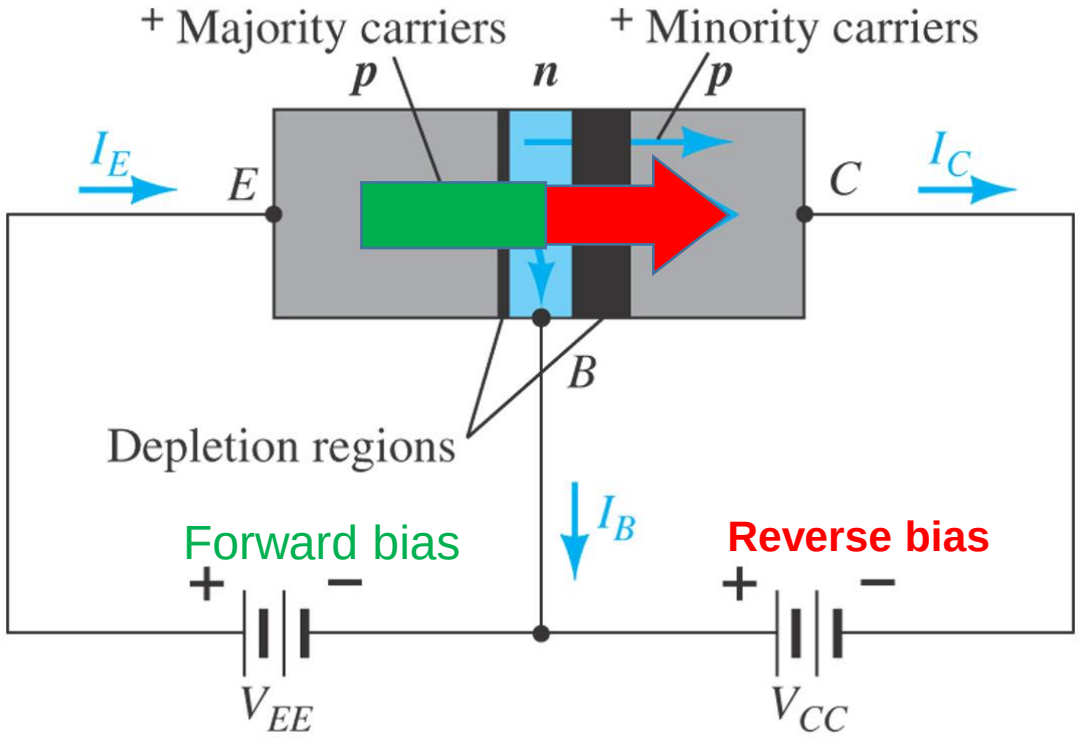


Depletion region, positive ions on N type side, negative ions on p type side. High electric field, built in potential, no free carriers, high resistance region

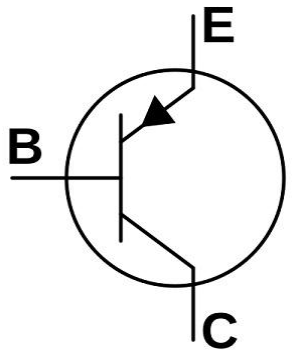
pn junction under DC bias



Majority and Minority carriers flow of a pnp transistor.



- E, Emitter
- B, Base
- C, Collector



$I_E = I_C + I_B$

Emitter current = Collector current + Base current

- Holes(positive charge) in an p-type are the **Majority carriers** and electrons are the minority carriers.
- In an n-type, electrons(negative charge) are the **Majority carries** and holes are the minority carriers.

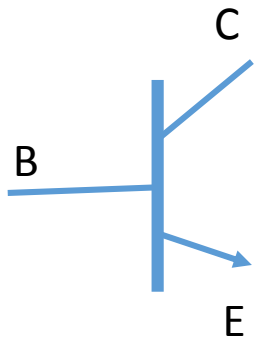
Transistor operations

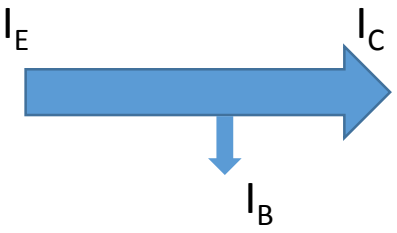
Two junctions;

- Emitter-Base(EB) junction is forward biased (Majority carries flow)
- Collector-Base (CB) junction is reverse biased (Minority carriers flow)
- BJTs are Current controlled devices(Base current I_B controls Collector current I_C)

- Emitter emits majority carriers(holes in p type) to the forward –biased EB junction, resulting in an emitter current I_E .
- The collector-base junction is reversed biased and only minority carriers flow(holes in n type).
- Emitted carriers (majority in p type) become minority in the base region (n type)are collected at the collector terminal I_C .
- The base current I_B is the results of minority carriers , hence it is the smallest.
- Current flow direction is opposite to the electrons flow, i.e. current direction is same as holes(+ve charge) flow direction.
- Now applying Kirchhoff's Current Law, KCL : $I_E=I_C+I_B$

"The sum of all currents flowing into a node equals the sum of currents flowing out of the node".



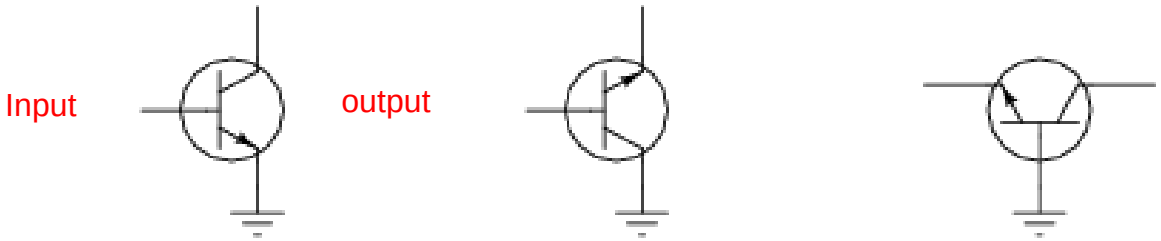


Transistor Configurations

Three possible configurations:

- Common Emitter
- Common Collector
- Common Base

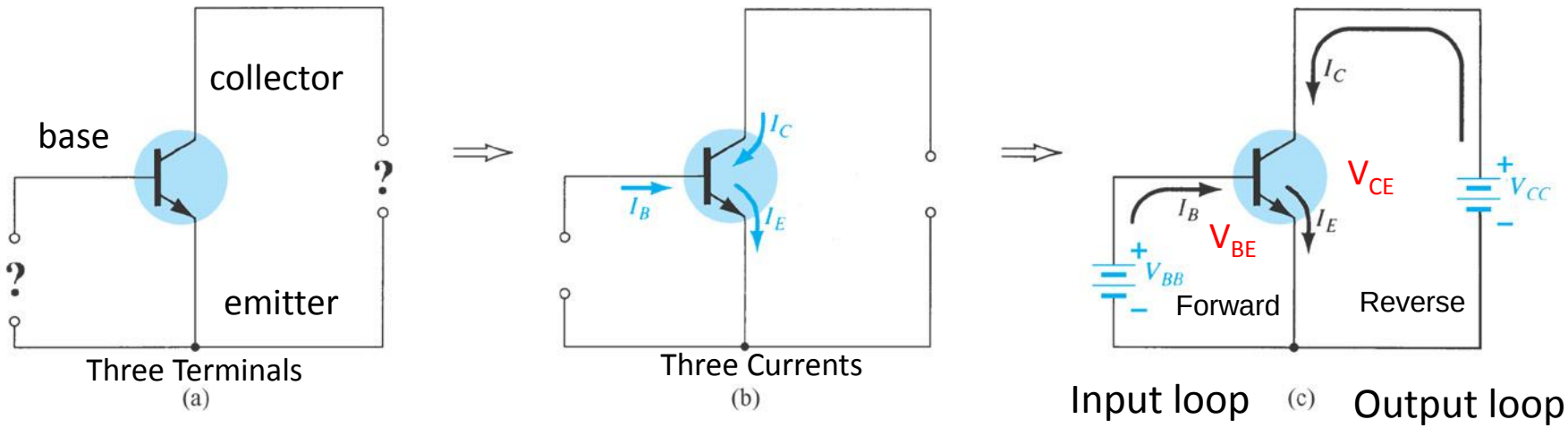
Depending which terminal is common between both input and output or at ground potential.



Common Emitter, **Common Collector**, Common Base

Common Emitter Configuration

Apply a bias

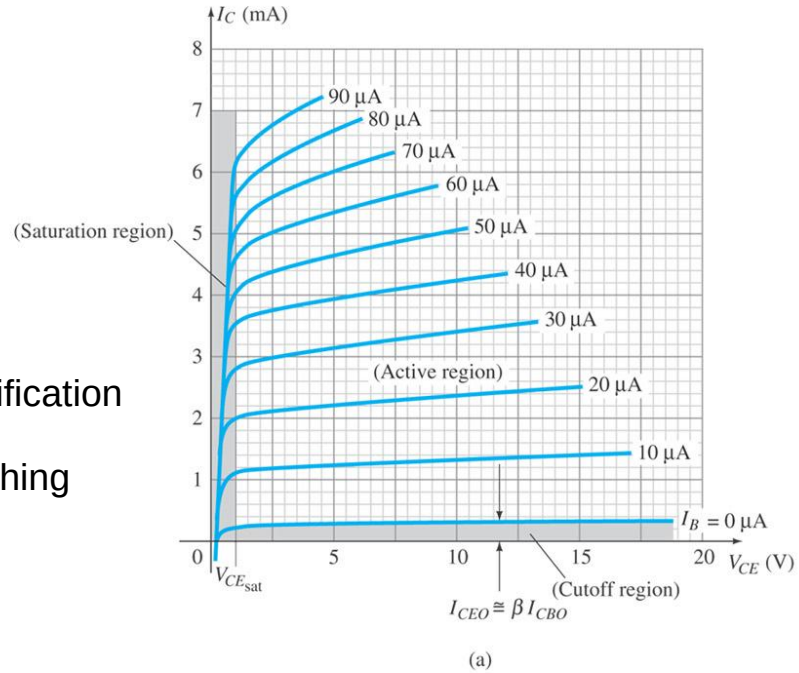


Three regions:

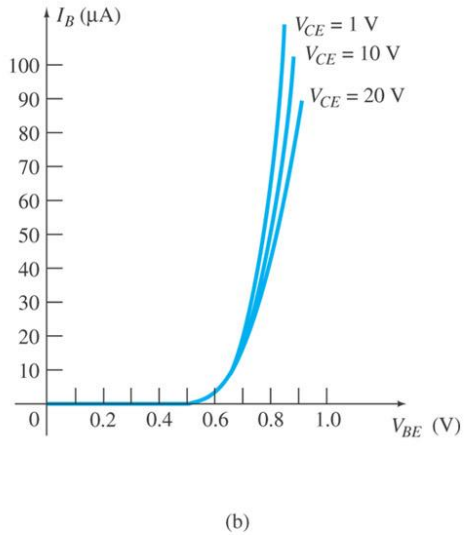
- Active(linear) region
- Saturation region
- Cutoff region

Linear region → Amplification

Saturation and cut-off → Switching



Output characteristics



Input characteristics

Limits of Operations

The maximum power dissipation in a transistor is given by:

$P_{cmax} = V_{CE} \times I_C$

e.g if V_{CE} is 10V and I_C = 30mA, then P_{cmax} = 300mW.

- Ensure that the maximum ratings are not being exceeded.
- Output signal should be with minimum distortion.
- Refer to current – voltage characteristics and data sheet before designing the circuits.

Example from data sheet

I_{Cmax} = 50mA

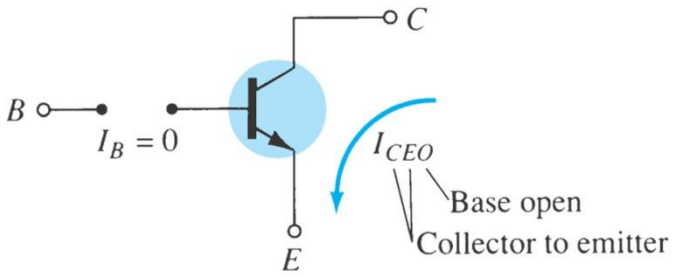
V_{CEO} = 20V

P_{cmax} =300mW

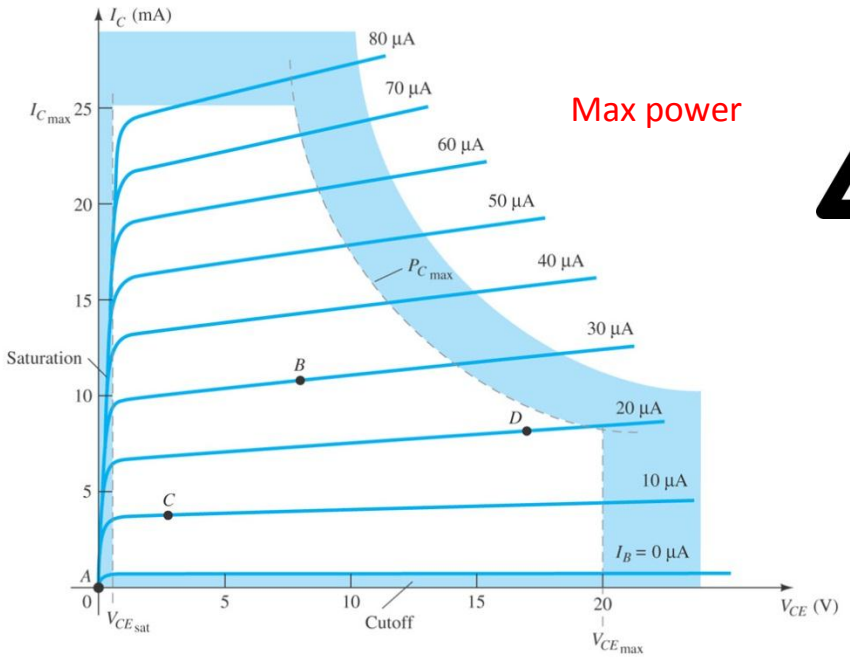
V_{CEsat} = 0.3V

I_{CEO} = 10µA(base open)

$I_{CEO} = \beta I_{CBO}$(emitter open) mainly leakage current for common emitter configuration



Maximum current



Max power

Max voltage

$I_{CEO} \leq I_C \leq I_{cmax}$

$V_{CEsat} \leq V_{CE} \leq V_{CEmax}$

$I_C \times V_{CE} \leq P_{cmax}$

Transistor Biasing

Chapter 4

- Biasing is applying DC supply to power the circuit.
- The desired operating point is established by the DC bias network.
- Biasing network will also determine the stability of the circuit against variations in temperature or changes in the value of β

β = common emitter forward current amplification factor

$\beta_{dc} = \frac{I_C}{I_B}$ $\frac{mA}{\mu A}$ (typical value between 100 to 300)

$\beta_{ac} = \frac{\Delta I_c}{\Delta I_b}$ (output current / input current)

$I_E = I_C + I_B = \beta I_B + I_B = I_B(1+\beta)$

The value of β is given by the transistor data sheet
Or can be calculated from the IV curves.

Load line and operating point

The network equation is defined by the DC biasing circuit. To draw the load line that represent the network equation on the output characteristics of the BJT transistor, the collector emitter loop equation is:

$V_{CC} = I_C R_C + V_{CE}$ (Kirchhoff's Voltage Law , KVL*)

Now assume $I_C = 0$ mA , then $V_{CE} = V_{CC}$ this represent the first point on the curve

For $V_{EC} = 0$, $I_C = V_{CC}/R_C$ this represent the second point on the curve

By joining the two points, the load line is constructed, and the intersection with (I_C-V_{CE}) transistor characterises showing all possible operating points.

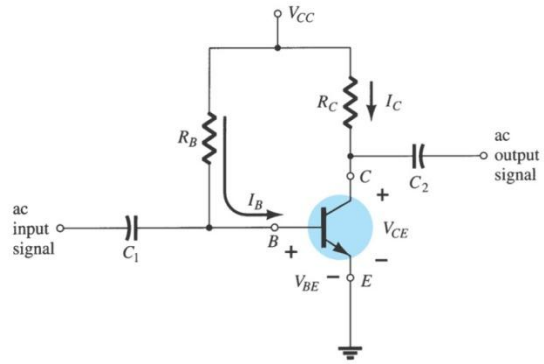
The operating point Q can be fixed by the values of R_C and R_B :

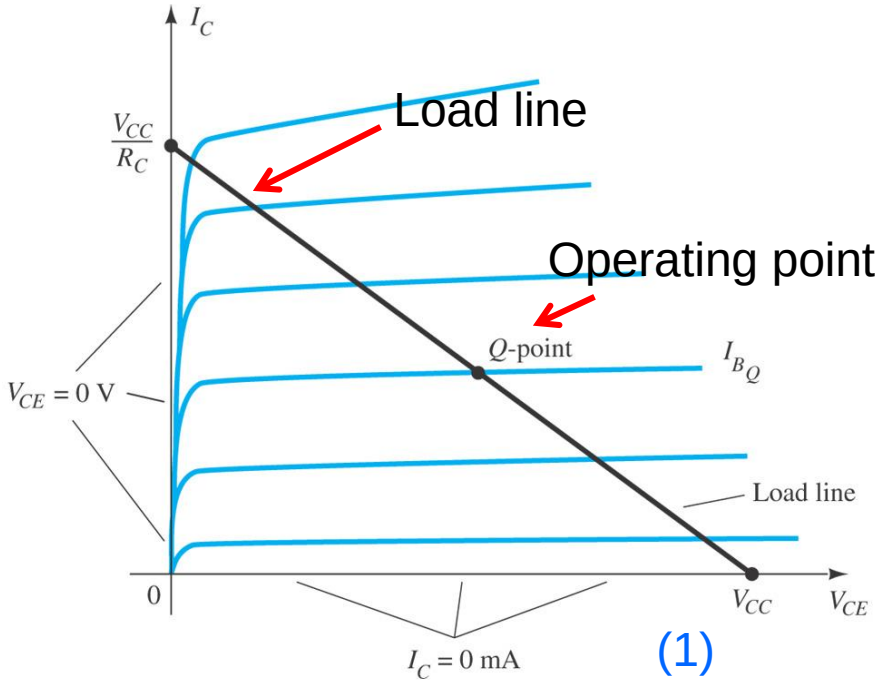
$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_{BQ}}$$

I_{CQ} and V_{CEQ} are the collector current and collector-emitter voltage at the operating point Q,

I_{BQ} is the base current at the operating point Q



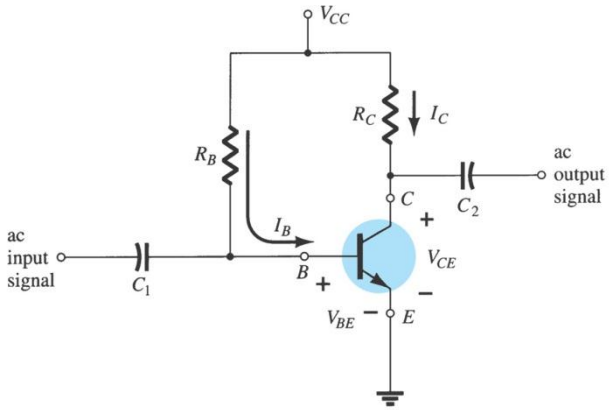


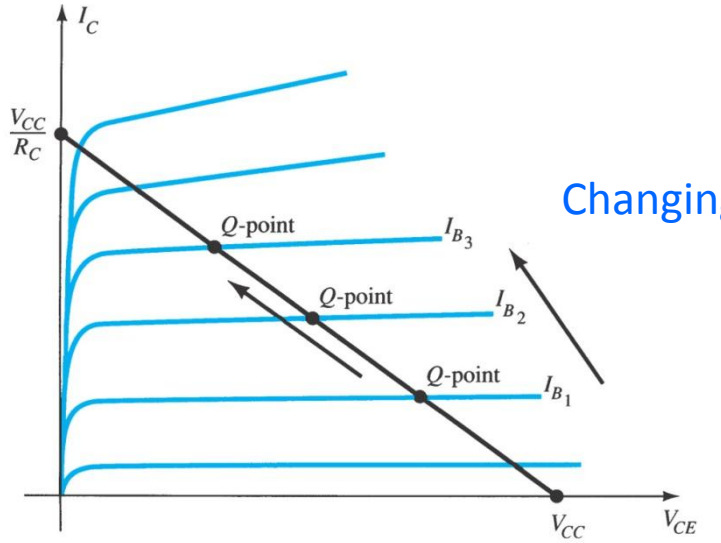
Output characteristics

**KVL law is based on the conservation of energy whereby voltage is defined as the energy per unit charge. The total amount of energy gained per unit charge must be equal to the amount of energy lost per unit charge, as energy and charge are both conserved.*

Load line adjustment

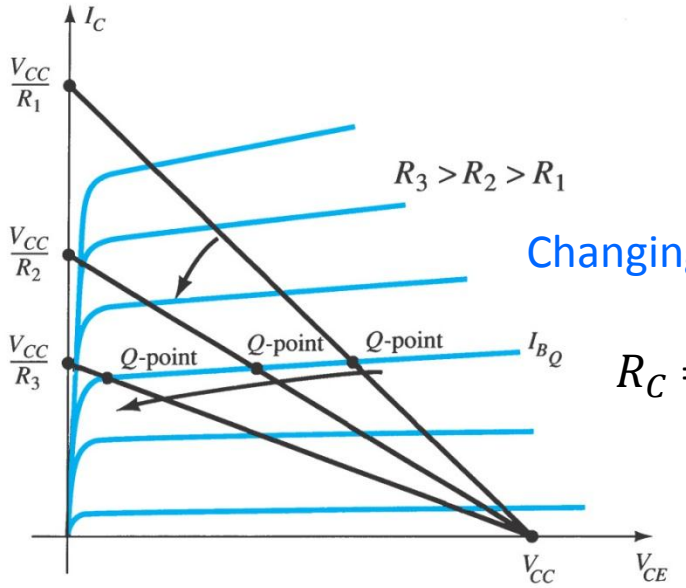
The operating point Q can be adjusted by changing R_C, R_B or V_{CC}





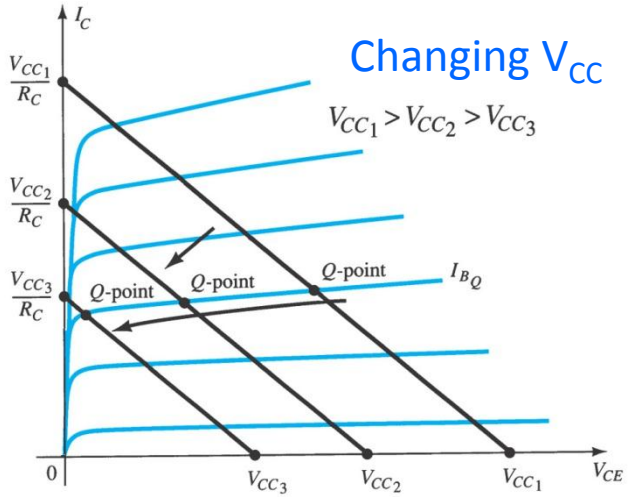
Changing I_B through R_B

$$R_B = \frac{V_{CC} - V_{BE}}{I_{BQ}}$$



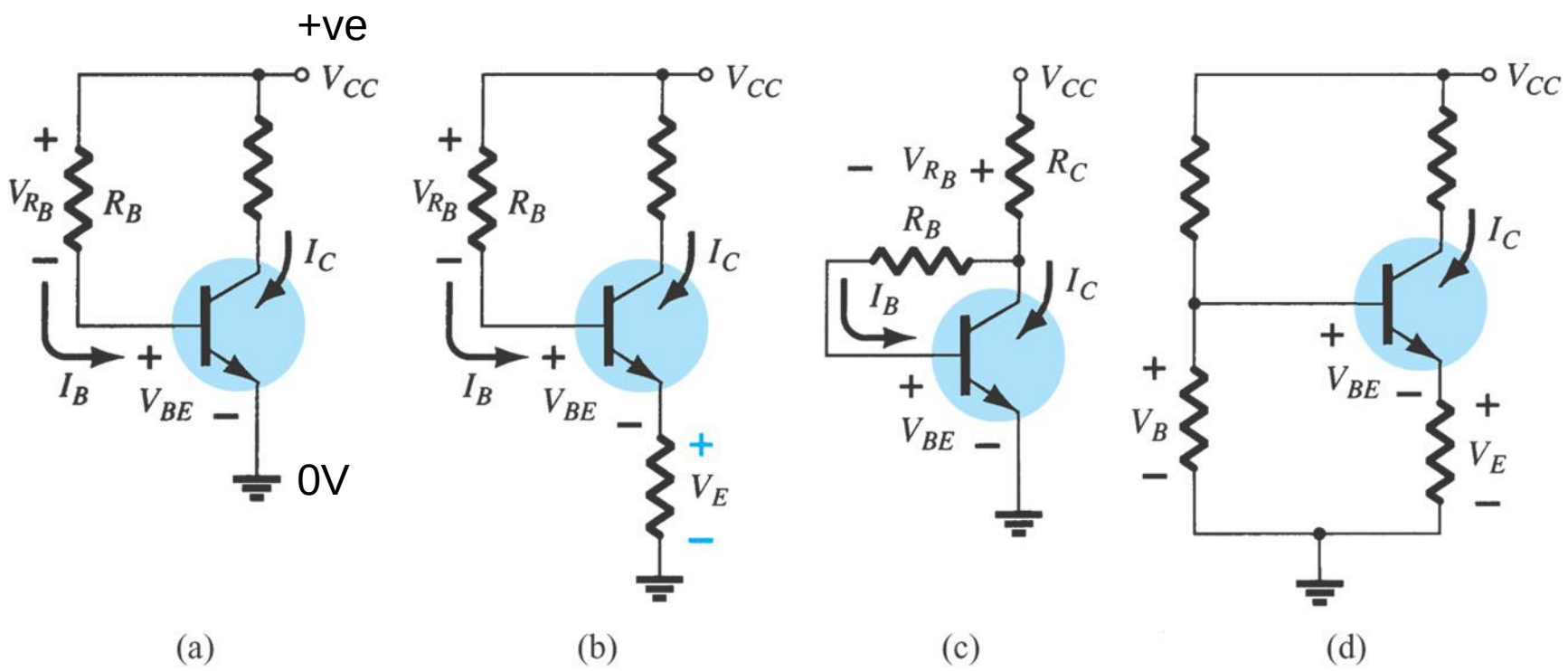
Changing R_C

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}}$$



Changing V_{CC}

DC biasing circuits



Fixed bias

Emitter bias

Feedback bias

Voltage divider bias

Fixed Bias Configuration

Base –Emitter loop (KVL)

$V_{CC} - I_B R_B - V_{BE} = 0$

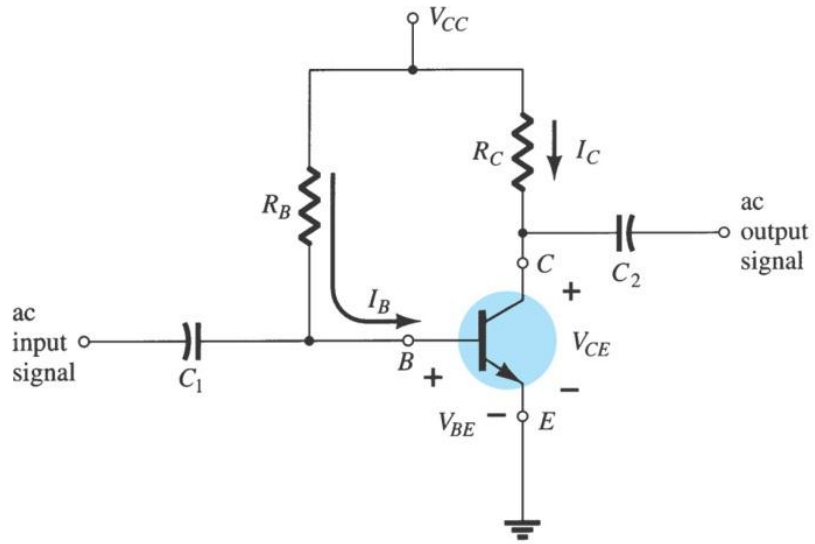
$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ R_B sets the level of base current for the operating point

Collector- Emitter loop (KVL)

$V_{CC} - I_C R_C - V_{CE} = 0$

$I_C = \frac{V_{CC} - V_{CE}}{R_C}$ R_C value determine the level of I_C

$V_{CE} = V_{CC} - I_C R_C$



Improved Bias stability

To improve the stability of the transistor circuit against variations in the value of β and temperature, a resistor is inserted between the emitter terminal and ground called R_E.

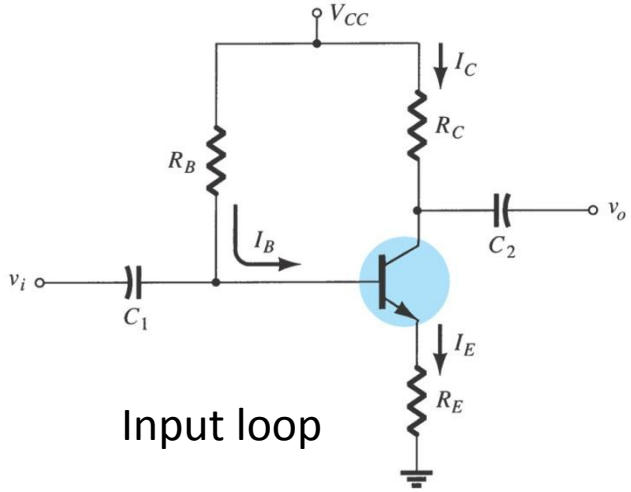
Base-Emitter Loop:

V_{CC}-$I_B R_B$-V_{BE}-$I_E R_E$ =0

Substitute for $I_E = (\beta + 1) I_B$

V_{CC}-$I_B R_B$-V_{BE}- $(\beta + 1) I_B R_E$ =0

Then solve for $I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$



Input loop

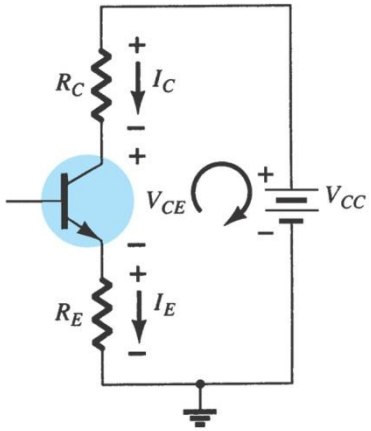
Collector-Emitter Loop:

V_{CC}-$I_C R_C$-V_{CE}-$I_E R_E$ =0

But $I_E \approx I_C$

V_{CC}-$I_C R_C$-V_{CE}-$I_C R_E$ =0

Solve for $I_C = \frac{V_{CC} - V_{CE}}{(R_C + R_E)}$



Output loop

Voltages across the transistor device

$V_E = I_E R_E \approx I_C R_E$

$V_{CE} = V_C - V_E$

$V_C = V_{CE} + V_E$

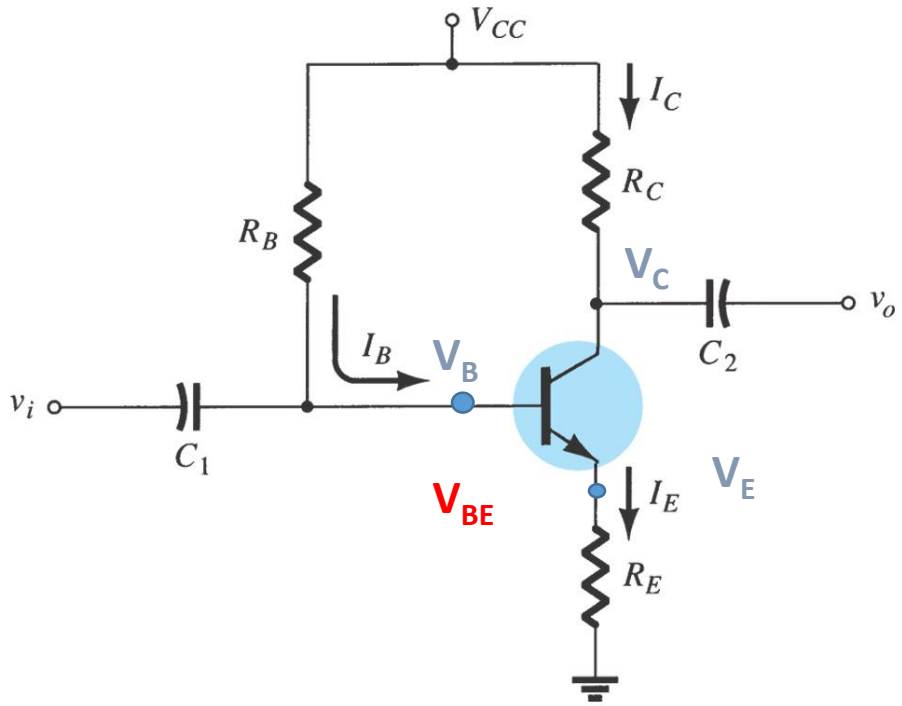
OR

$V_C = V_{CC} - I_C R_C$

$V_{BE} = V_B - V_E$

$V_B = V_{BE} + V_E$

$V_B = V_{CC} - I_B R_B$

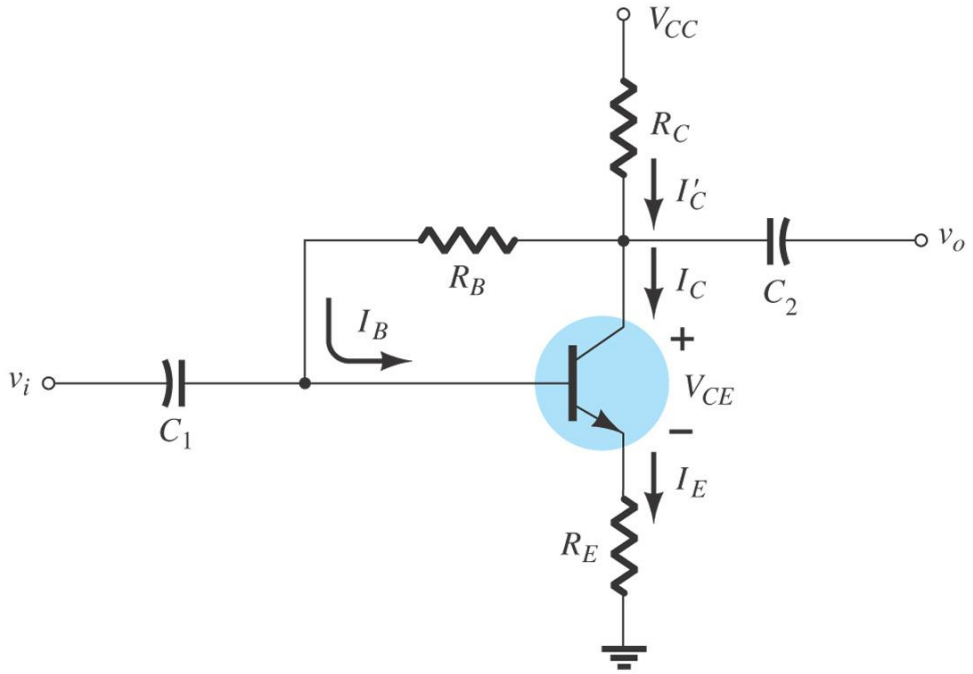


V_{BE} = 0.7V for Silicon Transistor, given by data sheets. For different semiconductors, V_{BE} is different and highly dependent on the Energy gap of the material

Feedback Bias

Base –Emitter Loop:

$V_{CC} - I_{C'} R_C - I_B R_B - V_{BE} - I_E R_E = 0$
$I_C = \beta I_B$
$I_{C'} = I_C + I_B = I_E$
But $I_C >> I_B$
$I_{C'} \approx I_C \approx I_E = \beta I_B$



Then:
$V_{CC} = \beta I_B R_C + I_B R_B + V_{BE} + \beta I_B R_E = 0$

Solve for $I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$

The feedback path results in a reflection of the resistance R_C back to the input loop
Now if $\beta (RC + RE) >> R_B$

$I_B \approx \frac{V_{CC} - V_{BE}}{\beta(R_C + R_E)}$

$I_C = I_B\beta = \frac{V_{CC} - V_{BE}}{(R_C + R_E)}$ i.e I_C is independent on β when $\beta(R_C+R_E) >> R_B$

Feedback Circuit output loop

Collector-Emitter loop:

$V_{CC} - I_{C'} R_C - V_{CE} - I_E R_E = 0$

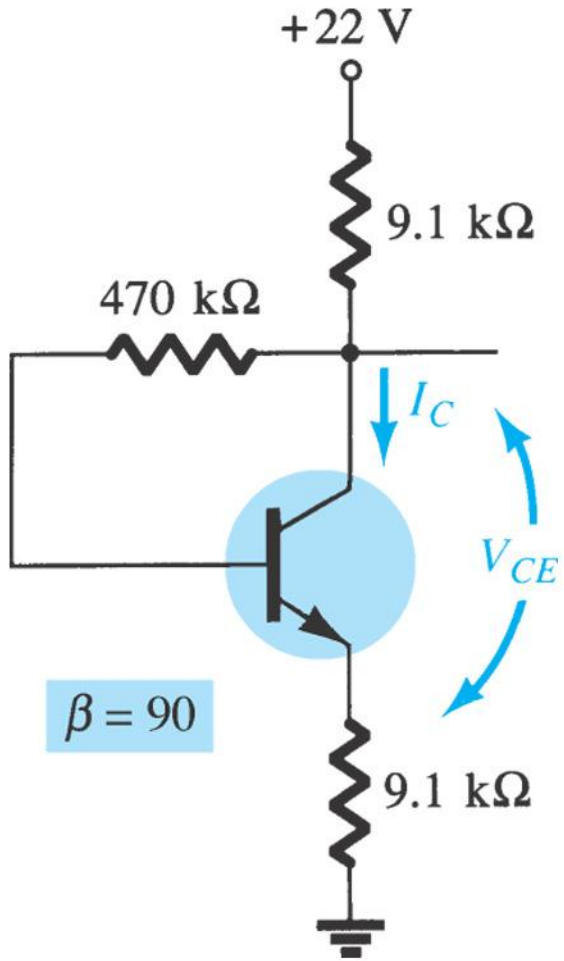
Since $I_{C'} = I_E \approx I_C$, $I_C >> I_B$

$V_{CC} = I_C R_C + V_{CE} + I_C R_E$

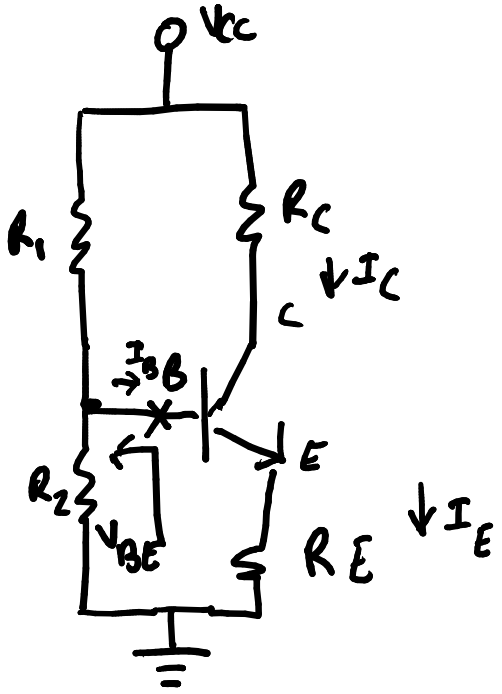
$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

And

$V_{CE} = V_{CC} - I_C (R_C + R_E)$

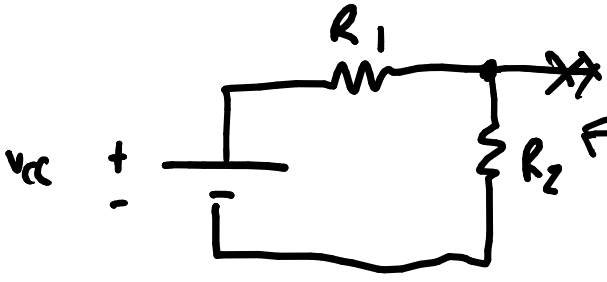


DC biasing



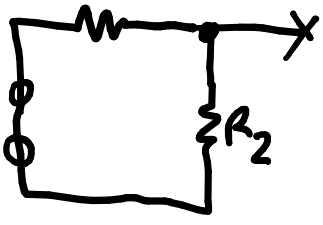
I_B, I_C, I_E, V_{CE}

Thevenin



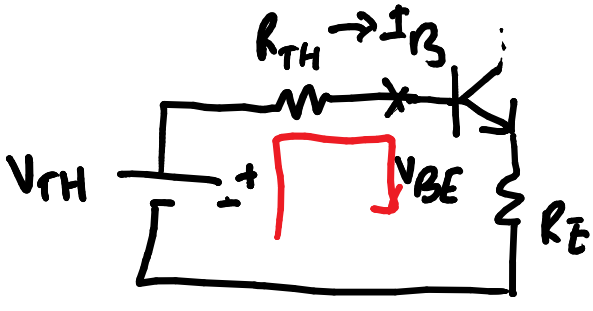
$$V_{TH} = V_{CC}\left(\frac{R_2}{R_1 + R_2}\right)$$

Short R_1



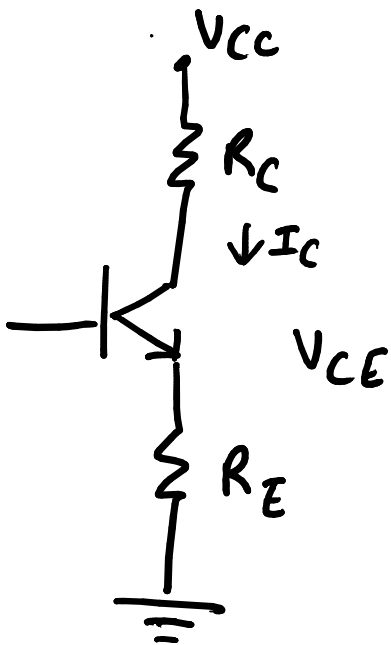
$$R_{TH} = R_1 \parallel R_2$$

$$\therefore I_E = I_B(\beta + 1)$$



$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

Solve for I_B = $\dfrac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E}$



$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$I_C \simeq I_E$$

$$I_C = \frac{V_{CC} - V_{CE}}{(R_C + R_E)}$$

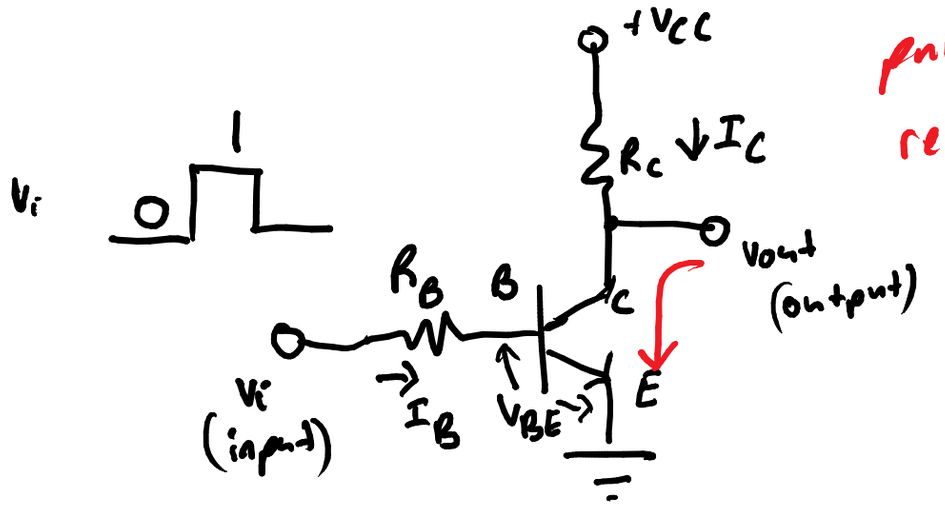
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$V_{CE} = V_C - V_E$$

$$V_E = I_E R_E$$

$$V_{BE} = V_B - V_E$$

Transistor switching

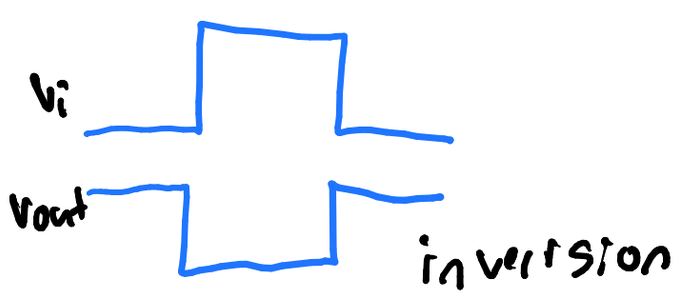


for $V_i = 0$, $I_B = 0$, $I_C = 0$

$V_{out} = V_{CC}$ = High level

for V_i = High (logic) level, I_B with flow $+I_C$ flow

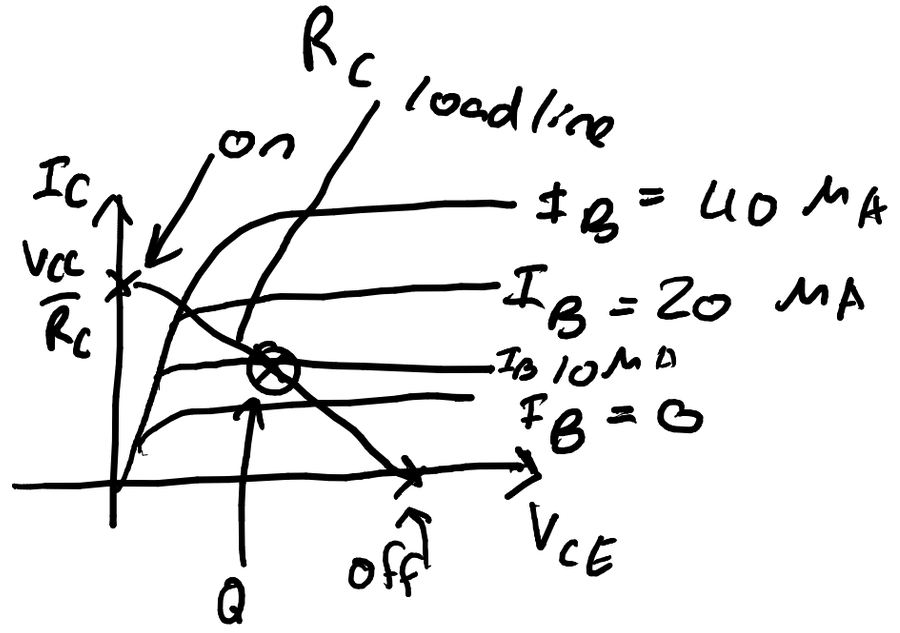
$V_O = 0$ V, low level



$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

(1) $$I_B = \frac{V_i - V_{BE}}{R_B}$$

(2) $$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$ load line?



$I_C = \frac{V_{CC}}{R_C}$ Switch either "on" or "off"

(2) $V_{CE} = V_{CC} - I_C R_C$

for $V_{CE} = 0$

$I_C = \frac{R_C}{V_{CC}}$

for $I_C = 0$

$V_{CE} = V_{CC}$

To ensure transistor is on

(1) $I_C = V_{CC}/R_C = I_{C\,sat}$ - ?

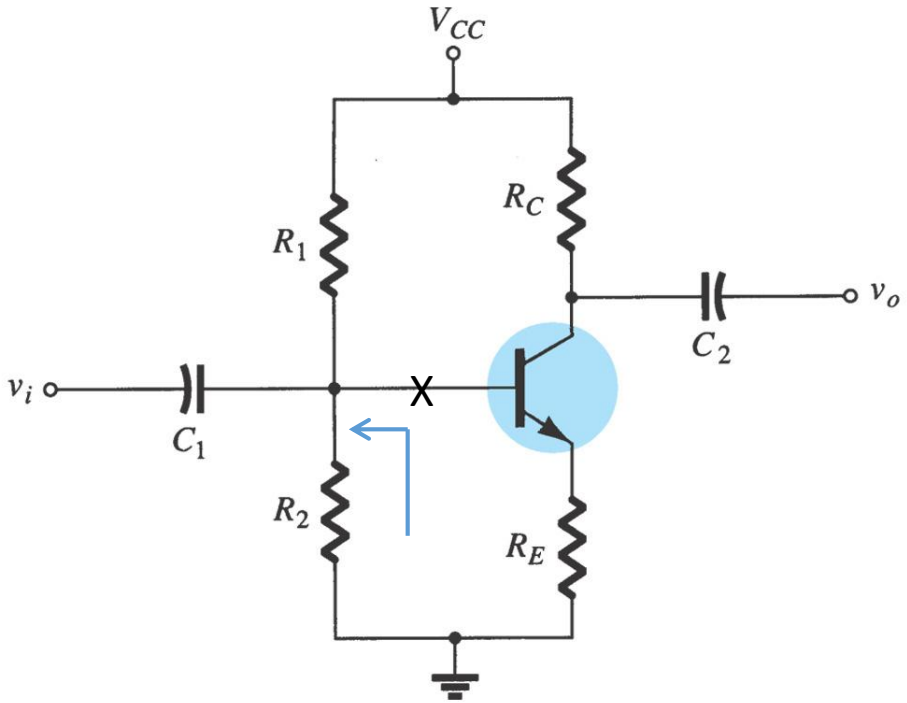
(2) $I_C = \beta I_B$

(3) $I_B = \frac{V_i - V_{BE}}{R_B}$ calculate I_B (3)

$V_{BE} = 0.7$ V

Voltage Divider Bias

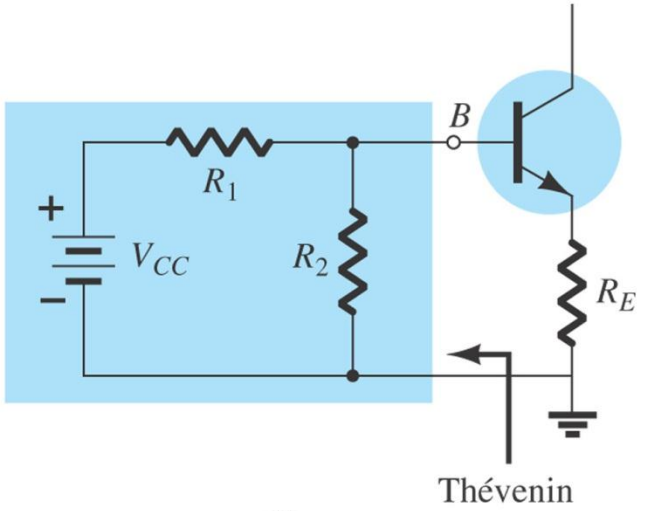
A bias circuit that is less sensitive to variations in the value of β by essentially reducing the effective value of R_B

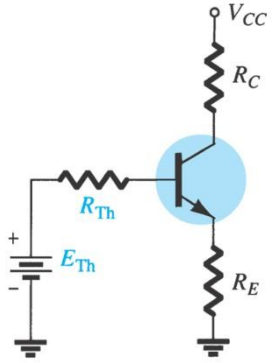


$$R_B = R_1//R_2$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Using Thevenin's equivalent circuit for the left hand side of the circuit shown:

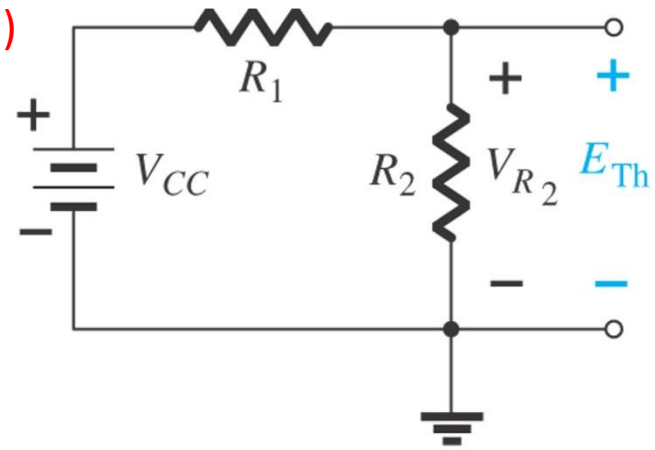




Equivalent circuit

Applying Thevenin's Equivalent Circuit

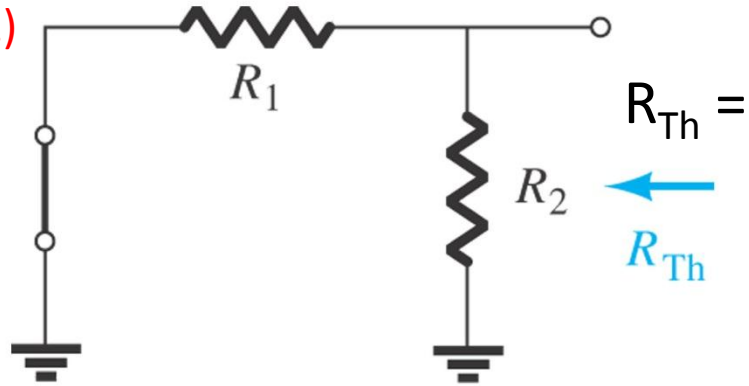
(1)



$$E_{Th} = V_{CC} \frac{R_2}{R_2+R_1} \quad \text{.....(1)}$$

Using Voltage Divider rule to find $V_{R2} = E_{TH}$

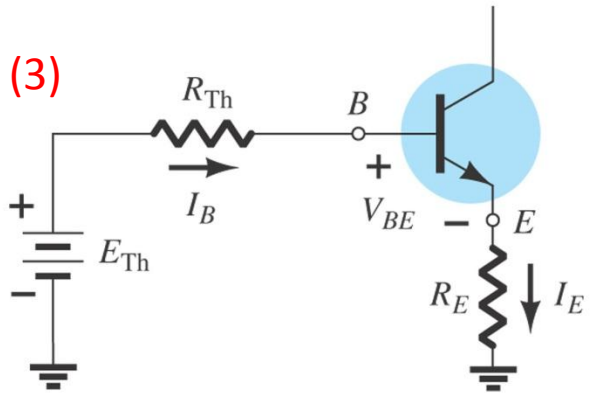
(2)



$$R_{Th} = \frac{R_1 R_2}{R_1+R_2} \quad \text{.....(2)}$$

Find the equivalent resistance R_{Th} of the circuit with $V_{CC} = 0$

(3)



Redraw the circuit with E_{Th} and R_{Th} and calculate I_B

$$I_B = \frac{E_{Th}-VBE}{R_{TH}+(1+\beta)R_E} \quad \text{.....(3)}$$

Applying Kirchhoff's voltage law;

$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$

$I_E = (1+\beta)\, I_B$

$E_{Th} - I_B R_{Th} - V_{BE} - (1+\beta) I_B R_E = 0$

Then solve for I_B equation(3)

Output Loop

Collector-Emitter loop:

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

Since $I_C \approx I_E$, $I_C >> I_B$

$V_{CC} = I_C R_C + V_{CE} + I_C R_E$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

Voltages across the transistor:

$V_{CE} = V_{CC} - I_C (R_C + R_E)$

$V_{CE} = V_C - V_E$

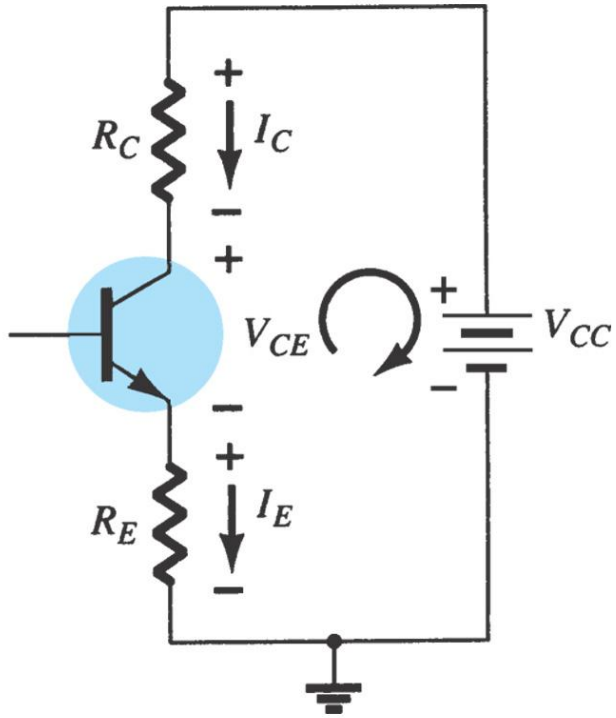
$V_E = I_E R_E$

$V_{BE} = V_B - V_E$

$V_B = V_{BE} + V_E$

$V_C = V_{CC} - I_C R_C$

V_{BE} = 0.7V for Si transistors



Transistor Switching

To ensure the transistor is switched ON

$I_C = \beta I_B \geq I_{Csat}$

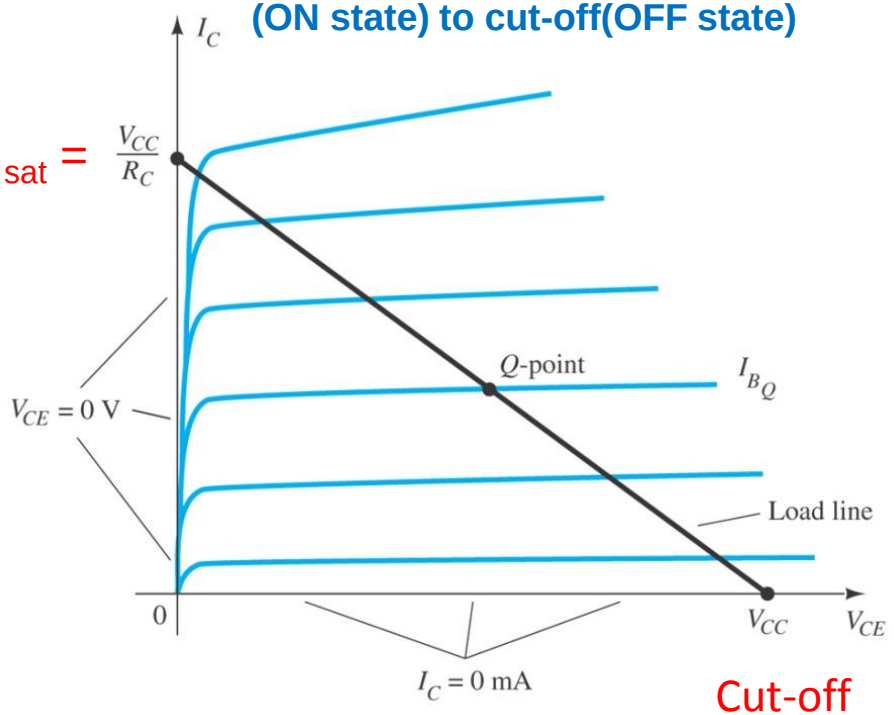
$I_{C\,sat} = V_{CC} / R_C$ highest collector current

$V_{CE} = V_{CC} - I_C R_C$ from the output loop

$I_B = (V_i - V_{BE})/R_B$ from circuit input loop

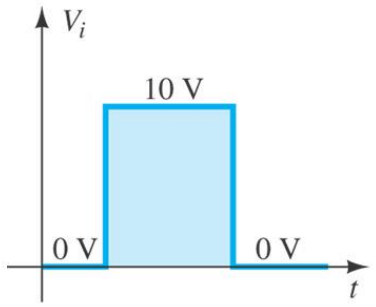
Transistor switching from saturation (ON state) to cut-off(OFF state)

$I_{C\,sat} =$

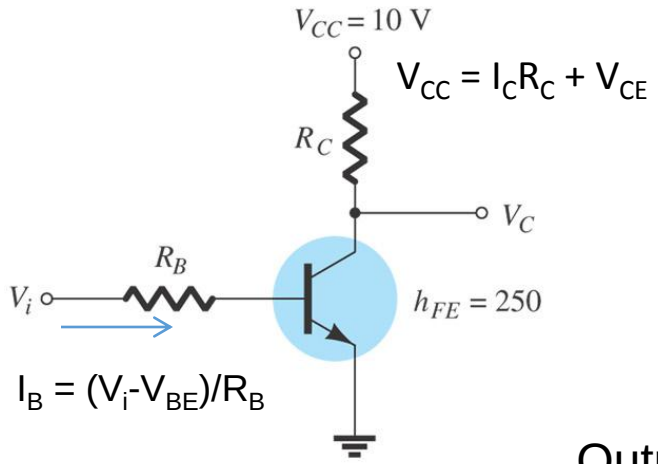


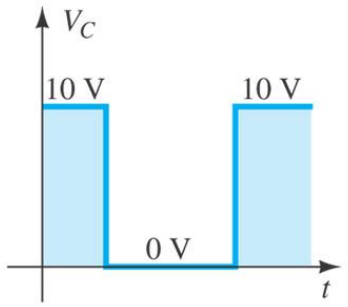
Cut-off

I_C = 0mA



Input voltage





Output voltage

Transistor Switching

Consider applying a square waveforms at the base terminal of the BJT circuit shown:

(1) At V_i = 0V (low voltage level)

$I_B = \frac{V_i - V_{BE}}{R_B}$ = 0 as there is no current flowing for input voltage = 0V.

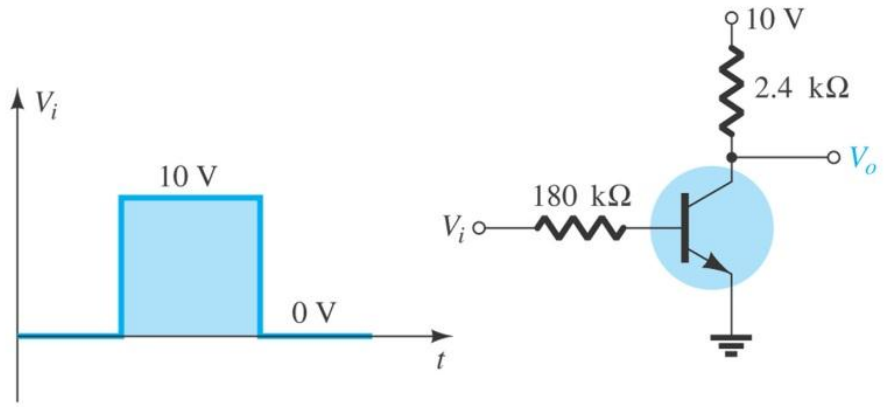
As V_{BE} = 0V, I_B = 0, I_C =0, **Transistor is OFF**
$V_{CE} = V_{out} = V_{CC}$ = 10V (no current is flowing in the collector therefore output voltage is high)

(2) At V_i = 10V (high voltage level) , V_{BE} will be 0.7V

$I_B = \frac{V_i - V_{BE}}{R_B}$ will be flowing and I_B value is determined by R_B

Then I_C will be flowing and has high value, the **Transistor is switched ON**, output voltage is small as the output is exposed to ground

$V_{CE} = V_{out}$ ~ 0V , low voltage state,
(practically V_{CEsat} = 0.15 – 0.2V)

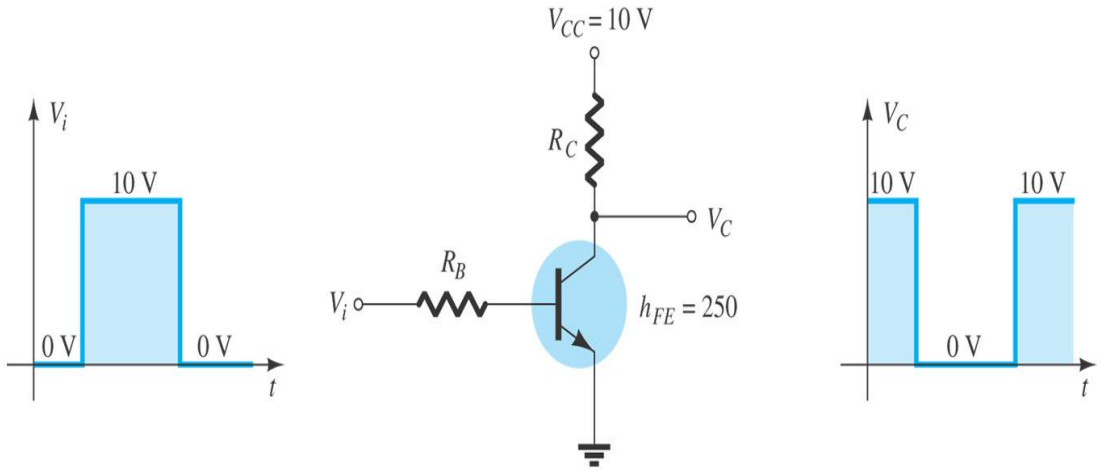


To ensure transistor is ON in Saturation

Calculate $I_B = \frac{V_i - V_{BE}}{R_B}$ ……(1)

Then calculate $I_B = \frac{I_{C\,sat}}{\beta}$ ……(2)

$I_{Csat} = \frac{V_{CC}}{R_C}$ ……(3)



To ensure that the transistor will be working in saturation region (ON state)

The base current I_B calculated from equation 1 must be larger than I_B calculated from equation 2. This is usally determined by the value of the resistance used in the base terminal R_B.

Example

If R_C = 0.82kΩ and R_B = 63kΩ

Is the transistor in saturation or cut off mode for the input voltage shown:

$I_{csat} = V_{CC}/R_C$ as V_{CE} is very small in saturation region $V_{CC} = I_{csat} R_C + V_{CEsat}$

For saturation condition to establish, the level of I_B must be made:

$I_{Bmin} \geq \frac{I_{Csat}}{\beta_{dc}}$ to ensure saturation

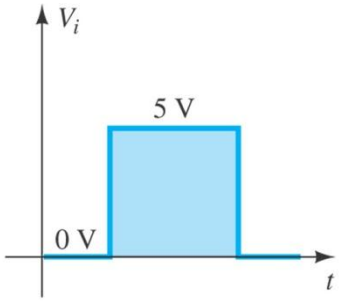
Now for V_i = 5V, $I_B = \frac{V_i - V_{BE}}{R_B} = \frac{5 - 0.7}{63k}$ = 68 μA from the circuit

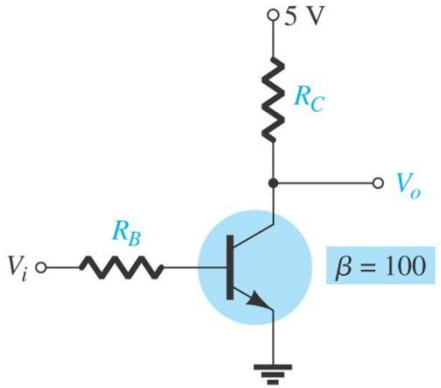
$I_{csat} = \frac{V_{CC}}{R_C} = \frac{5V}{0.82k} = 6.1mA$

I_B = 68 μA $> \frac{I_{Csat}}{\beta_{dc}} = \frac{6.1mA}{100}$ = 61 μA

Using transistor with higher β will ensure saturation

68 μA > 61 μA then the transistor is in saturation





$R_{sat} = \frac{V_{CEsat}}{I_{Csat}} = \frac{0.15V}{6.1mA}$ = 24.6 Ω (transistor has low resistance when ON)

Now if Vi = 0V, Transistor is OFF, I_B=I_C=0mA

$R_{cutoff} = \frac{V_{CC}}{I_{CEO}} = \frac{5V}{10\mu A}$ = 500kΩ very high resistance in cut-off region.

I_{CEO} is the minority carriers current flowing in the reverse bias collector emitter junction.