Schematic: Seeed SoM - STM32MP157C

SHEET	SHEET NAME
01	Title/Revision History
02	MPU_1
03	MPU_2
04	DDR3
05	eMMC
06	PMU
07	PINOUT/LED

Revision History

DATE	REVISION	DESCRIPTION
2019/05/21	Seeed SoM - STM32MP157C_v1.0_SCH_190521	Initial Release
2019/09/04	Seeed SoM - STM32MP157C_v1.01_SCH_190904	
2019/12/13	Seeed SoM - STM32MP157C_v1.01_SCH_191213	Change R5,R6 from 1k to 2k

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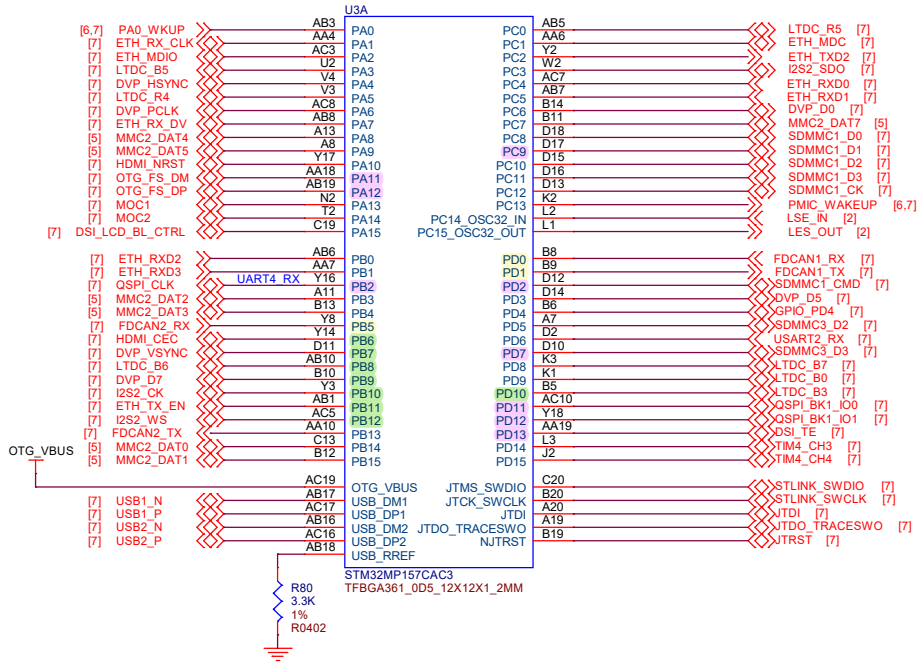
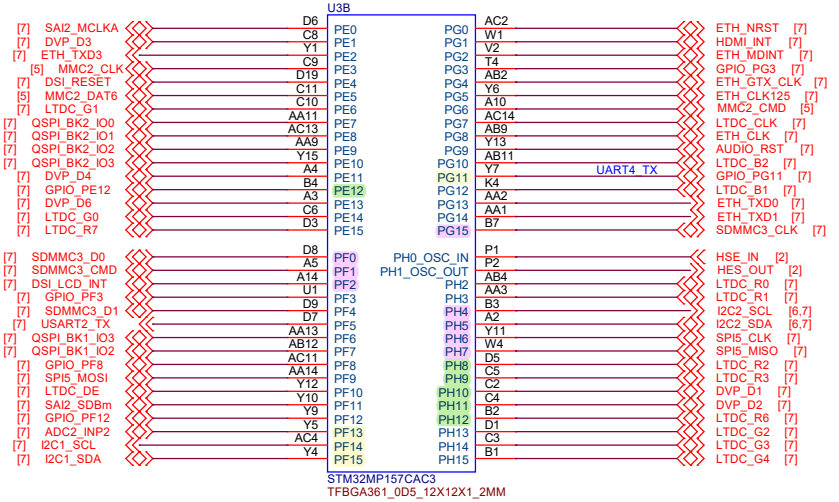
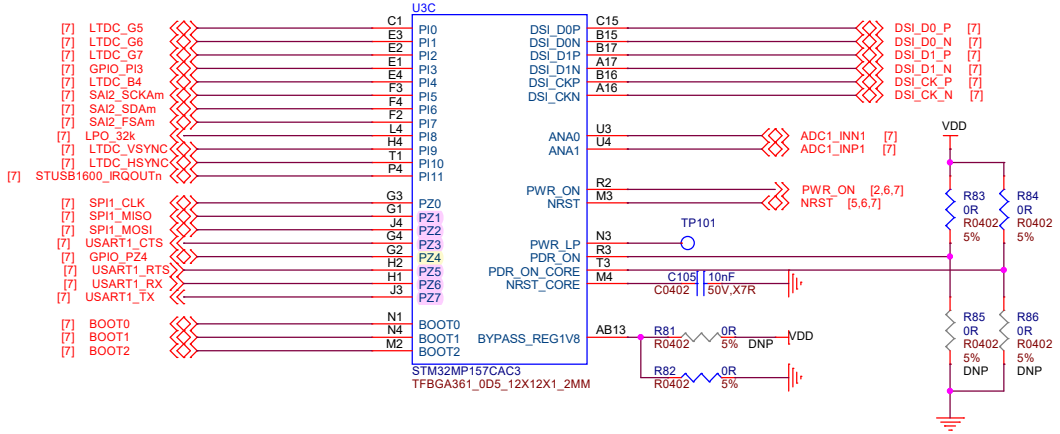
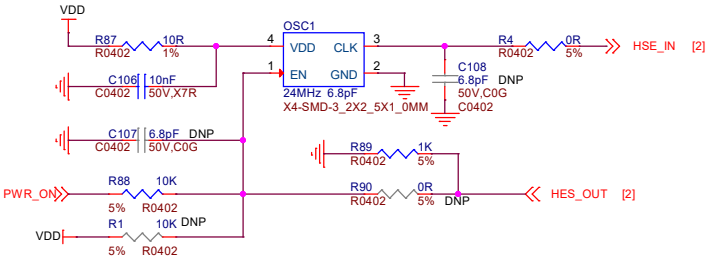
Title: Seeed SoM - STM32MP157C

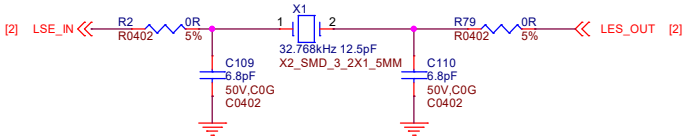
Size: A3	Document Number: 01 Title / Revision History	Rev: v1.01
Draw By: weifeng	Date: Friday, December 13, 2019	Sheet: 1 of 7











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	Title: Seeed SoM - STM32MP157C		
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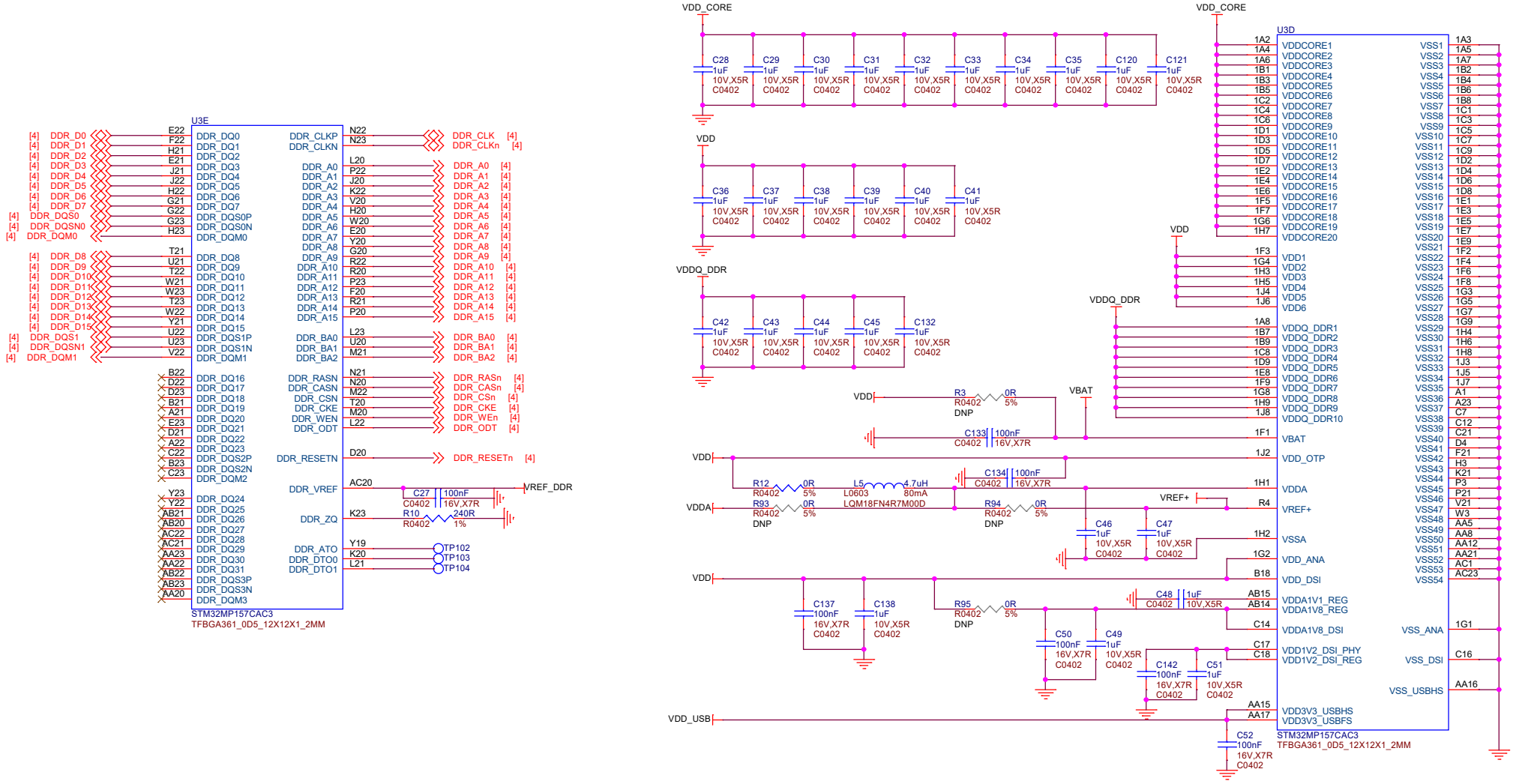
U3E
STM32MP157CAC3
TFBGA361_0D5_12X12X1_2MM
U3D
STM32MP157CAC3
TFBGA361_0D5_12X12X1_2MM
VDD_CORE
VDD
VDDQ_DDR
VBAT
VDD_USB
VREF_DDR
VREF+
DDR_CLK
DDR_CLKn
DDR_RESETn
DDR_VREF
DDR_ZQ
DDR_ATO
DDR_DTO0
DDR_DTO1
DDR_RASn
DDR_CASn
DDR_CSn
DDR_CKE
DDR_WEn
DDR_ODT
DDR_BA0
DDR_BA1
DDR_BA2
DDR_DQS0P
DDR_DQS0N
DDR_DQM0
DDR_DQS1P
DDR_DQS1N
DDR_DQM1
DDR_DQS2P
DDR_DQS2N
DDR_DQM2
DDR_DQS3P
DDR_DQS3N
DDR_DQM3
VDD_OTP
VDDA
VSSA
VDD_ANA
VDD_DSI
VDDA1V1_REG
VDDA1V8_REG
VDDA1V8_DSI
VDD1V2_DSI_PHY
VDD1V2_DSI_REG
VDD3V3_USBHS
VDD3V3_USBFS
VSS_ANA
VSS_DSI
VSS_USBHS
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Size: A3
Document Number: 03 MPU_2
Rev: v1.01
Draw By: weifeng
Date: Thursday, September 12, 2019
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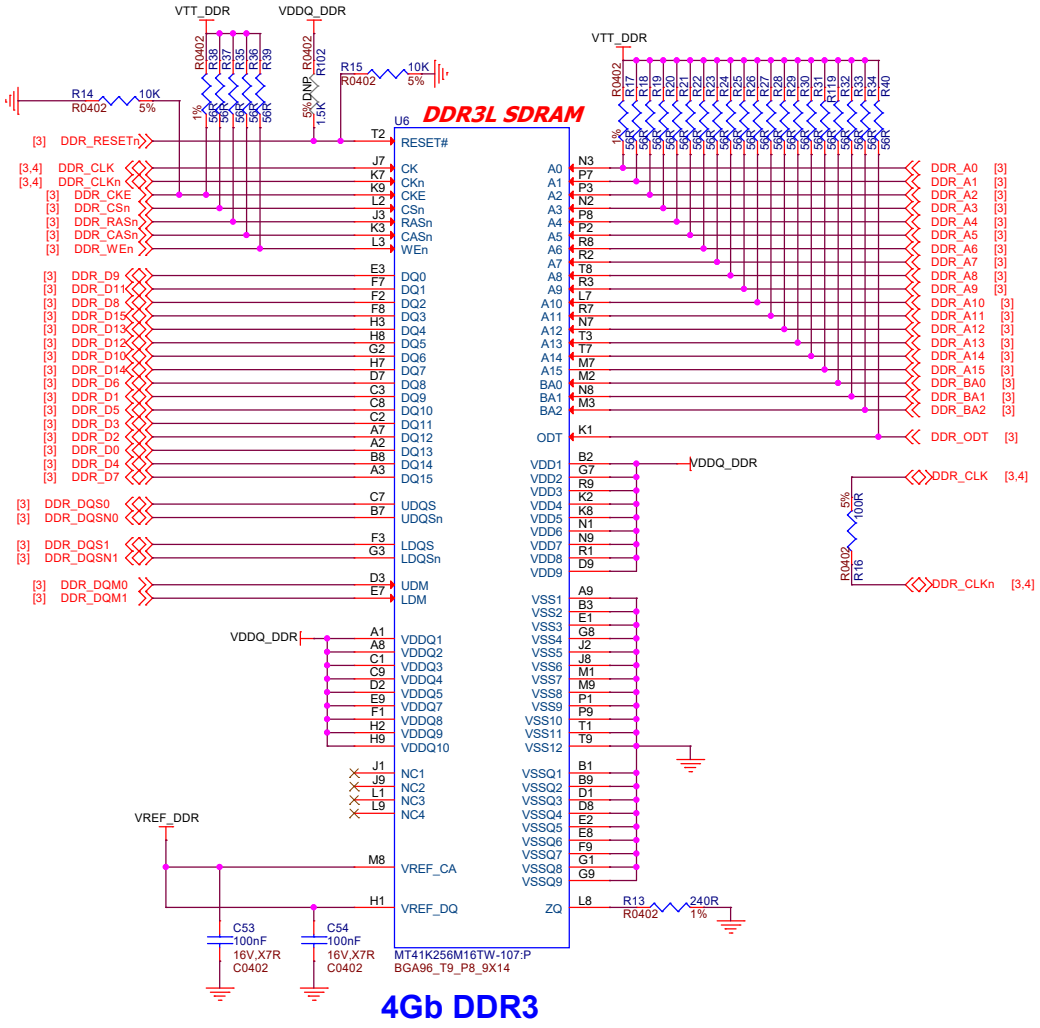

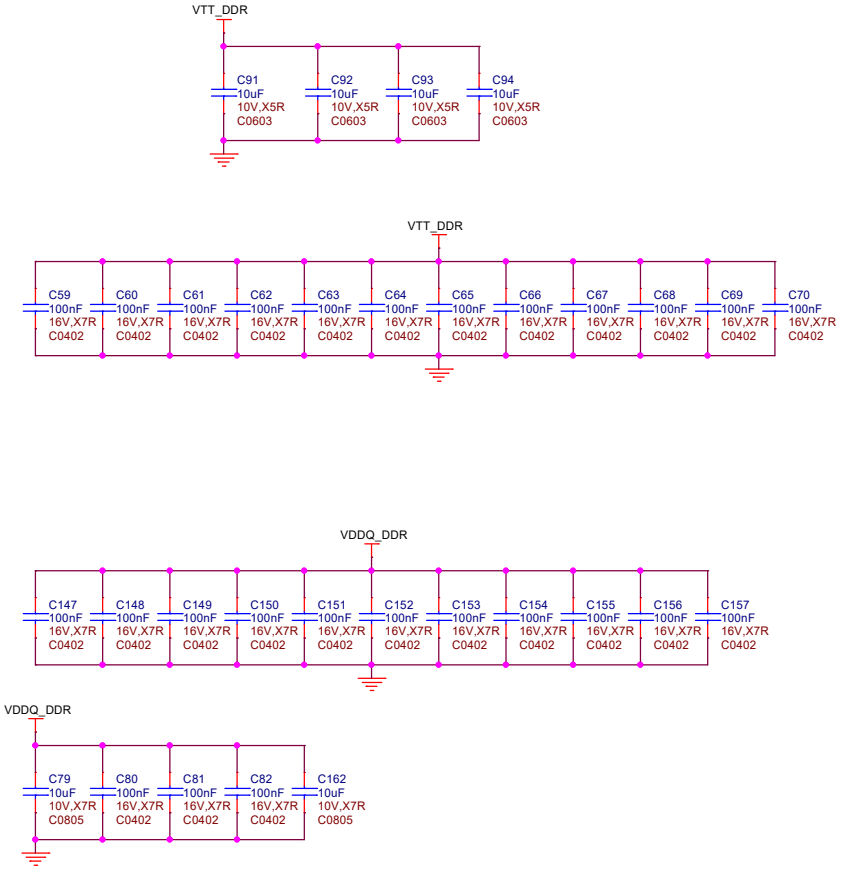

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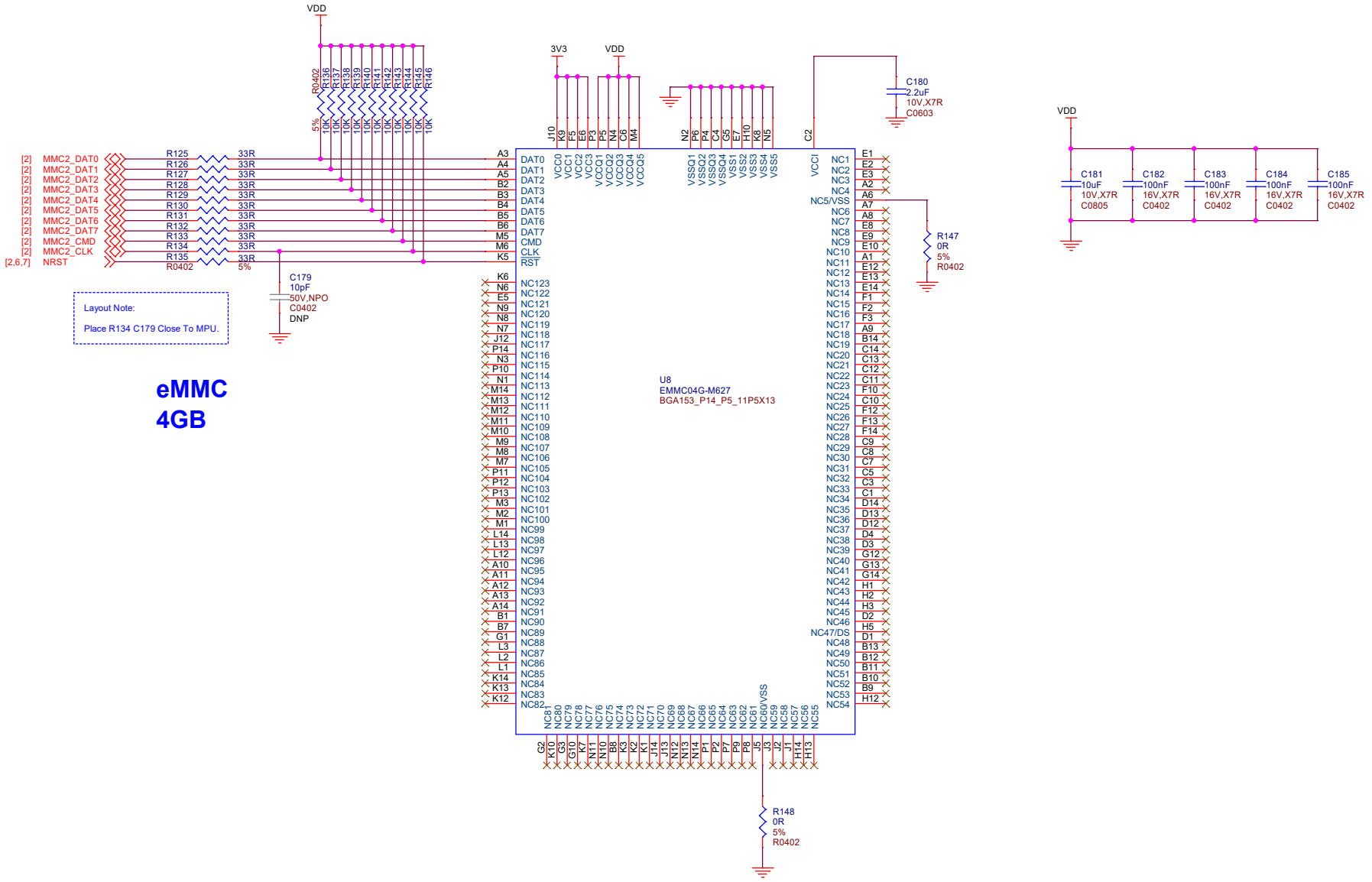
Title:	Seeed SoM - STM32MP157C	
Size: A3	Document Number: 04 DDR3	Rev: v1.01
Draw By: weifeng	Date: Thursday, September 12, 2019	Sheet: 4 of 7



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Title: Seeed SoM - STM32MP157C		
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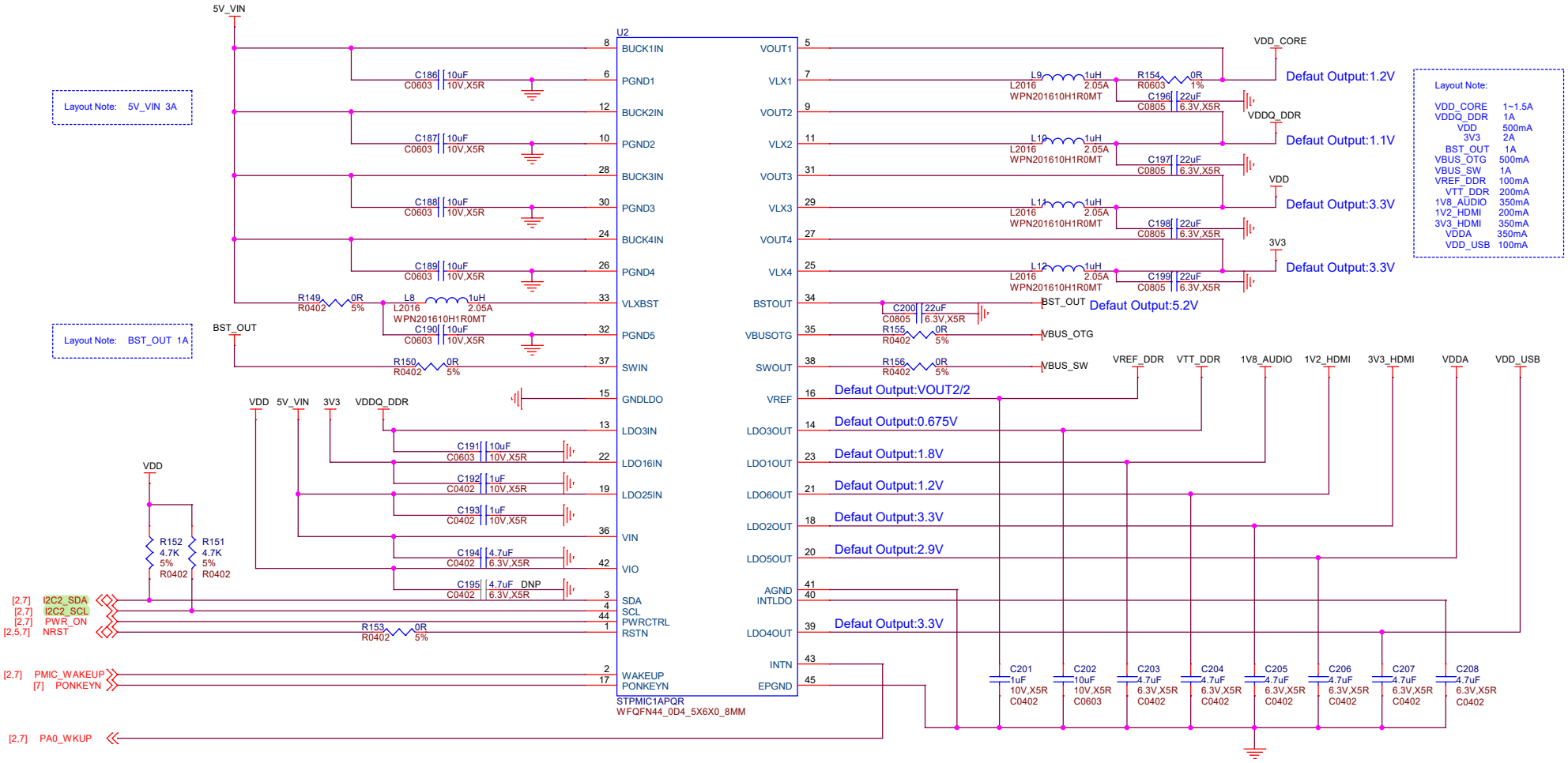

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	Title: Seeed SoM - STM32MP157C	
Size: A3	Document Number: 06 PMU	Rev: v1.01
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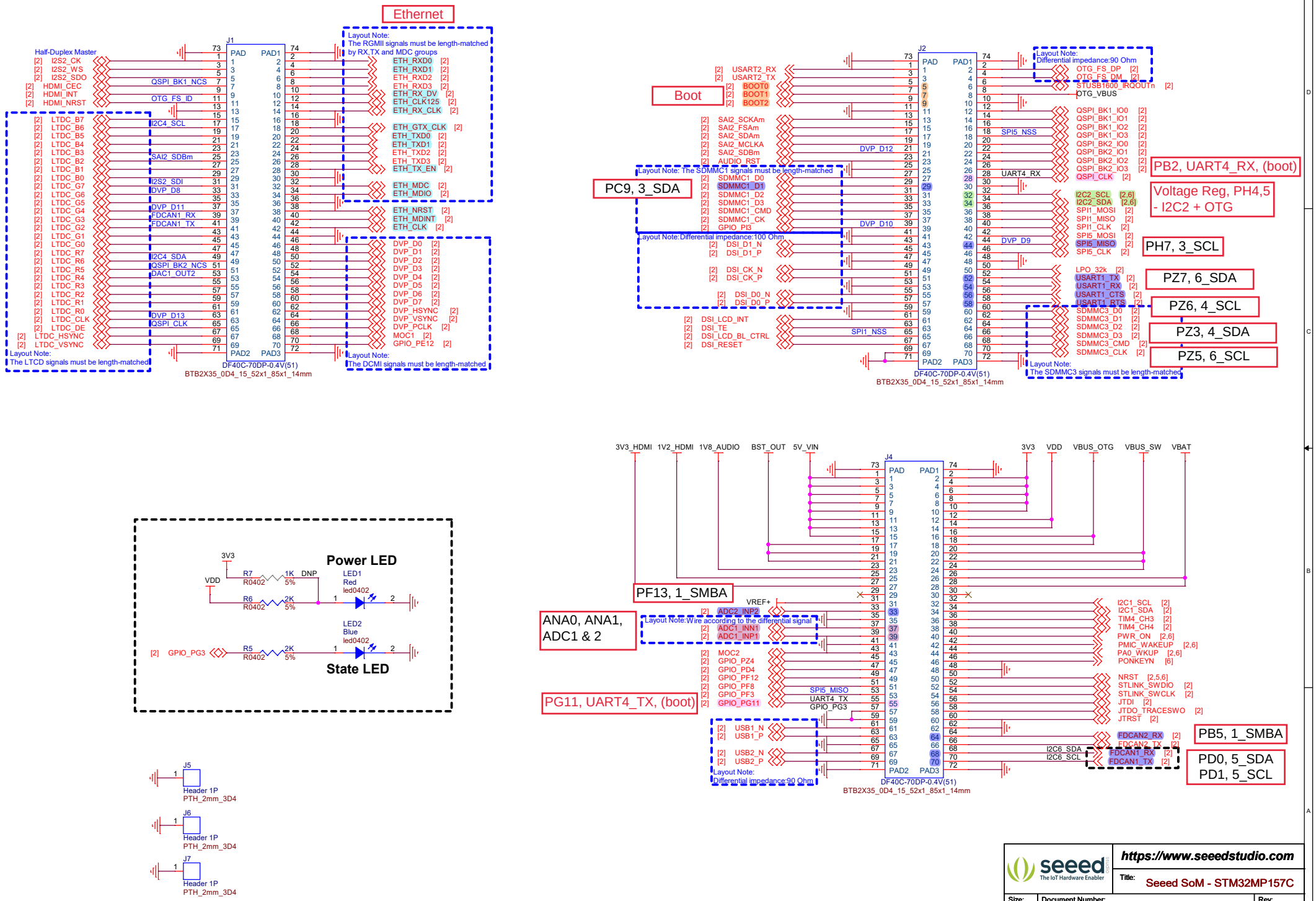
Ethernet
J1
Half-Duplex Master
Layout Note:
The RGMII signals must be length-matched by RX,TX and MDC groups
Layout Note:
The LTCD signals must be length-matched
Layout Note:
The DCMI signals must be length-matched
DF40C-70DP-0.4V(51)
BTB2X35_0D4_15_52x1_85x1_14mm
Boot
PC9, 3_SDA
Layout Note: The SDMMC1 signals must be length-matched
Layout Note:Differential impedance:100 Ohm
J2
Layout Note:
Differential impedance:90 Ohm
Layout Note:
The SDMMC3 signals must be length-matched
PB2, UART4_RX, (boot)
Voltage Reg, PH4,5 - I2C2 + OTG
PH7, 3_SCL
PZ7, 6_SDA
PZ6, 4_SCL
PZ3, 4_SDA
PZ5, 6_SCL
Power LED
LED1
Red
led0402
LED2
Blue
led0402
State LED
J4
PF13, 1_SMBA
ANA0, ANA1, ADC1 & 2
Layout Note:Wire according to the differential signal
PG11, UART4_TX, (boot)
Layout Note:
Differential impedance:90 Ohm
PB5, 1_SMBA
PD0, 5_SDA
PD1, 5_SCL
J5
J6
J7
Header 1P
PTH_2mm_3D4
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Title: Seeed SoM - STM32MP157C
Size: A3
Document Number: 07 PINOUT/LED
Rev: v1.01
Draw By: weifeng
Date: Friday, December 13, 2019
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