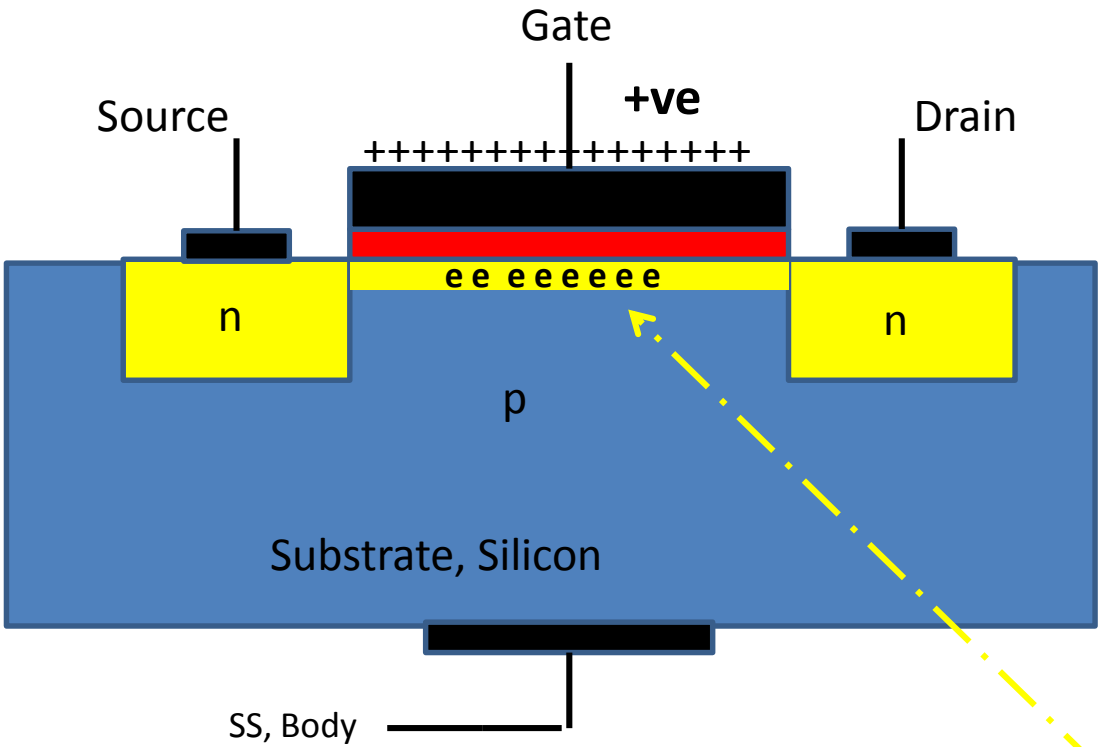
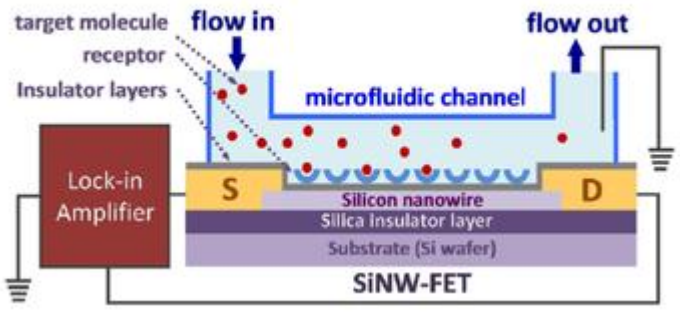
Enhancement MOSFET structure

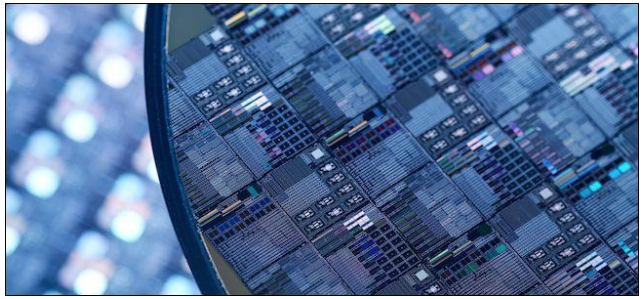




Bio Transistor based on FET technology

Switching Applications of MOS and CMOS Devices

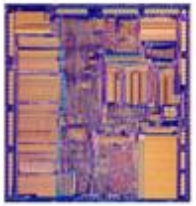
- MOS devices are characterised by their low power consumption
- High Input Impedance
- Ability to form Transistors, Diodes, Capacitors and Resistors from their structure, hence, integrated circuits are constructed from transistors only structure.
- Easy to manufacture, simple device structure, can relate device performance (I_D and gm) to device materials and dimensions.
- Easy to integrate to ultra high scale (ULSI), 7.2 billion transistors per chip(2016).
- Scaling down to nanometre scale is possible, currently (2019) 7 nm technology is available by AMD, TSMC and Samsung
- Can be made from Silicon

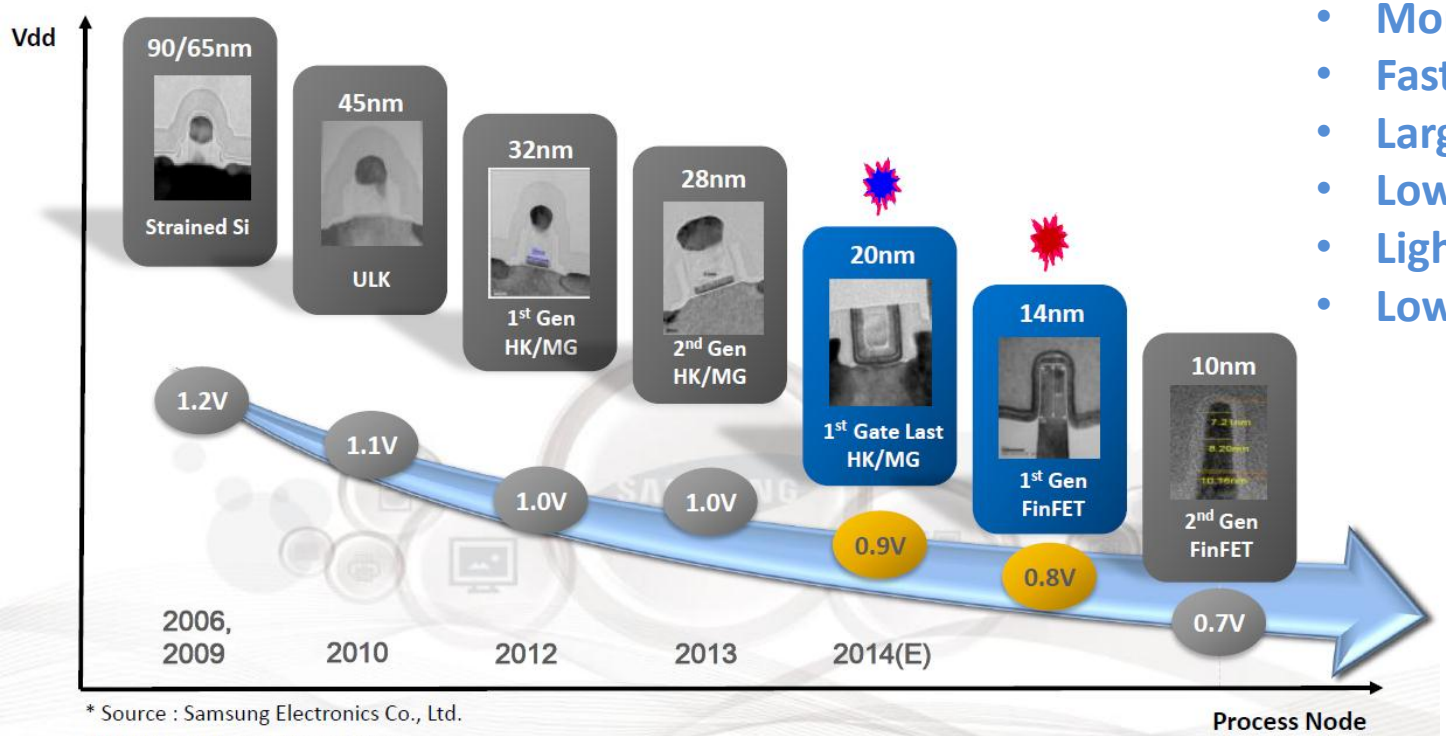


https://hexus.net/tech/news/industry/127382-tsmc-begin-7nm-euv-mass-production-march/
https://www.howtogeek.com/394267/what-do-7nm-and-10nm-mean-and-why-do-they-matter/

Transistor evolution

MOORE'S LAW "Transistor density on integrated circuits doubles about every two years." *

1950s	1960s	1970s	1980s	1990s	2000s
Silicon Transistor	TTL Quad Gate	8-bit Microprocessor	32-bit Microprocessor	32-bit Microprocessor	64-bit Microprocessor
					
1 Transistor	16 Transistors	4500 Transistors	275,000 Transistors	3,100,000 Transistors	592,000,000 Transistors

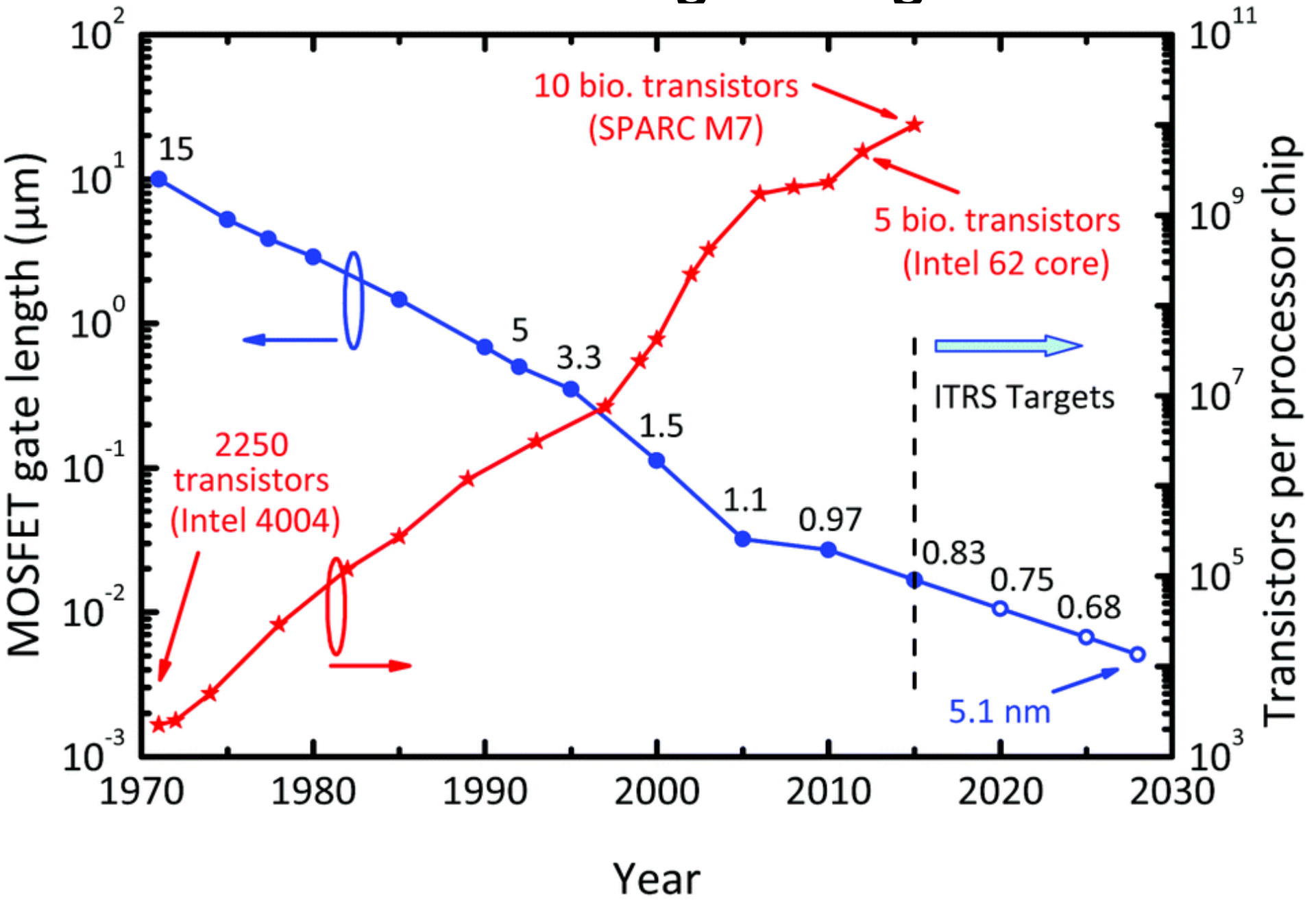


* Source : Samsung Electronics Co., Ltd.
*Vdd : Supplying voltage of drain

- More functionality
- Faster speed
- Larger memory capacity
- Lower power consumption
- Lighter weight
- Lower cost…

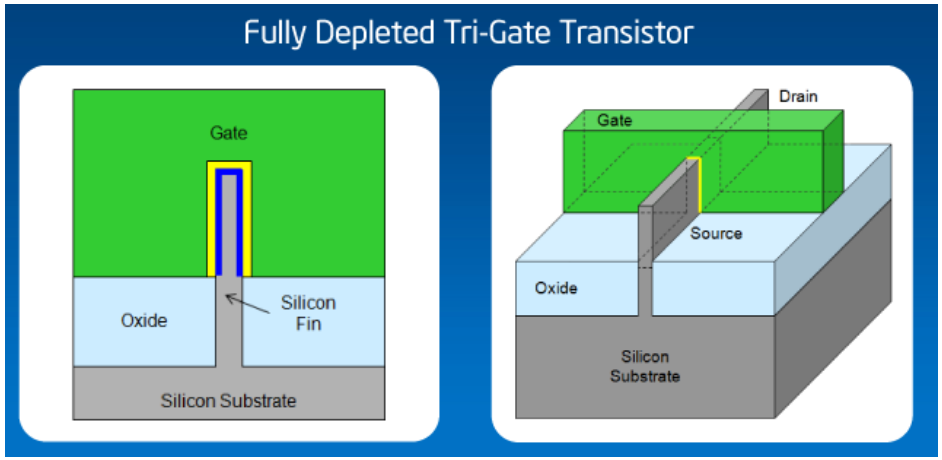
7.2 billion transistors,2016

Transistors gate length

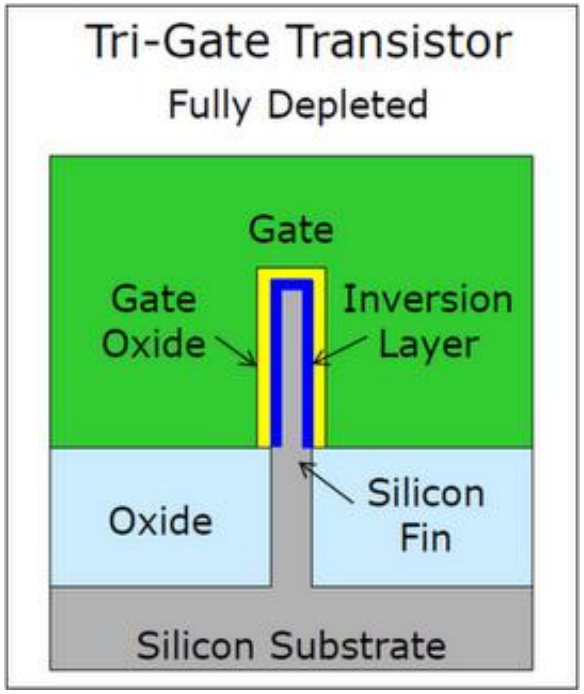


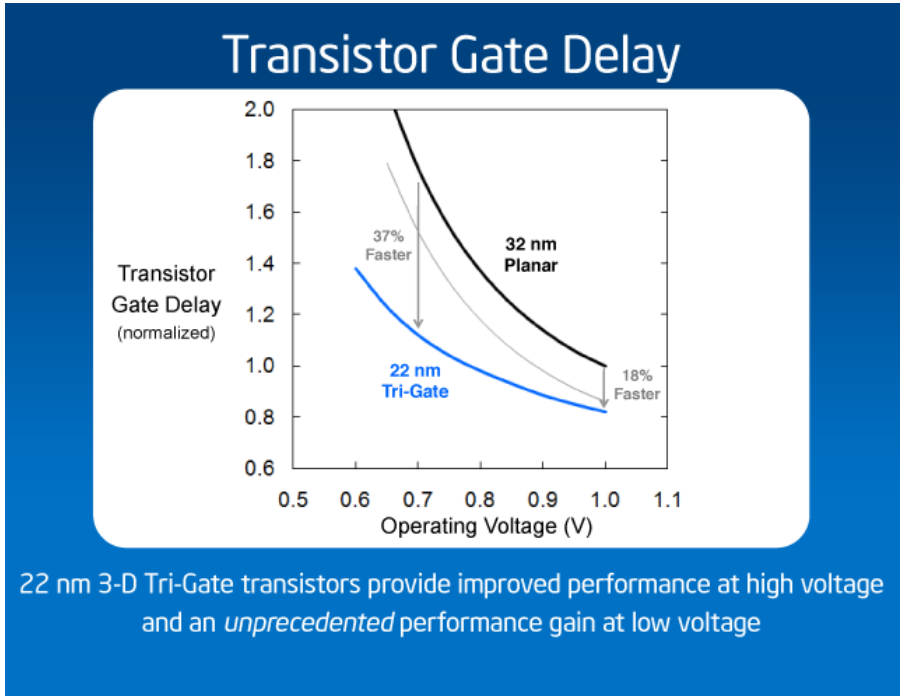
More functionality, continuous development

FinFET

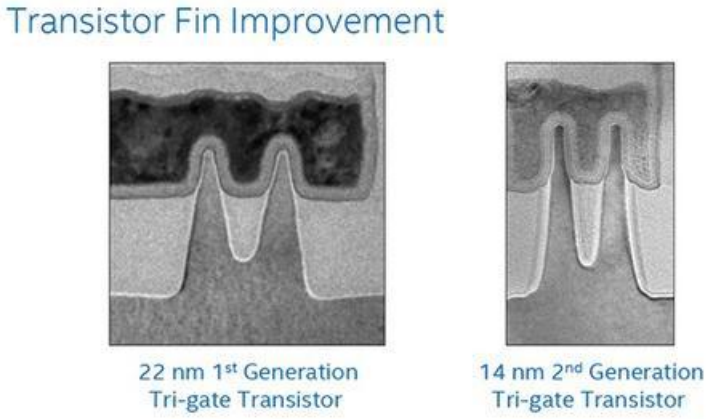


FinFET structure cross section and side view



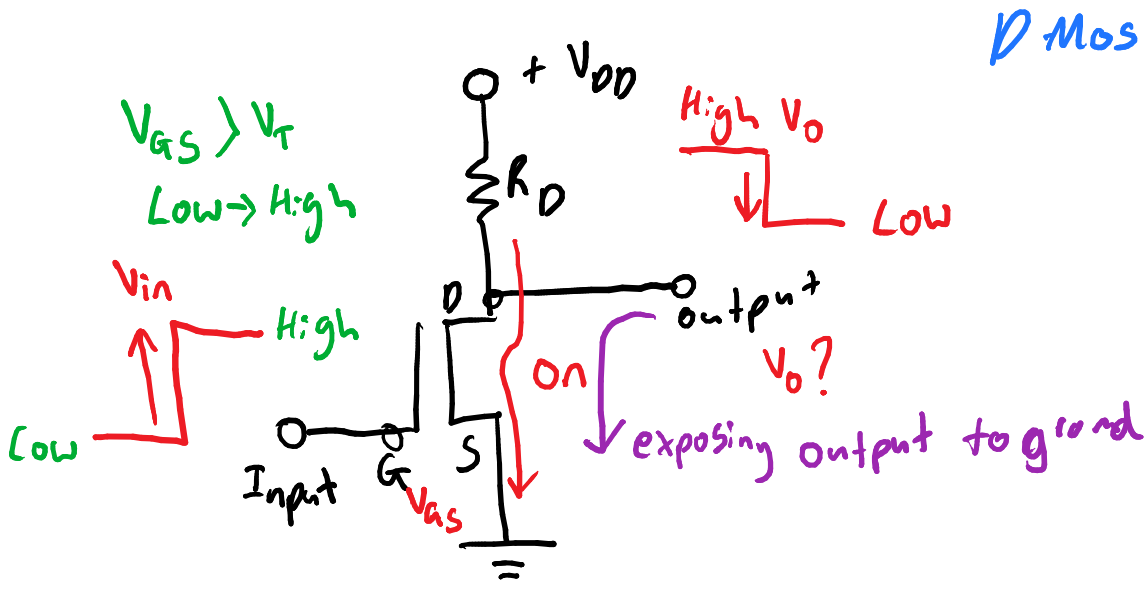


Speed and threshold voltage of FinFET

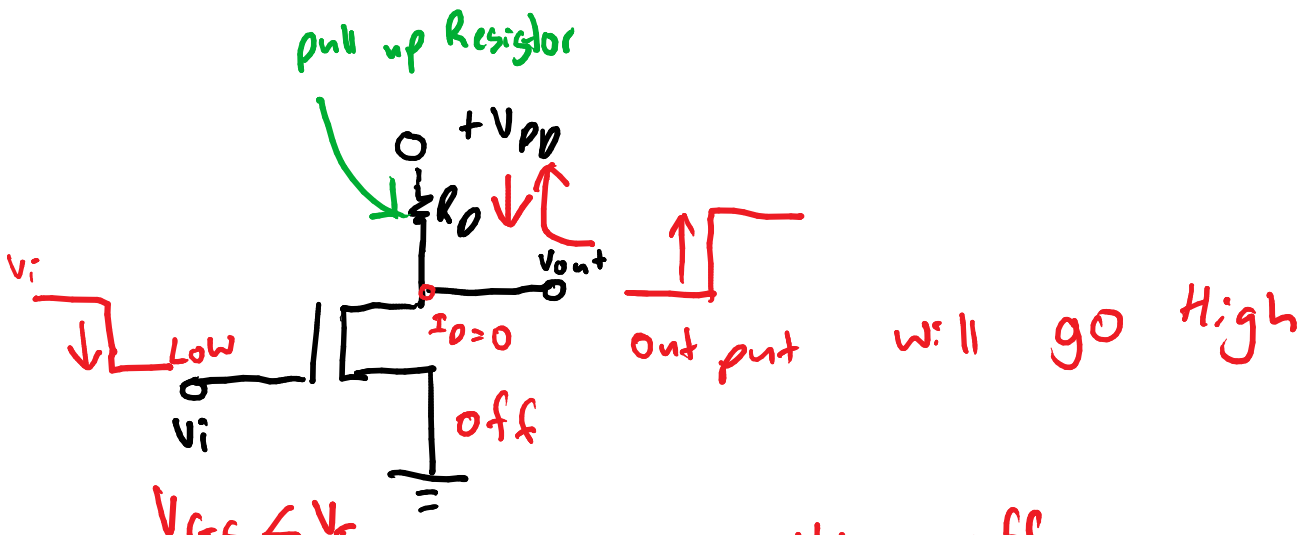


SEM image of FinFET developed by Intel

D Mos fet - pull up resistor

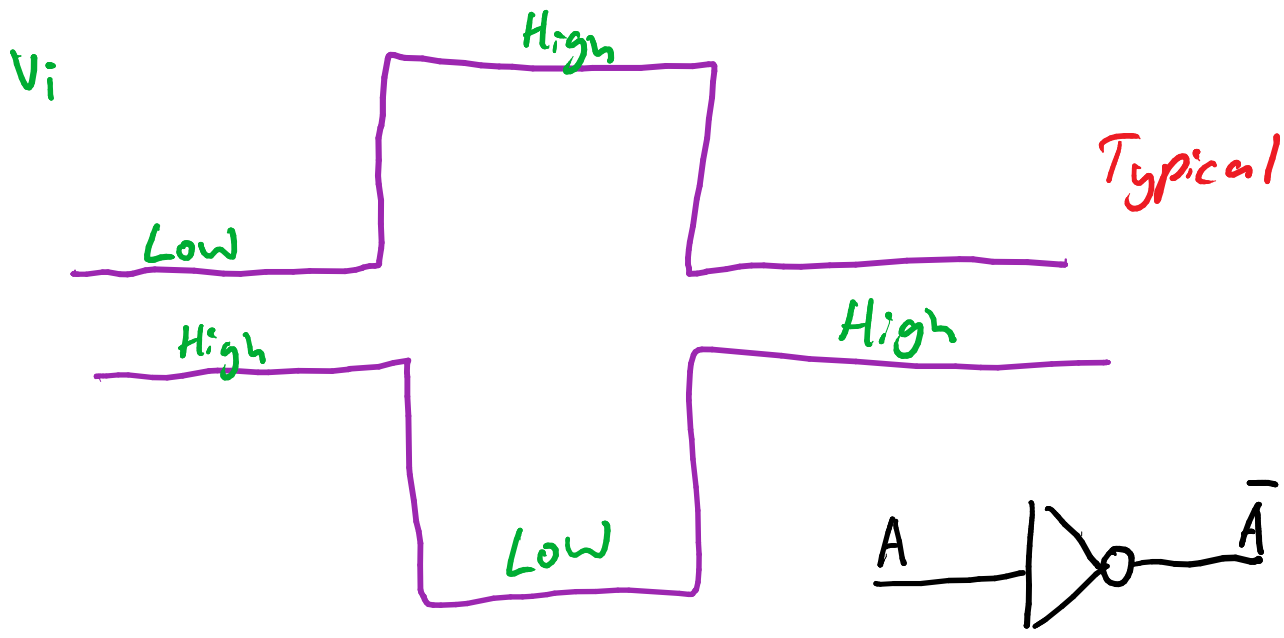


Transistor Switch on



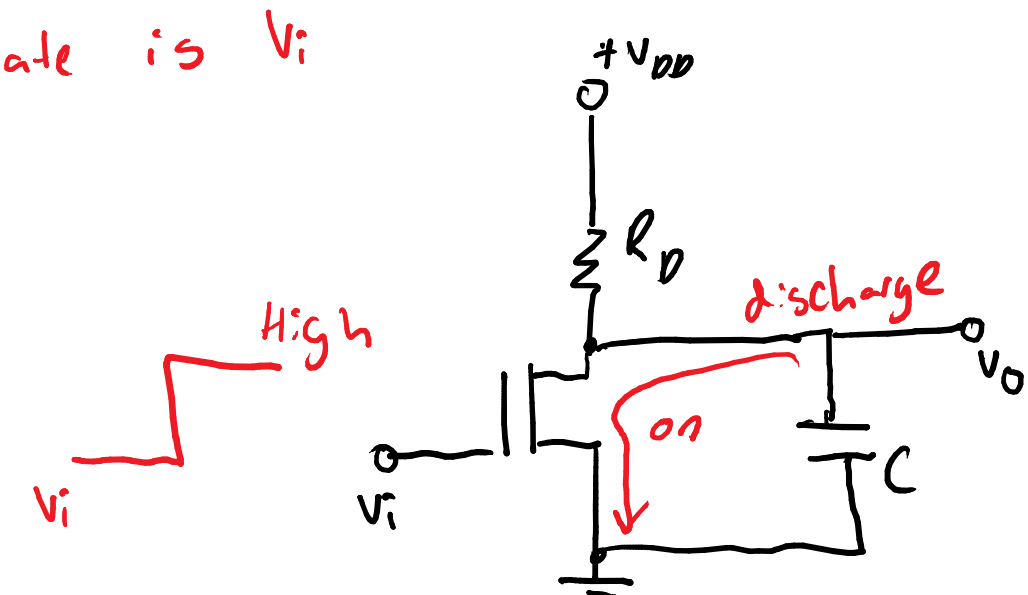
$V_{GS} < V_T$

Transistor switches off



Typical inverter

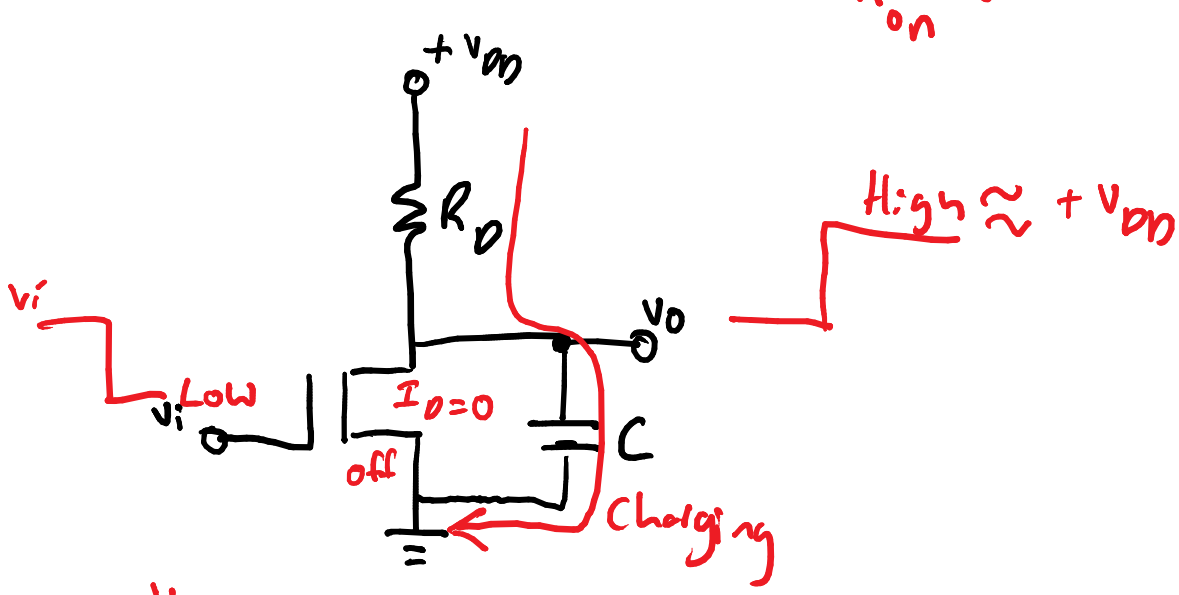
- Drain is V_o
- Gate is V_i



$V_{GS} > V_T$

RC time constant will determine the switch speed

R_{on} of the transistor is 1 Ω



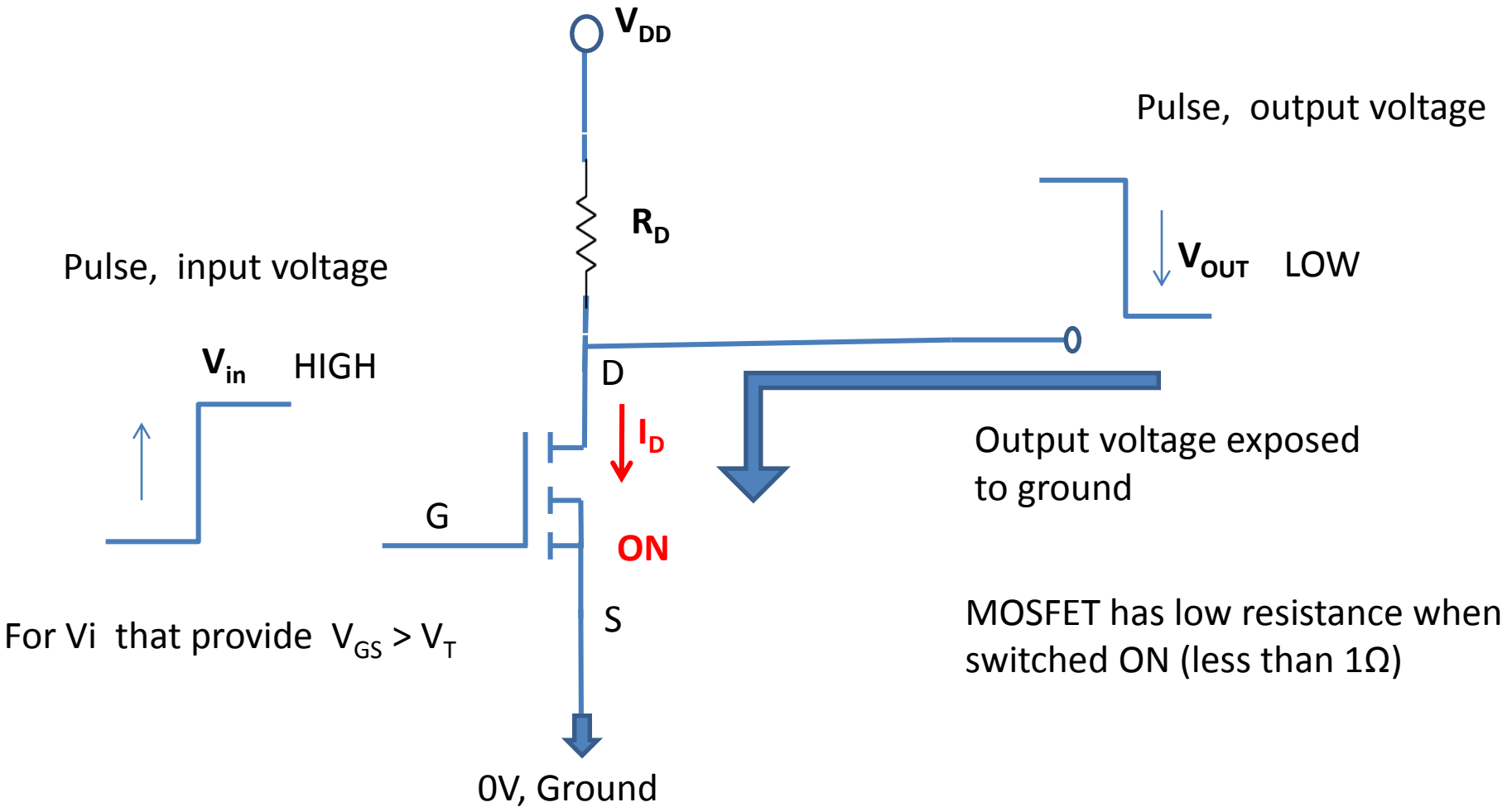
$V_{GS} < V_T$

capacitor charging through R_D.

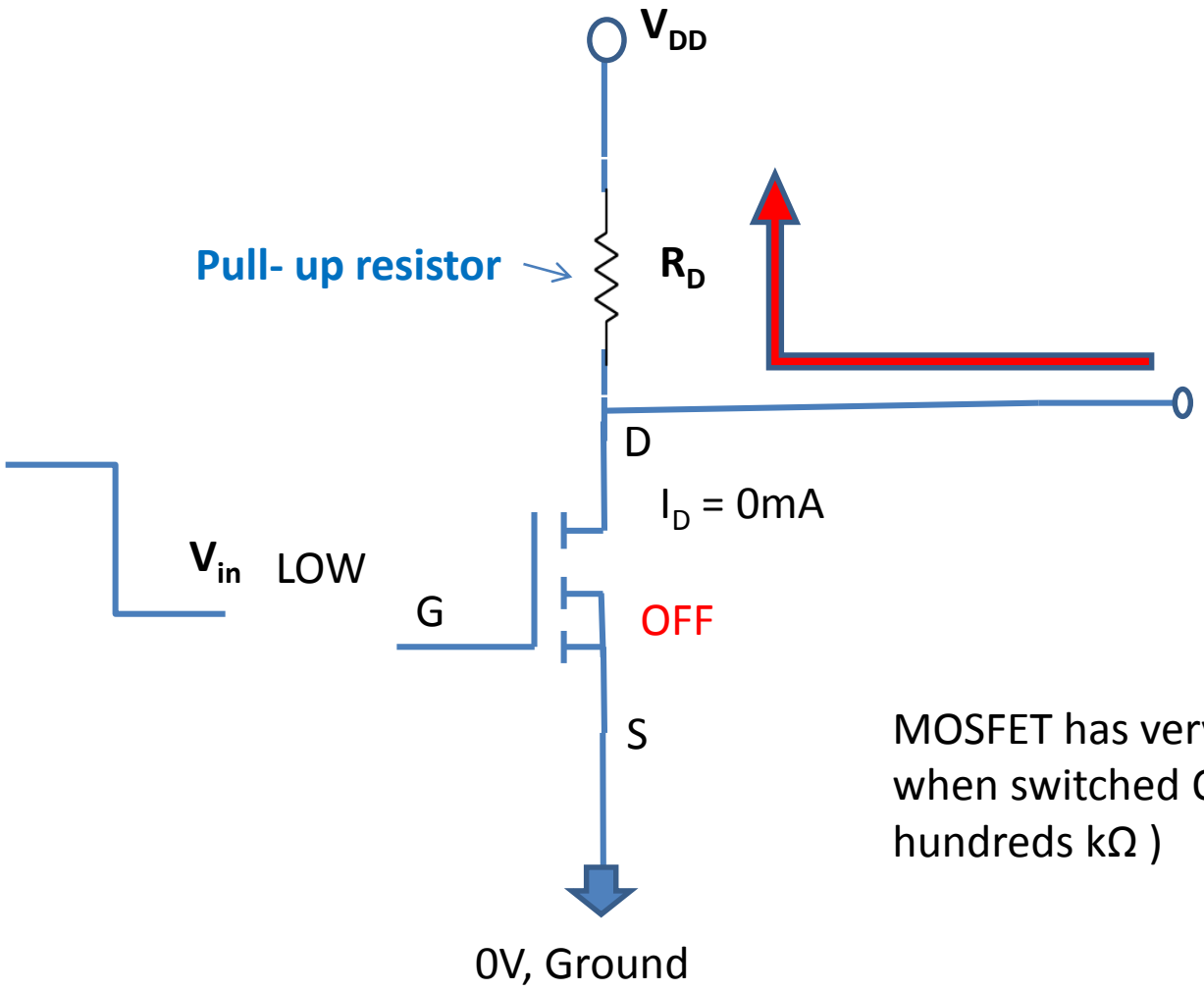
Time constant $R_D \cdot C$

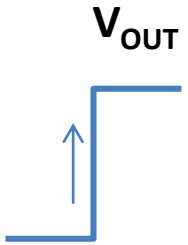
pull up resistor

Basic MOSFET Inverter



Basic MOSFET Inverter



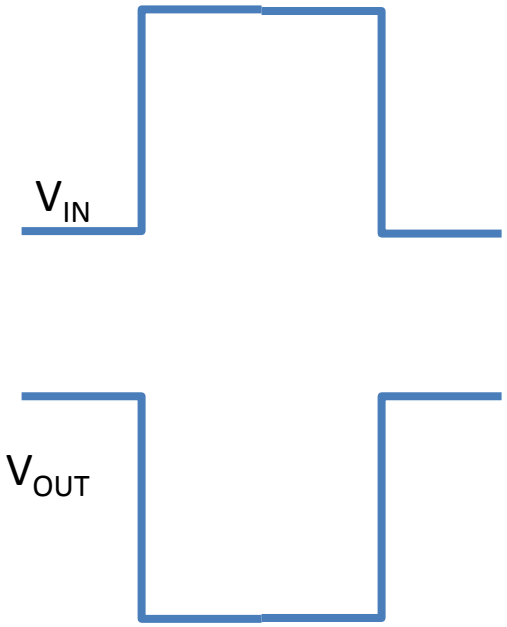


Output Voltage is pulled to V_{DD} when MOSFET is OFF

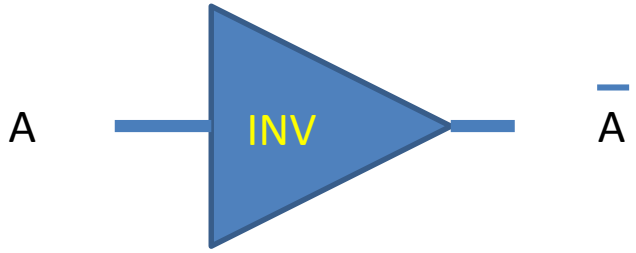
MOSFET has very high resistance when switched OFF (few hundreds kΩ)

MOSFET INVERETER Switching time

- For LOW input the output is HIGH
- For HIGH input the output is LOW
- This is a typical inverter action



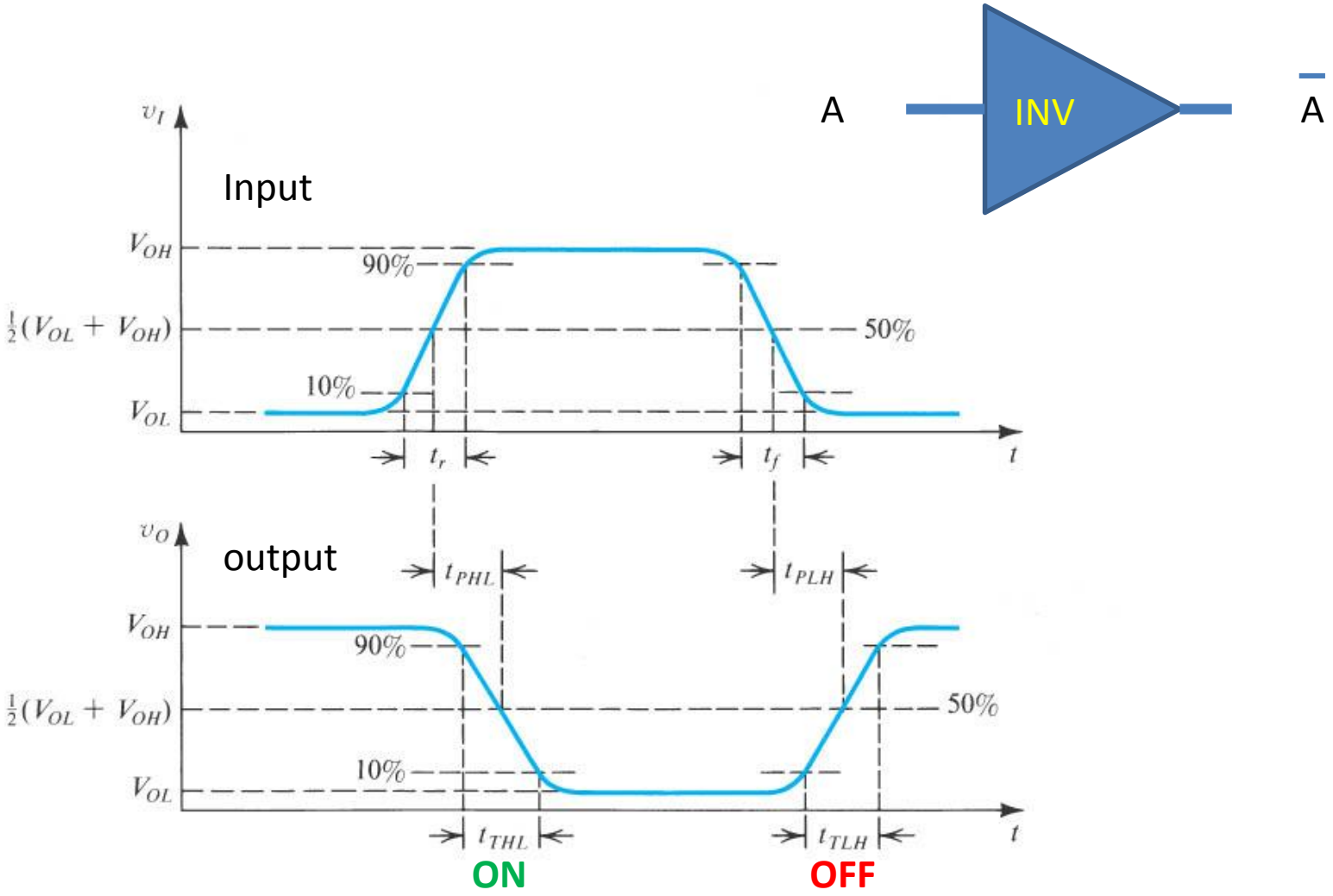
Ideal case



Symbol for Inverter

Output V_{OUT} is inverted relative to the input pulse V_{IN}

Time delay



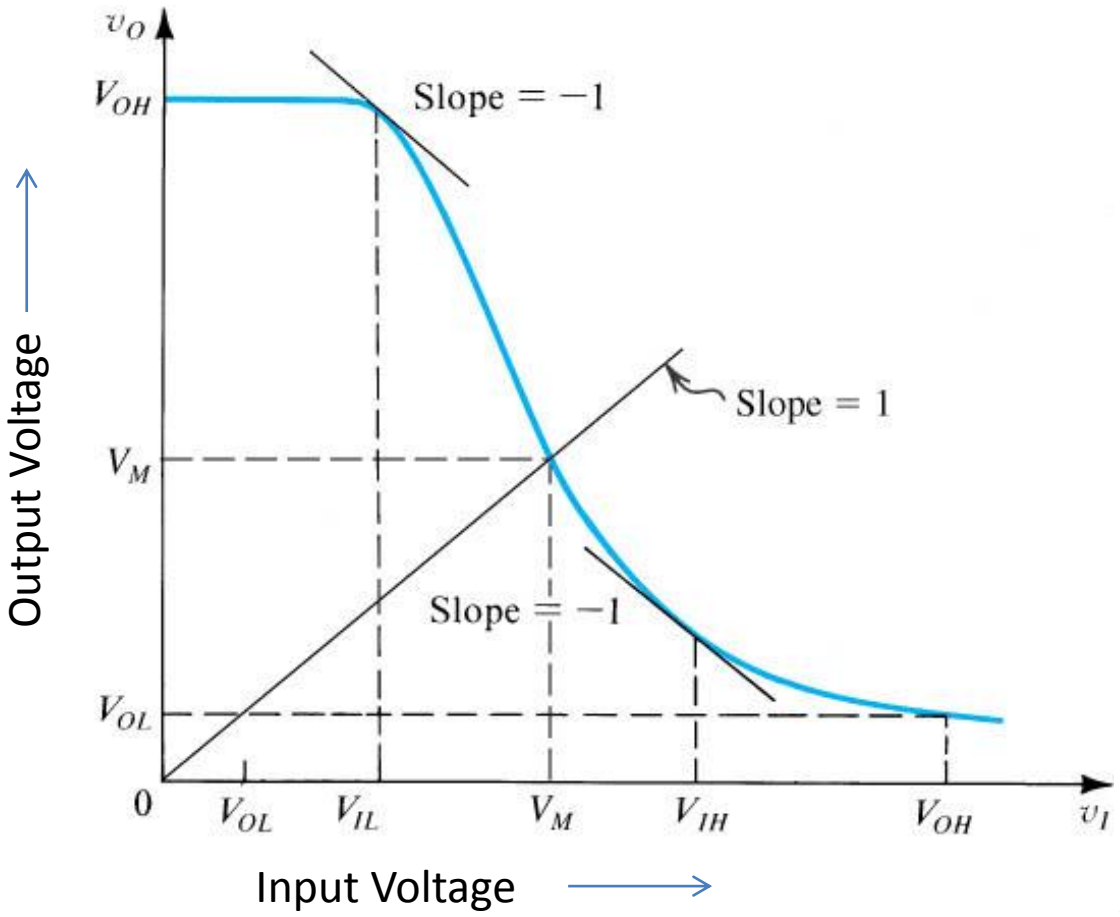
Delay times associated with ON and OFF switching

t_r is the rise time, t_f is the fall time, time it takes to go from 10% to 90% of pulse height

t_{THL} and t_{TLH} are the time for the pulse to go from high to low and from low to high respectively.

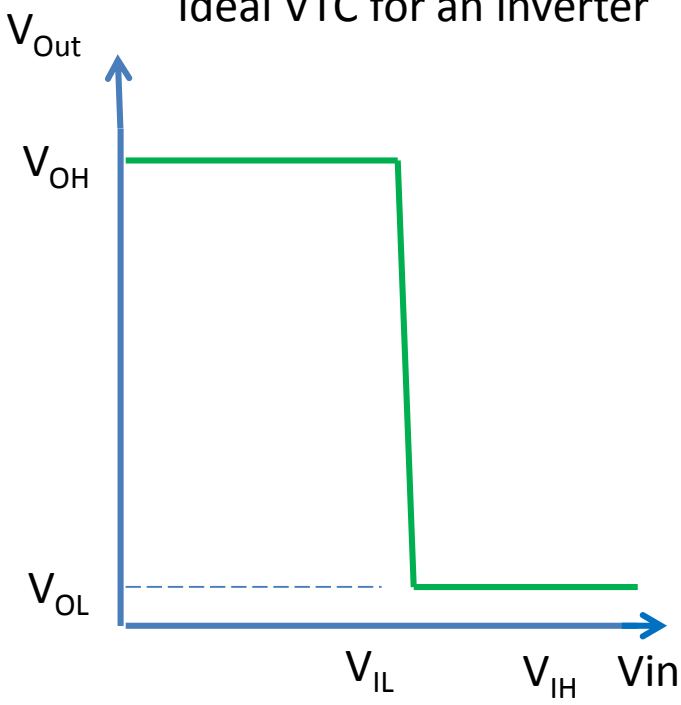
Voltage Transfer Curve VTC for MOS Inverter

Practical VTC



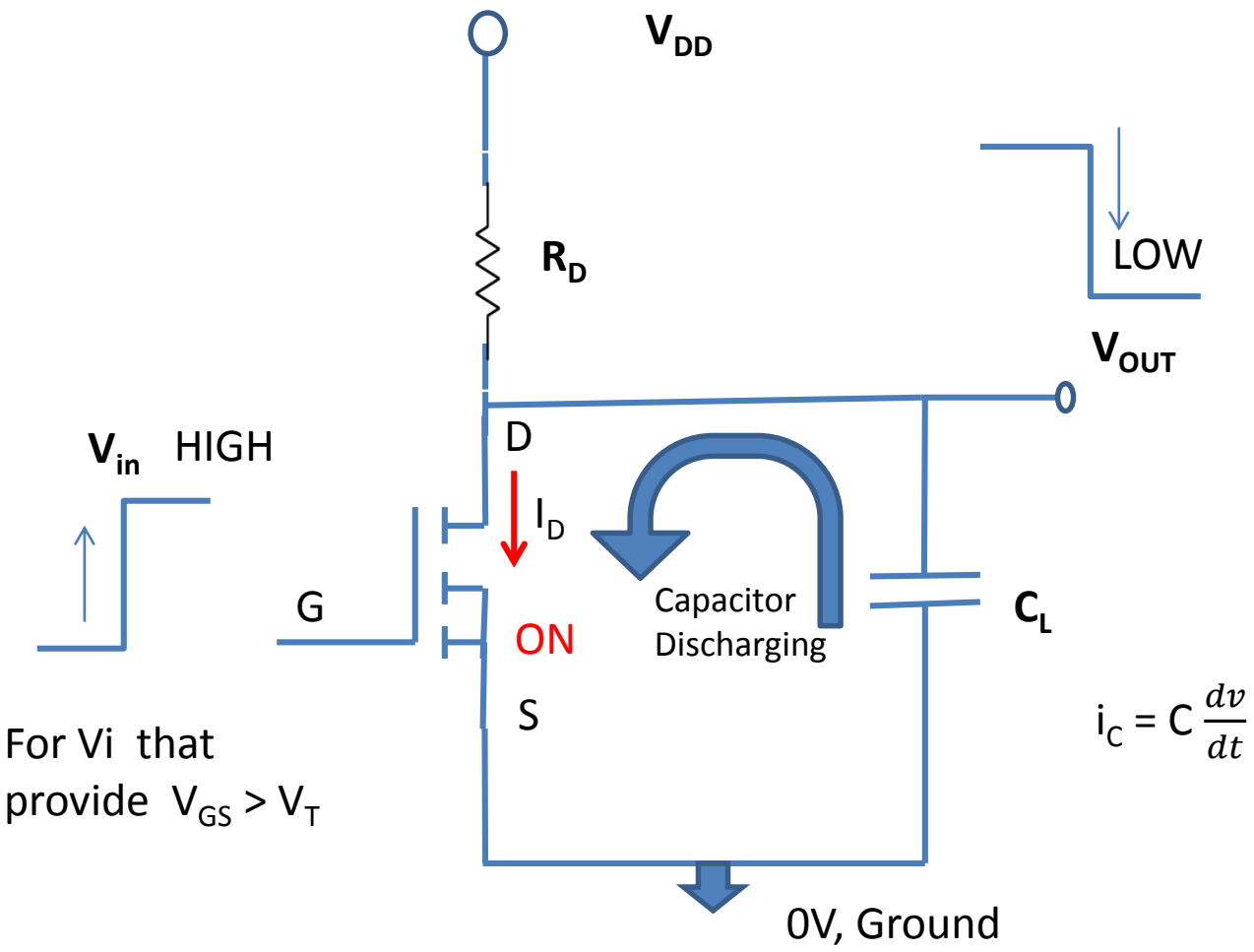
Relationship between input voltage and output voltage

Ideal VTC for an inverter



V_{OH} High Level output voltage
V_{OL} Low Level output voltage
V_{IL} Low Level input voltage
V_{IH} High Level input voltage

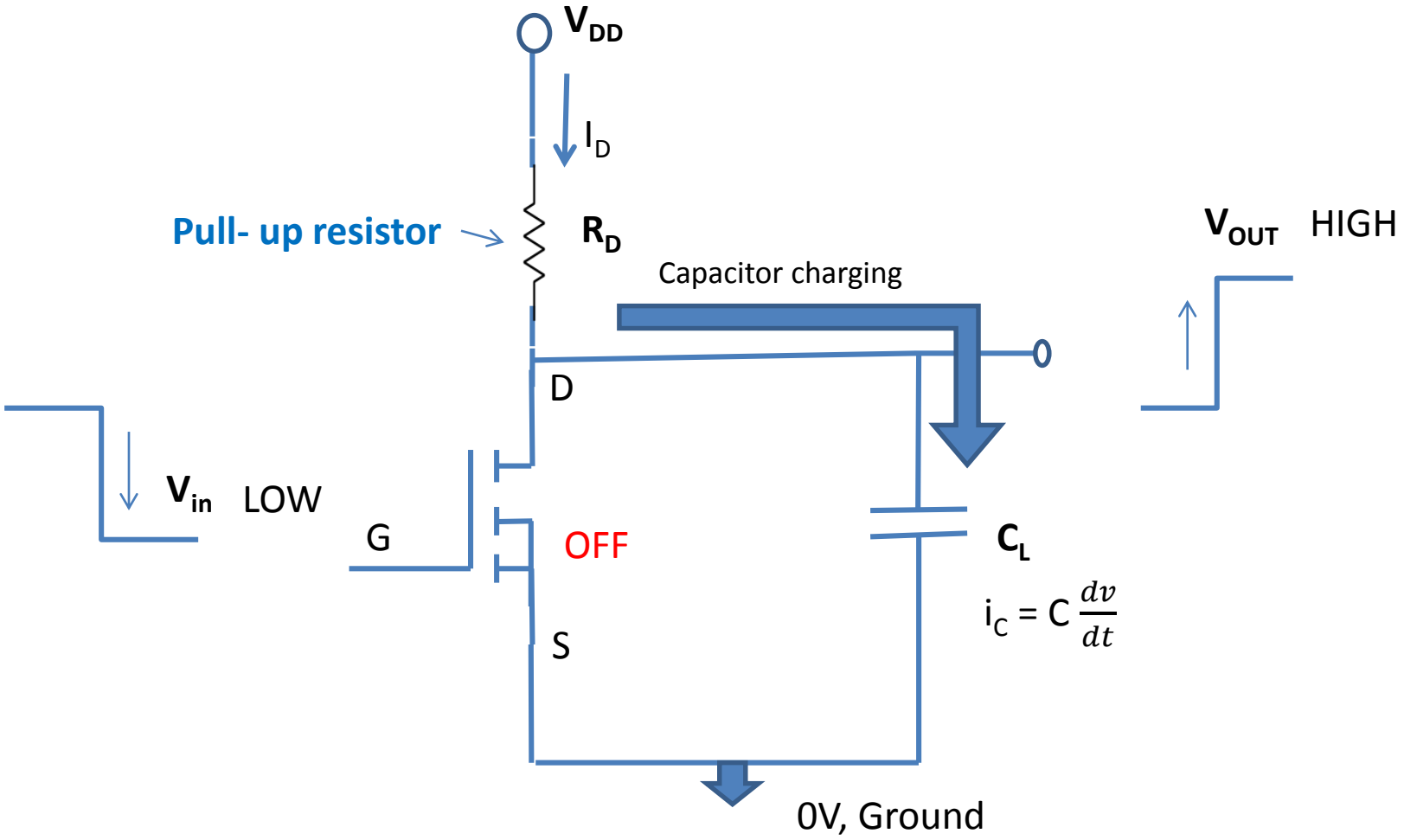
MOSFET Inverter with capacitive load C_L



Capacitor is discharging to ground through the ON switched FET, time constant = R_{on} X C_L

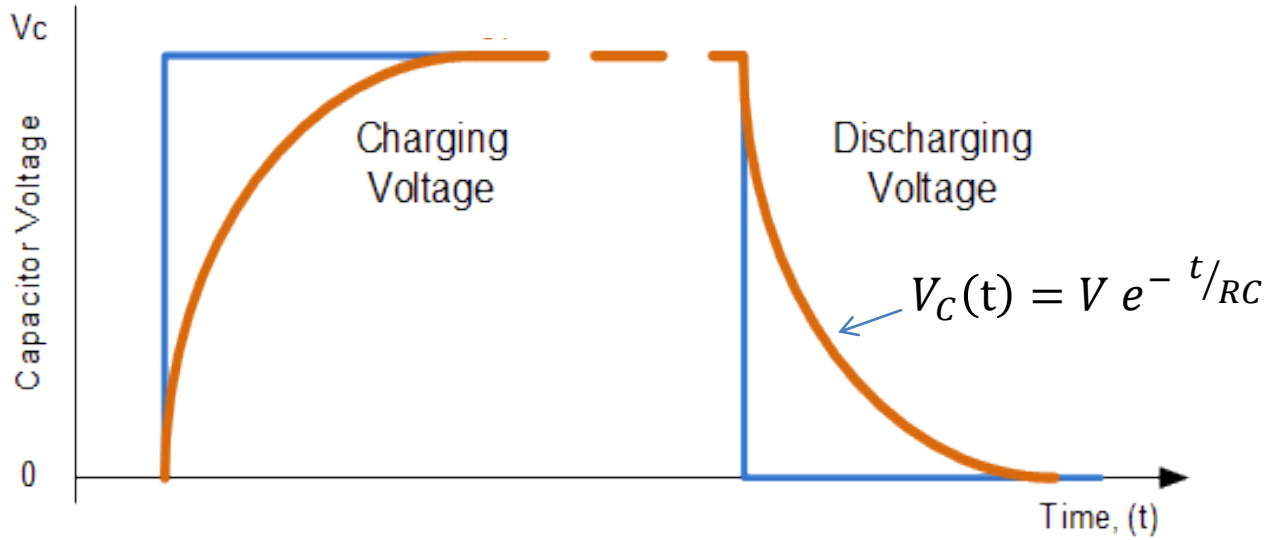
Switching speed is determined by how fast the capacitive load charge and discharge

Vin LOW , capacitor charging



Capacitor is charging through the pull-up resistor R_D to V_{DD}, Time constant = C_L X R_D

Capacitor charging and discharging waveforms



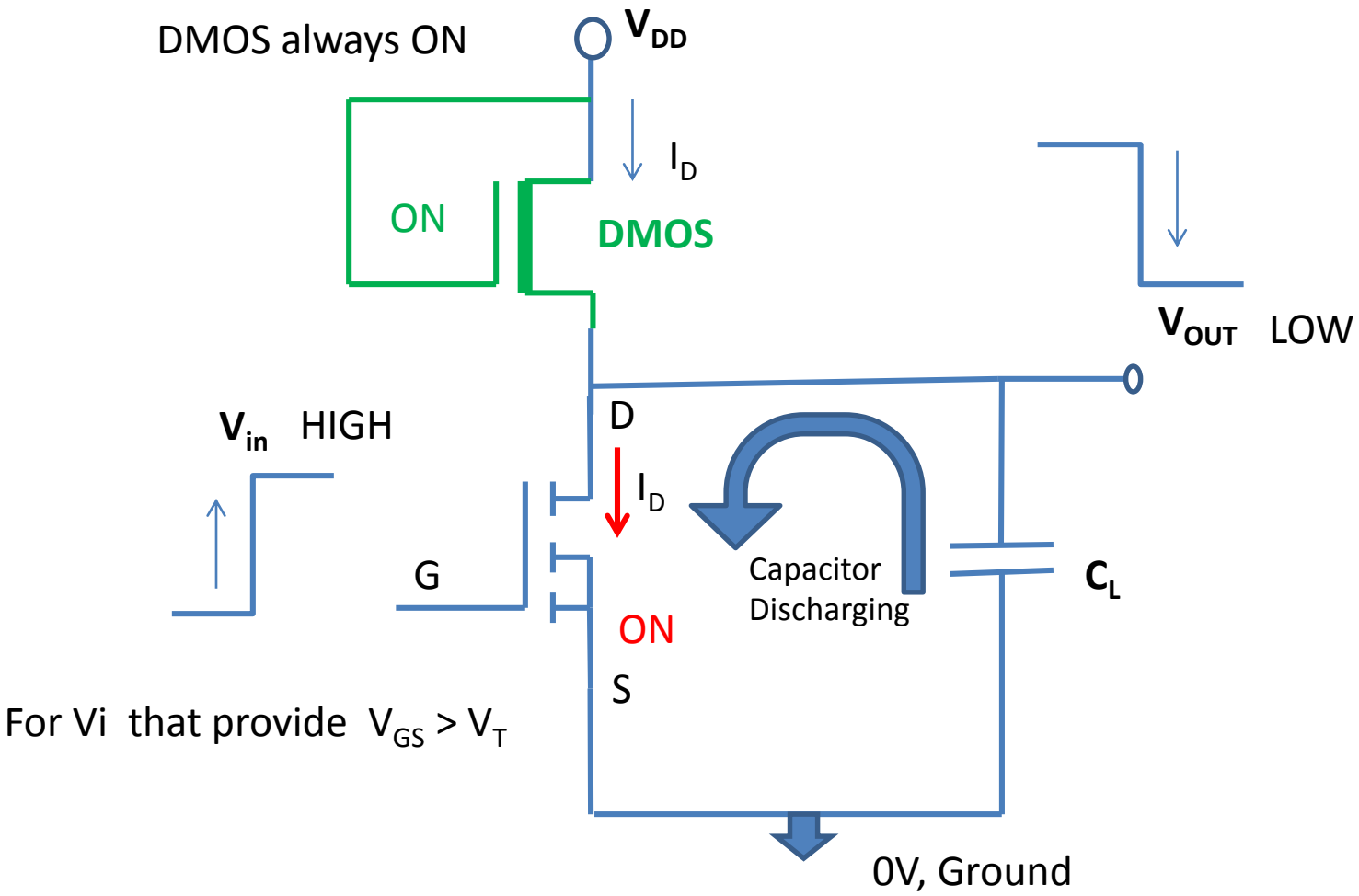
Charging and discharging time depending on the R . C_L time constant

$$C = \frac{\epsilon_o \epsilon_r}{t_{ox}} \mathbf{A}$$

Value of capacitor is determined by the area of device and dielectric properties of the material.

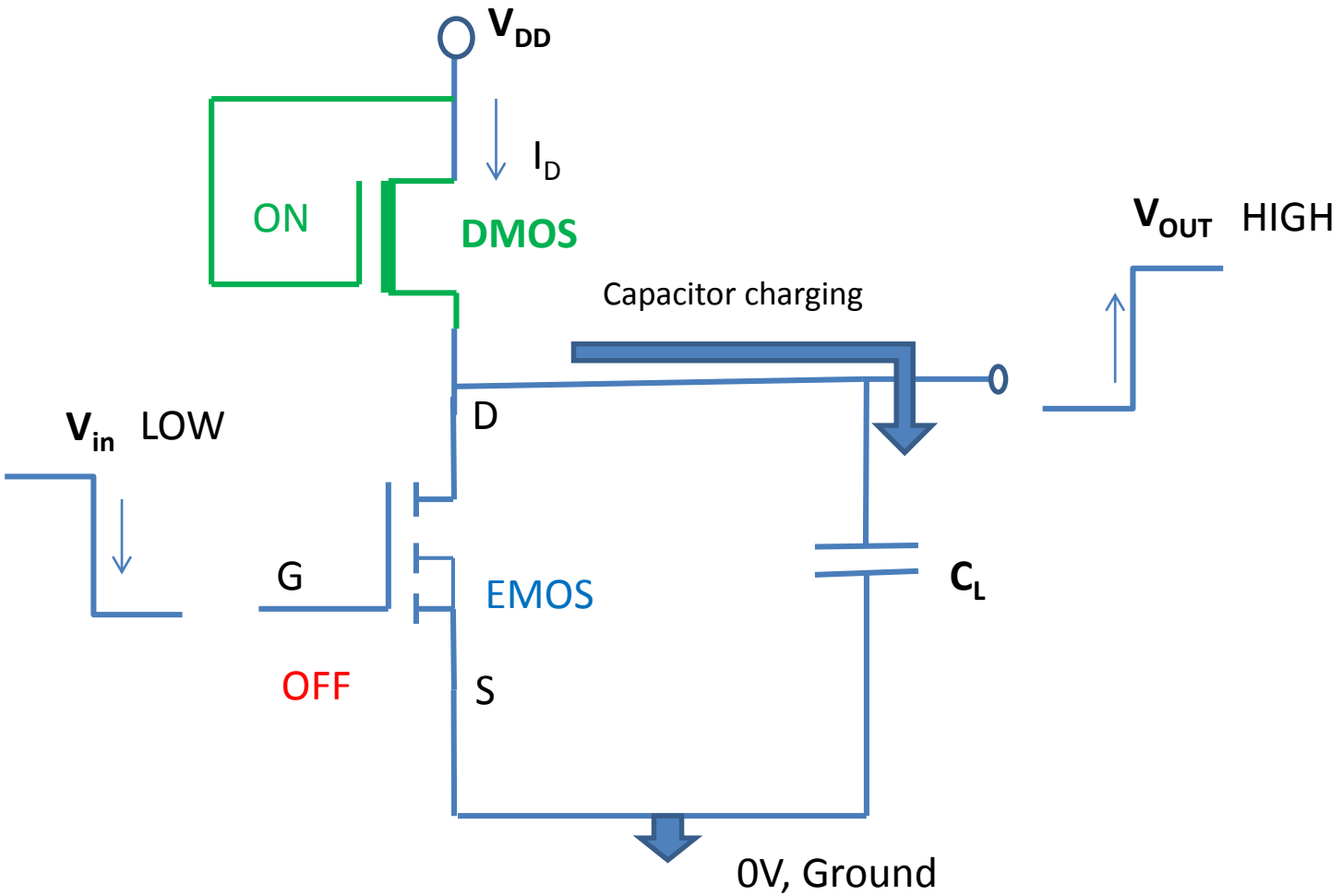
R is determined by the ON resistance of the MOSFET(On state) or the pull up resistor(Off state)

NMOS Switch and DMOS load



DMOS is used as a pull-up resistor, EMOS as switch

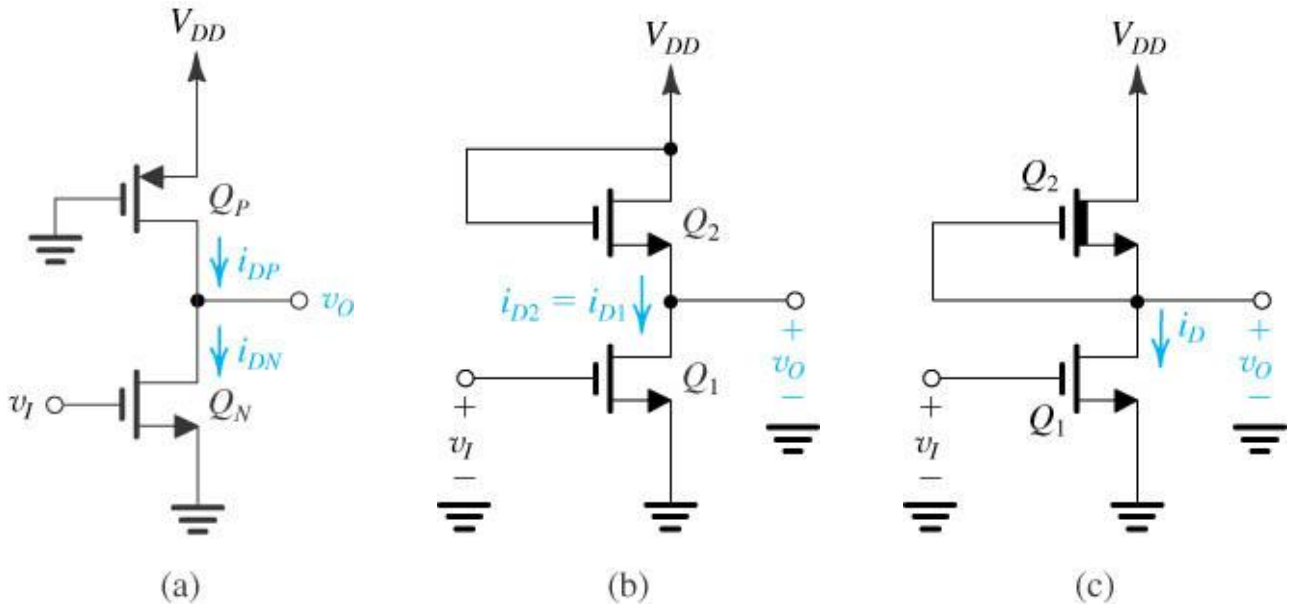
EMOS – DMOS Inverter



When the EMOS is OFF, the capacitor is charging through the DMOS to V_{DD}

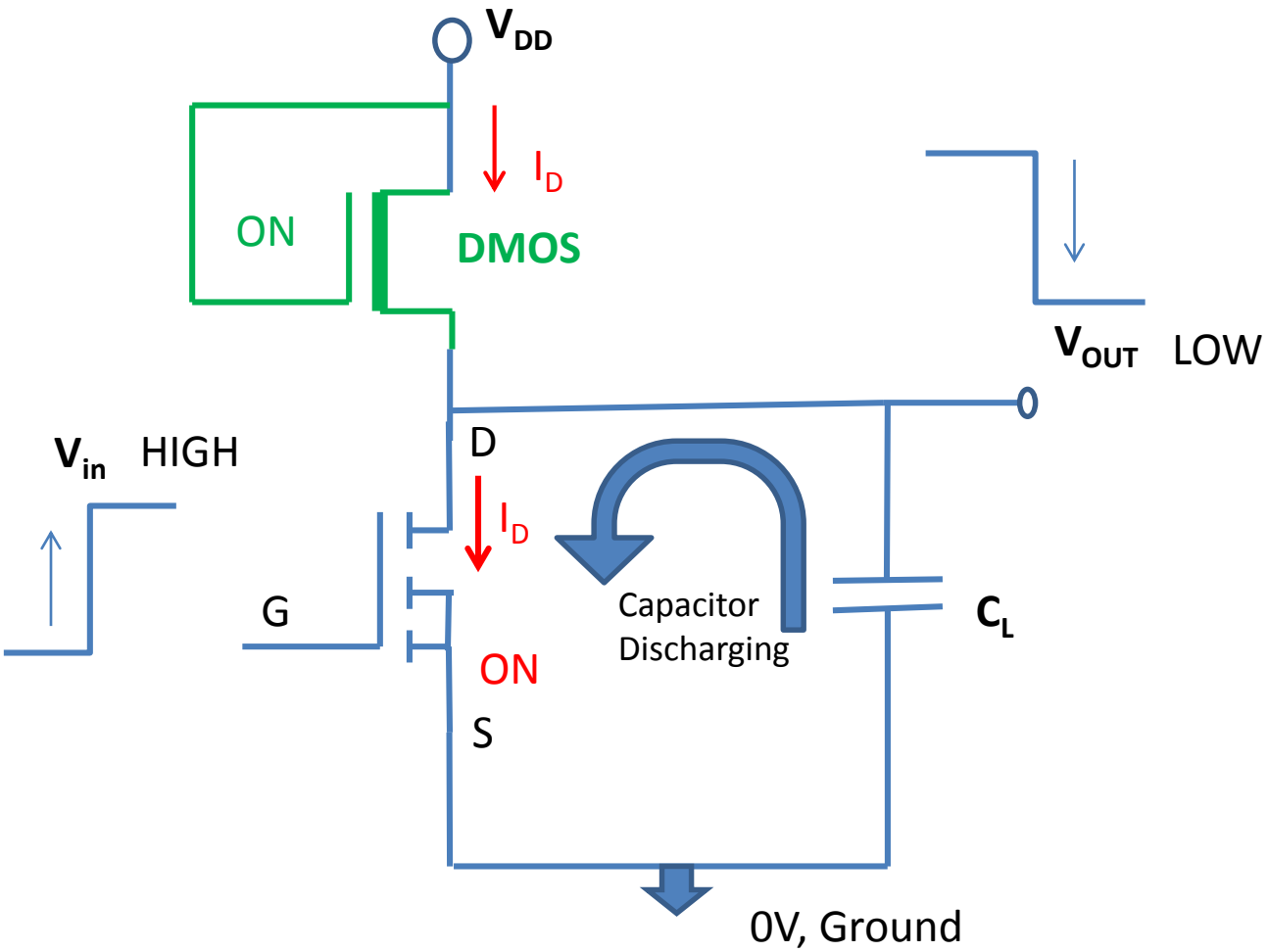
Inverter circuits

Inverters constructed with three design approaches



a) **Inverter with PMOS and NMOS configuration**
b) **Inverter with two NMOS FETs, Q2 is acting as the pull-up resistor**
c) **Inverter constructed with EMOS(Switch) and DMOS resistive, pull up transistor**

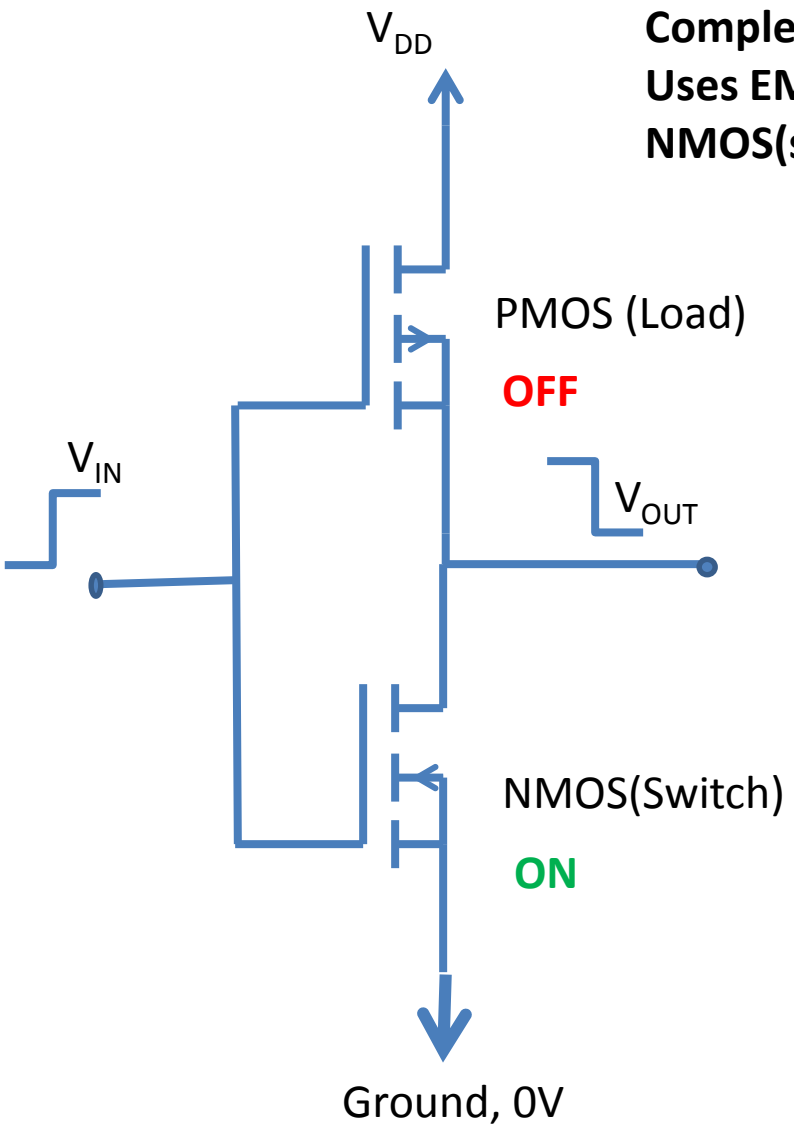
Power consumption problem with DMOS, EMOS inverters



When the EMOS is ON, the DMOS is also ON, exposing the power supply to ground and the power consumption is high .

Basic CMOS Inverter

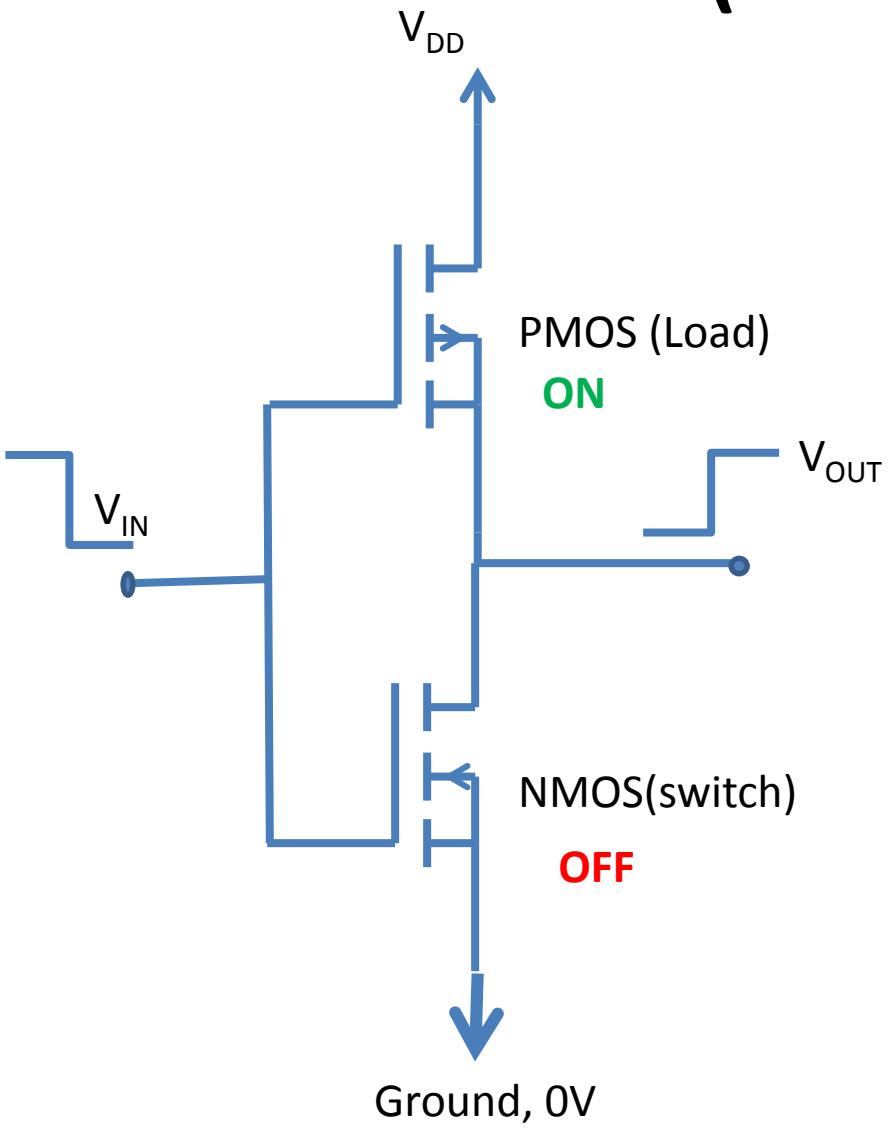
Complementary Metal Oxide Semiconductor Technology
Uses EMOS in both PMOS (resistive load) and NMOS(switch)configurations .



CMOS inverter

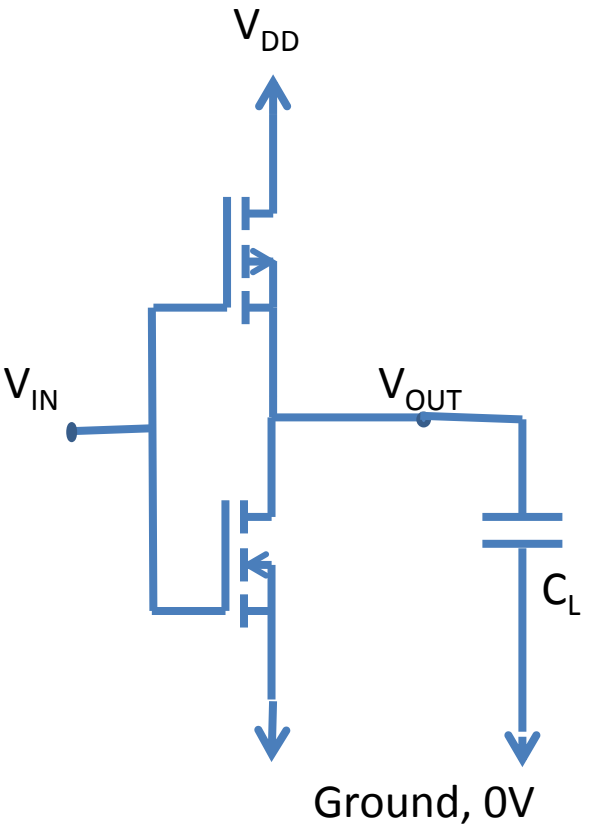
When the input voltage is HIGH and larger than the threshold voltage V_T
The NOMS is switched ON, V_{OUT} is LOW,
The PMOS is OFF, cutting V_{DD} from ground reducing power consumption.

Complementary Metal Oxide Semiconductor (CMOS) FET

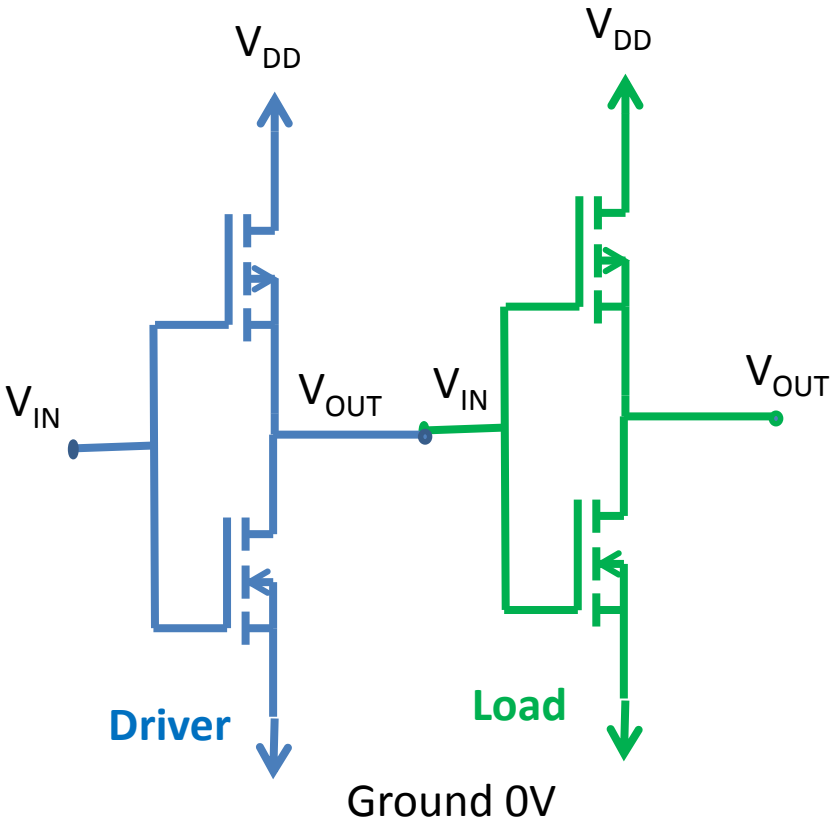


When the input voltage V_{IN} is LOW
NMOS is OFF
PMOS is ON and pulling the output voltage V_{OUT} to V_{DD}(HIGH).

CMOS Loading



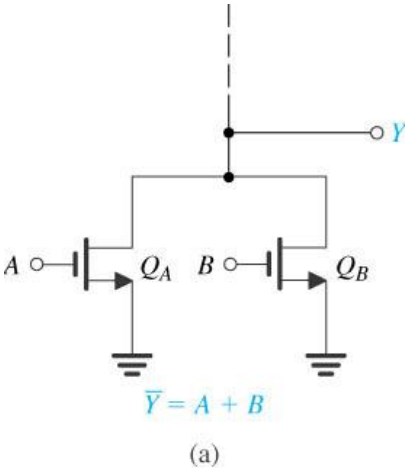
Capacitive load, charging through the PMOS, Discharging through the NOMS, the ON resistances of the PMOS and NMOS will determine the switching speed



CMOS driver, CMOS load

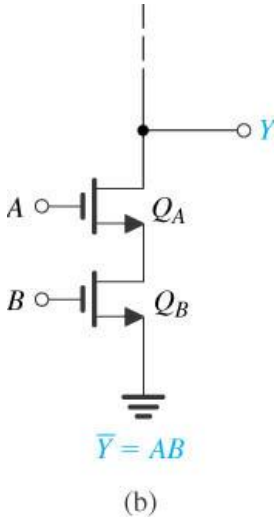
Output of driver is input to the load. Input is through the gate which is isolated from the channel with oxide, ie capacitive load.

Basic Digital Gates



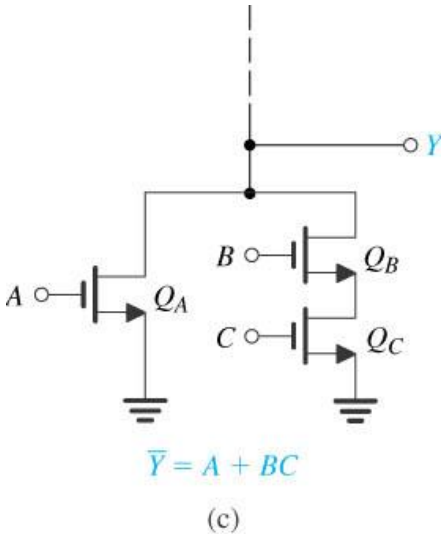
NOR gate

$Y = \overline{A+B}$



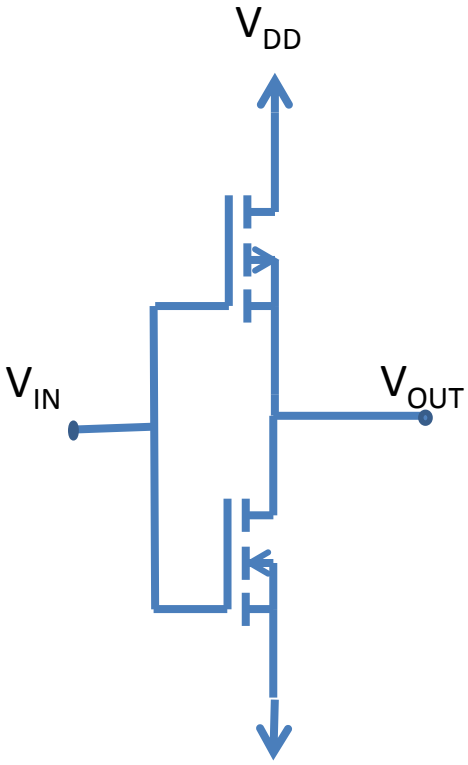
NAND gate

$Y = \overline{A.B}$



Implementation of a Boolean function

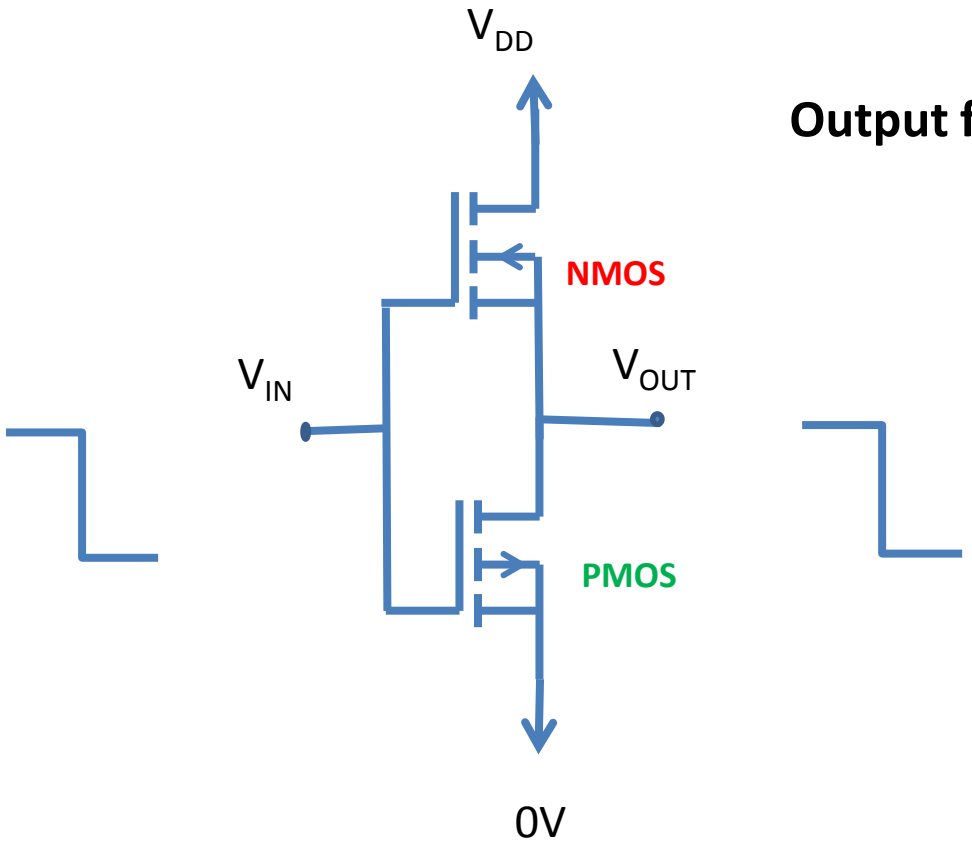
$Y = \overline{A + B.C}$



Ground, 0V

$V_{OUT} = \overline{V_{IN}}$

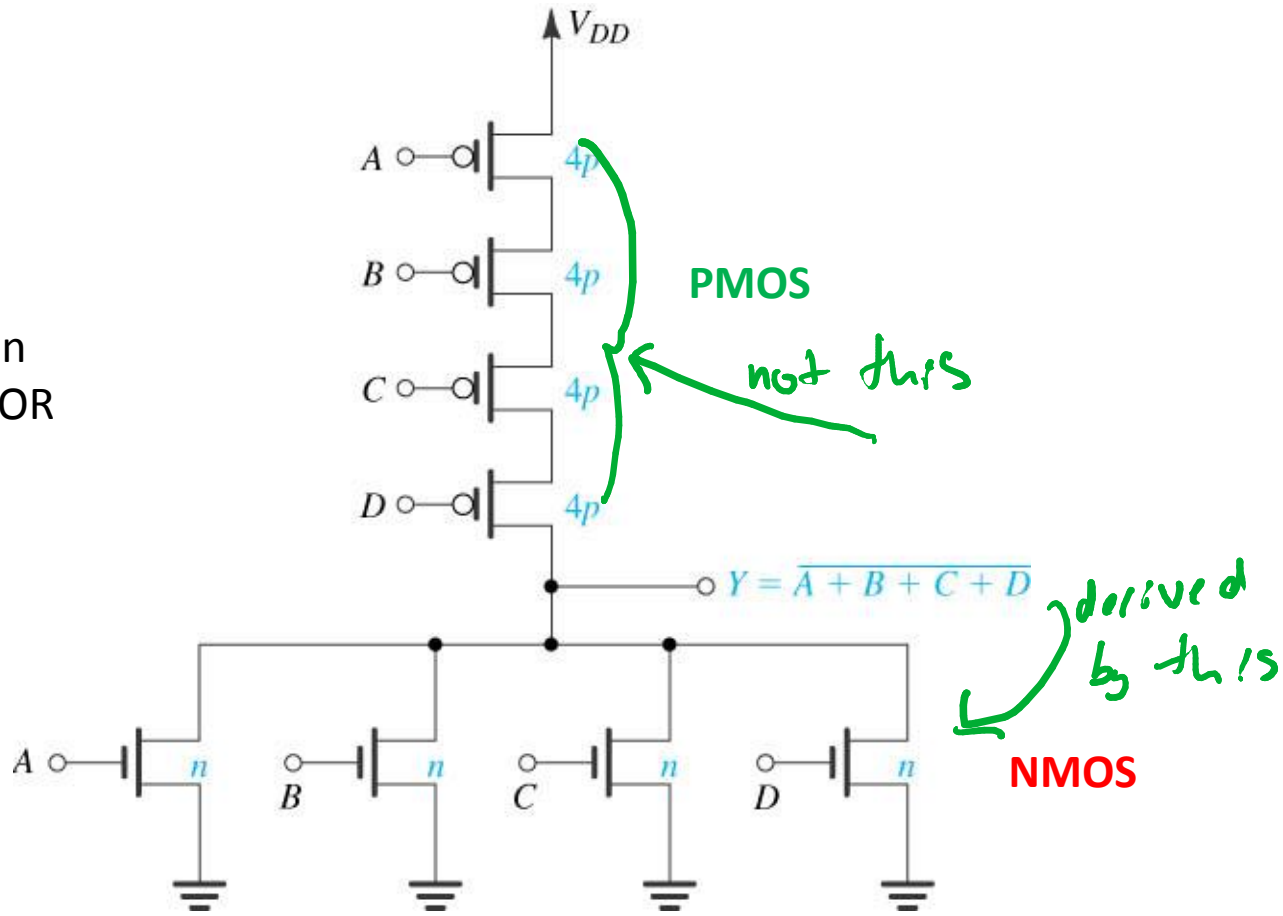
CMOS Non-Inverting case



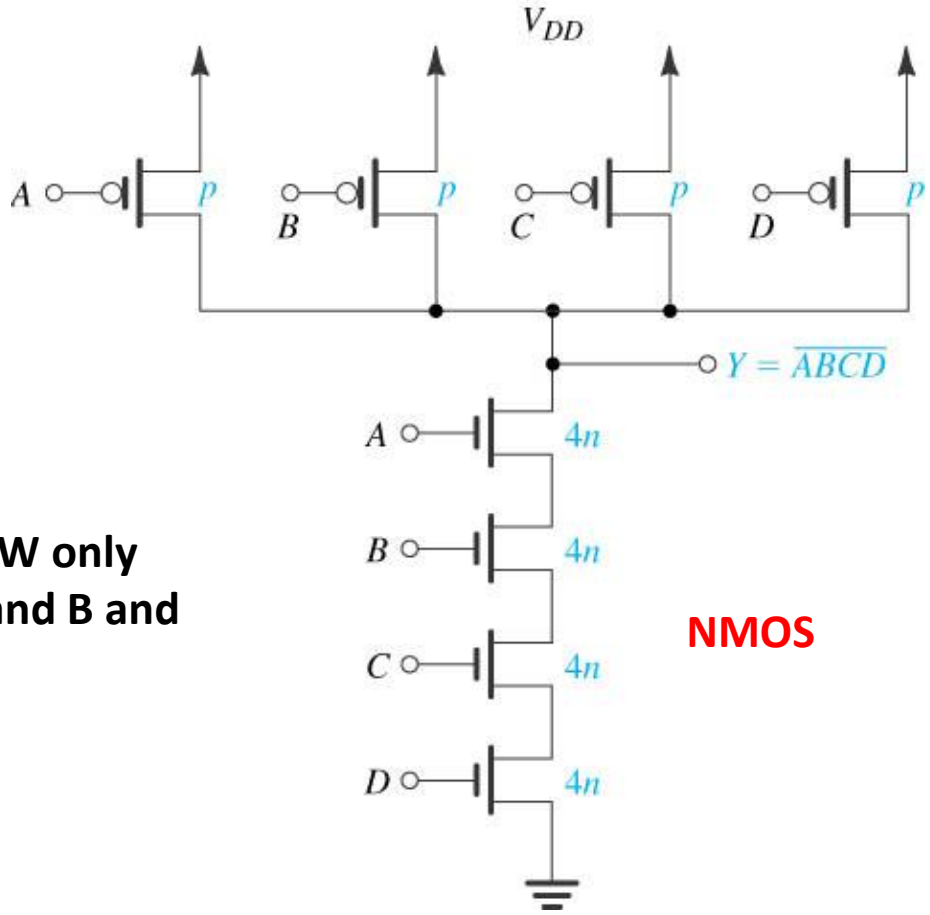
Output follow the input, No inversion

4 input NOR gate implemented using CMOS technology

The output (y) is LOW when either inputs(A OR B OR C OR D) are is high



4 input NAND gate implemented using CMOS technology



PMOS

NMOS

The output (y) is LOW only when all inputs (A, and B and C and D) are High

CMOS NAND and NOR gates