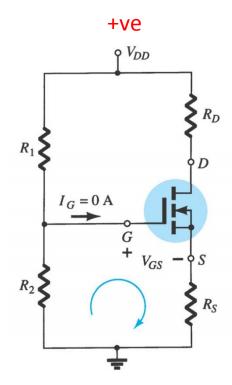
Field Effect Transistors DC biasing

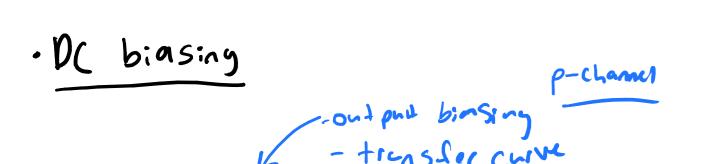
Chapter 7

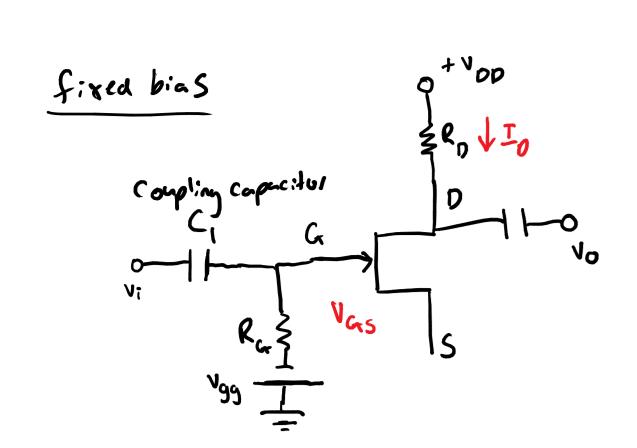
- Fixed Bias configuration
- Self Bias
- Voltage divider bias
- Feedback bias
- Graphical analysis

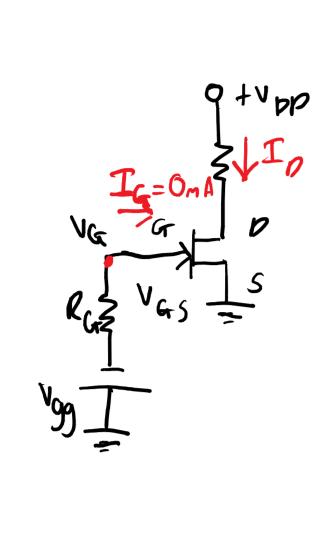
- Transfer curve
- Network equation
- Operating point



Application of DC supply (V_{DD}) to provide the required polarity and level of DC voltages for the transistors to operate in the region of interest







Shockley equation:

$$I_0 = T_{OSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

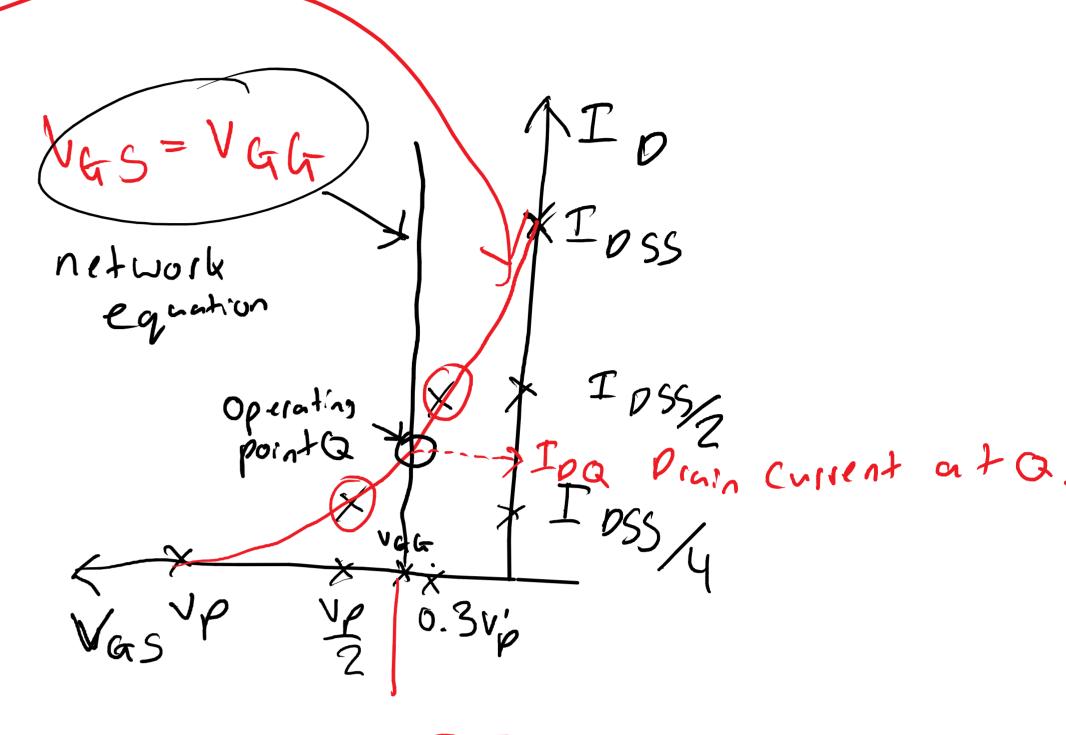
$$V_G = V_{GG} - \frac{1}{G} G_G$$

$$V_G = V_{GG} - V_S$$

$$V_{GS} = V_{GG} - V_S$$

$$V_{GS} = V_{GG} - O$$

$$V_{GS} = V_{GG} - O$$



$$Vpp = FpRp + VpS$$

$$T_p = Vpp - VpS$$

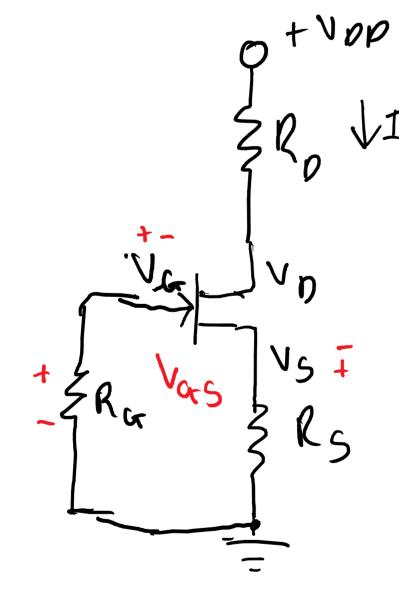
$$R_p$$

$$VpS = Vp - TpRp$$

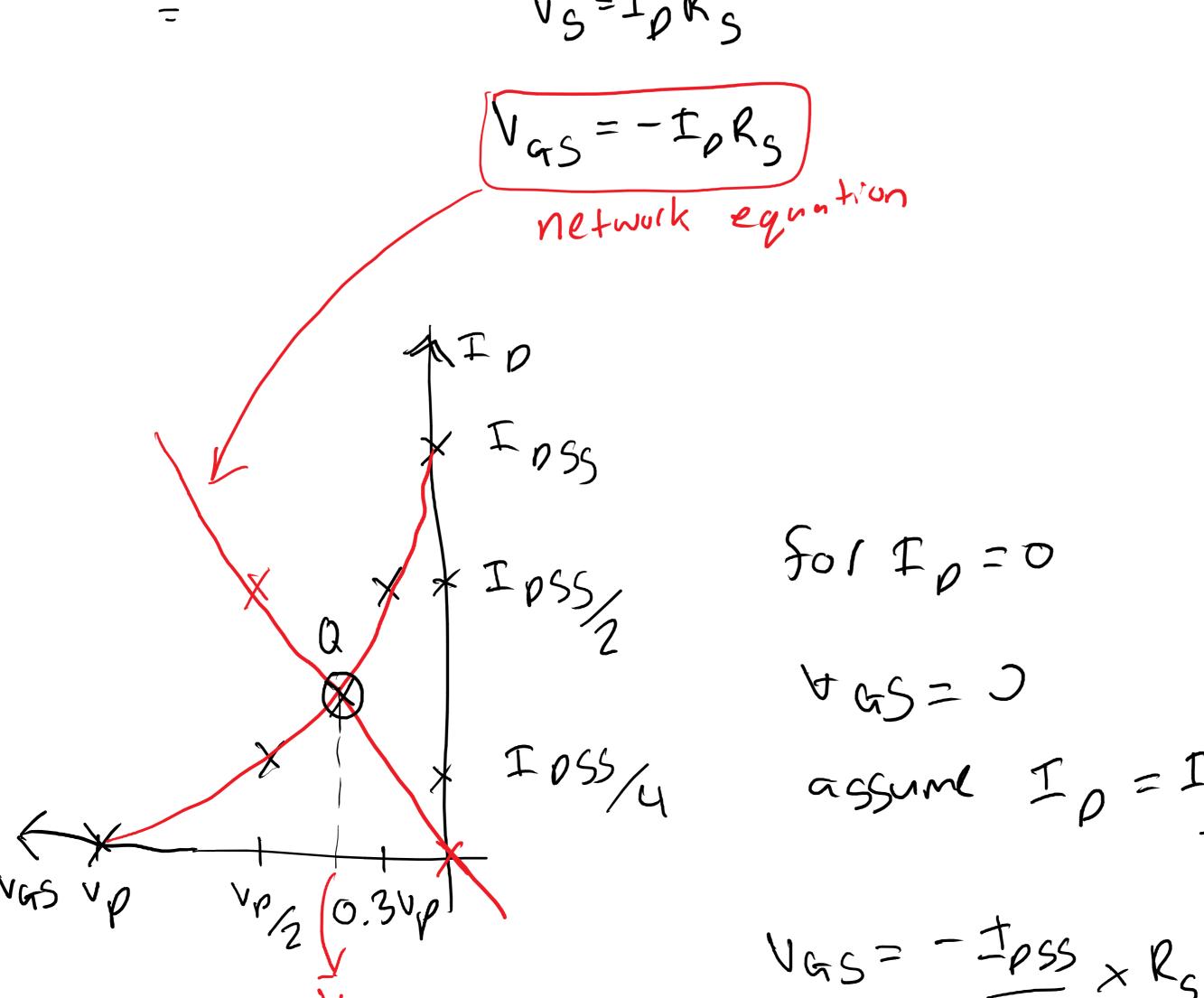
$$VpS = Vp - Vs$$

Self-bias configuration

$$I_p = I_{pss} \left(1 - \frac{V_{qs}}{V_p} \right)^2 T_{ransfer} curve$$



$$VGS = VG - VS$$
 (network eq)
 $VG = 0$, $IG = 0$
 $VGS = 0 - VS$
 $VS = ISRS$
 $IS = ID$
 $VS = IDRS$



FET DC Biasing Circuits Analysis

- I_D is controlled by V_{GS} Voltage Controlled Transistor
- In all dc analysis of FET's circuits

$$I_G = 0$$
 mA, gate current = 0

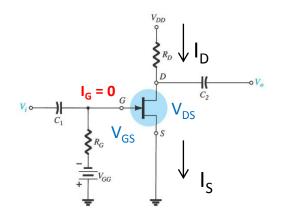
- I_D = I_S Drain Current = Source Current
- Shockley Equation relates input voltage V_{GS} and output current I_D in JFET's and DMOS transistors:

$$I_D = I_{DSS} (1 - \frac{V_{GS}}{V_P})^2$$
(1)

For Enhancement type MOSFET :

$$I_D = K(V_{GS} - V_T)^2$$
(2)

- Equations 1 and 2 are applied for JFET and MOSFET devices, they don't change
 With biasing network configurations.
- It is the network that determine the level of current and voltage associated with the operating point Q.
- DC analysis is the solution of simultaneous equations established by the DEVICE and NETWORK.
- DC analysis can be performed by mathematical or graphical methods.

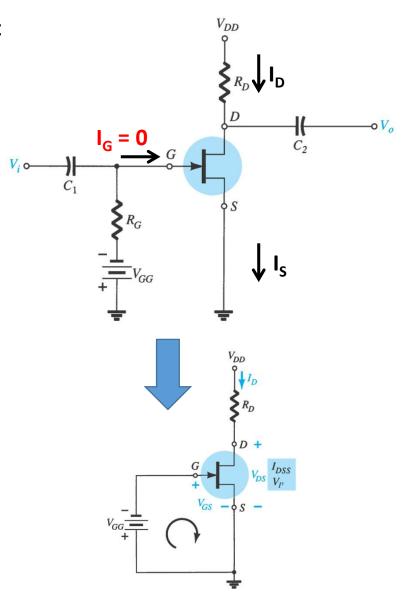


Fixed -bias configuration for JFET's

- R_G is placed to ensure that V_i appears at the input of the FET for ac applications and analysis.
- Coupling capacitors are open circuit for DC analysis and short circuit for ac analysis(and applied signals)

DC analysis and mathematical approach:

- I_G = 0mA (Hence V_{GG} appears at the Gate G)
- $V_{RG} = I_G R_G = 0V$
- -V_{GG}-V_{GS} = 0V (input loop)
- V_{GS} = -V_{GG}(network Equation)
- Since V_{GG} is fixed supply voltage, hence the name Fixed bias configuration.
- Apply Shockley equation: $I_D = I_{DSS} (1 \frac{V_{GS}}{V_p})^2$
- I_{DSS} and V_P are usually obtained from the data sheet, Specified by the manufacturing company.
- V_{GS} is fixed by the V_{GG}(network equation).
- Then I_D can be calculated for the fixed bias circuit using Shockley equation.



JFET Fixed bias DC circuit

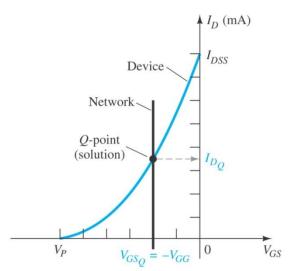
Graphical analysis(plot of Shockley equation)

- 1. Construct the transfer curve using Shockley equation: $I_D = I_{DSS} (1 \frac{V_{GS}}{V_-})^2$
- 2. Find the network equation for the circuit and superimpose it on the transfer curve. $V_{GS} = V_G V_S = V_G$ as $V_S = 0V$ (fixed bias).
- 3. The point where the two curves intersect is the common solution to the two equations and it is called the Q operating point.
- 4. At the Q point, I_{DQ} and V_{GSQ} can be determined, e.g. I_{DQ} = 2.6mA, and V_{GSQ} = -2.6V
- 5. The output loop equations

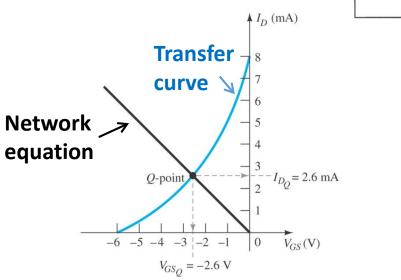
$$V_{DS} = V_{DD} - I_{D}R_{D}$$

$$V_{DS} = V_{D} - V_{S}$$

$$V_{D} = V_{DS} + V_{S} \text{ for this case } V_{S} = 0V$$
Then $V_{D} = V_{DS}$



Fixed Bias



Self Bias

Example

Find V_{GSQ} , I_{DQ} , V_{DS} , V_{G} and V_{S} for the circuit shown using mathematical and graphical method.

Mathematical method:

Network Equation

$$V_{GS} = V_G - V_S = V_G$$
 since $V_S = 0$ (ground)
 $I_G = 0mA$
 $V_{GS} = V_G = -V_{GG} = -2V = V_{GSO}$

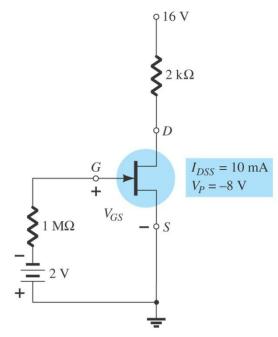
Shockley Equation

$$I_D = I_{DSS} (1 - \frac{V_{GS}}{V_D})^2 = 10 \text{mA} (1 - \frac{-2}{-8})^2 = I_{DQ} = 5.625 \text{mA}$$

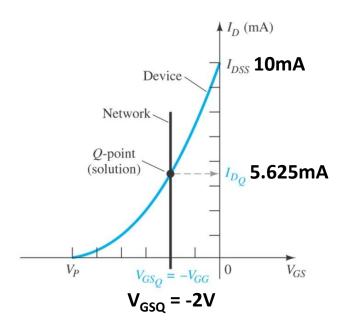
Output loop:

$$V_{DD} = I_D R_D + V_{DS}$$

 $V_{DS} = V_D - V_S = (V_{DD} - I_D R_D) - 0V$
 $V_{DS} = 16 - 5.625 \times 10^{-3} \times 2 \cdot 10^3 = 4.75V$
 $V_D = V_{DS} + V_S = 4.75 + 0 = 4.75 V$
 $V_G = V_{GS} + V_S = -2V + 0 = -2V$
 $V_S = 0V$ ground potential, common source configurations.



JFET fixed bias circuit



Graphical method

$$I_D = I_{DSS} (1 - \frac{V_{GS}}{V_P})^2$$

For $V_{GS} = 0V$, $I_D = I_{DSS} = 10 \text{mA}$
For $V_{GS} = V_P$, $I_D = 0 \text{mA}$
For $V_{GS} = \frac{1}{2} V_P = -4V$, $I_D = I_{DSS} / 4 = 2.5 \text{ mA}$
For $I_D = I_{DSS} / 2 = 5 \text{mA}$
 $V_{GS} = 0.3 V_P = 0.3 x - 8 V = -2.4 V$

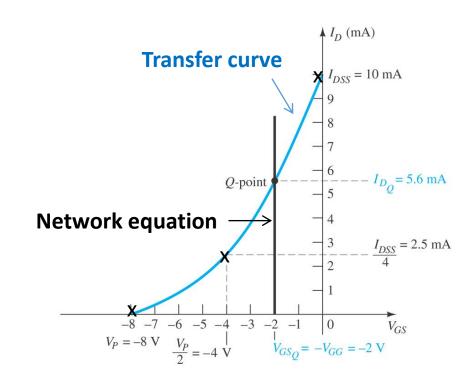
Network Equation:

$$V_{GS} = V_G - V_S = V_G - 0V$$

 $V_G = V_{GG} = -2V = V_{GSQ}$ (Fixed at -2V)

Q point from the intersection of the network equation(black line) and the transfer curve(blue)

$$V_{GSQ} = -2V$$
 and $I_{DQ} = 5.6$ mA



Construction of Transfer Curve

Self-Bias Configuration

One DC supply V_{GS} is determined by R_S

DC analysis:

 $I_G = 0mA$

 R_G can be replaced with short circuit no current flow in R_G , hence the voltage is the same on either end of R_G (ground).

$$I_D = I_S$$

$$V_{RS} = I_D R_S = V_S$$

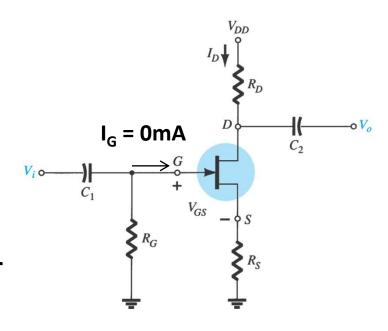
$$V_{GS} = V_G - V_S \quad \text{but } V_G = 0V$$

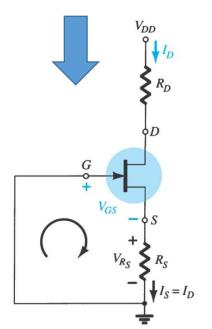
$$V_{GS} = -V_S = -I_D R_S \quad \text{(Network equation)}$$

$$I_D = I_{DSS} (1 - \frac{V_{GS}}{V_P})^2$$
 (Transfer curve)

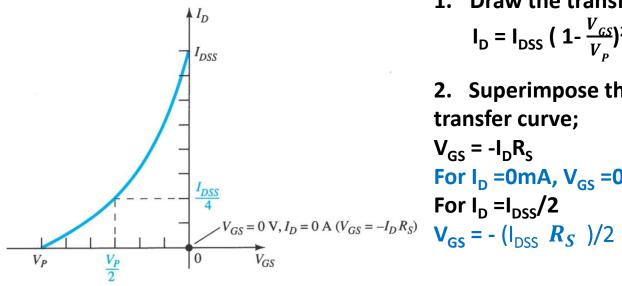
Solve Shockley equation to find I_{DQ} by substituting

$$V_{GS} = -I_D R_S$$
 $I_{DQ} = I_{DSS} (1 - \frac{-I_{DQ} R_S}{V_P})^2$





Graphical analysis



- **Draw the transfer curve using Shockley equation** $I_{D} = I_{DSS} (1 - \frac{V_{GS}}{V_{-}})^{2}$
- 2. Superimpose the network equation on the transfer curve;

$$V_{GS} = -I_D R_S$$

For $I_D = 0$ mA, $V_{GS} = 0$ V 1st point
For $I_D = I_{DSS}/2$
 $V_{GS} = -(I_{DSS} R_S)/2$ 2nd point

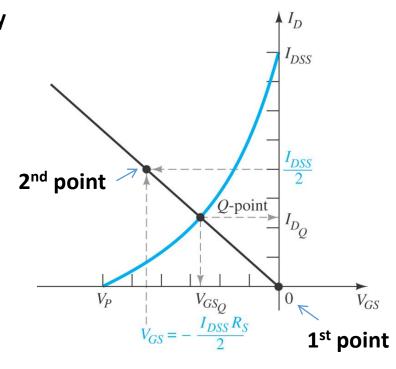
- 3. From the intersection of the straight line defined by the network and transfer curve defined by Shockley equation, the operating point Q is established: I_{DO} and V_{GSO} can be found.
- 4. From the output loop

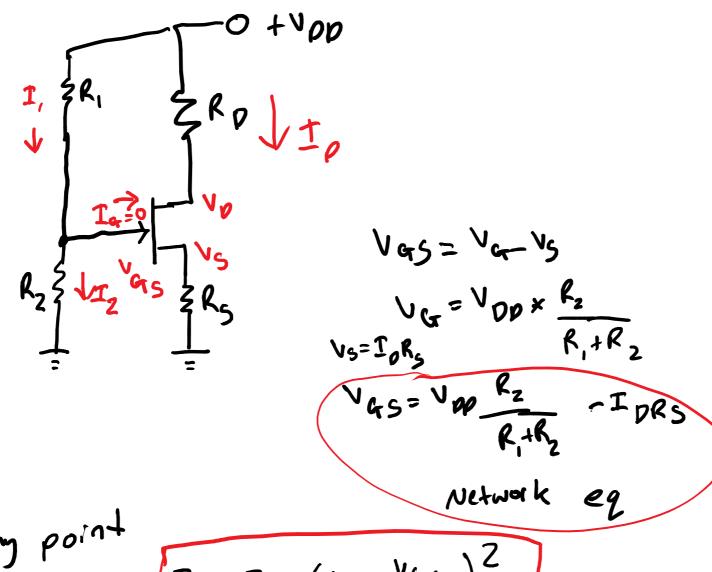
$$V_{DD} = V_{RD} + V_{DS} + V_{RS}$$

 $V_{DS} = V_{DD} - V_{RD} - V_{RS} = V_{DD} - I_D R_D - I_D R_S$ ($I_D = I_S$)

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_S = I_D R_S$$
, $V_G = 0V$
 $V_D = V_{DS} + V_S = V_{DD} - V_{RD}$





· Operating point

· Operating point

Shockley equation
$$Io = I_{oss}(1 - \frac{v_{us}}{vp})^2$$

Transfer Curve

Ip=Is

$$V_{00} = T_0 R_p + V_{pS} + T_0 R_S$$

$$V_{00} = T_0 (R_0 + R_S) + V_{0S}$$

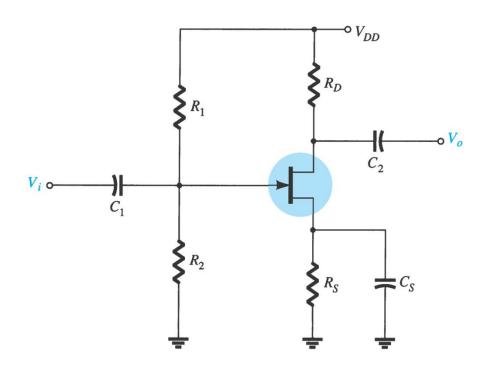
$$I_{D} = \frac{V_{00} - V_{05}}{R_{0} + R_{5}}$$

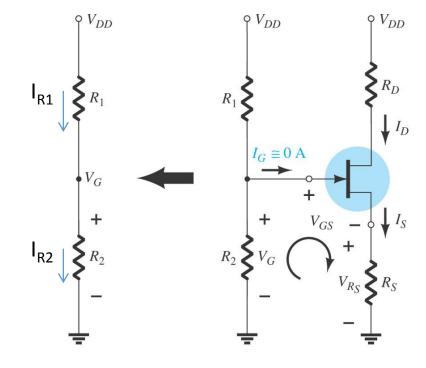
$$V_{0S} = V_{0} - I_{0}(R_{0} + R_{S})$$
 $V_{0S} = V_{0} - V_{S}$
 $V_{0} = V_{00} - I_{0}R_{0}$
 $V_{S} = I_{0}R_{S}$
 $V_{0S} = (V_{00} - I_{0}R_{0})$
 $V_{0S} = (V_{00} - I_{0}R_{0})$
 $V_{0S} = V_{0S} + I_{0}R_{0}$

$$T_{1} = T_{2} = \frac{V\rho\rho}{R_{1} + R_{2}}$$

$$T_{2} \downarrow R_{2}$$

Voltage Divider Bias





$$I_G = 0mA$$

 $I_{R1} = I_{R2}$

$$V_{G} = \frac{V_{DD} R_{2}}{R_{2} + R_{1}}$$

Voltage Divider Rule

V_G is positive

$$V_{GS} = V_G - V_S$$

 $V_{GS} = V_G - I_D R_S$

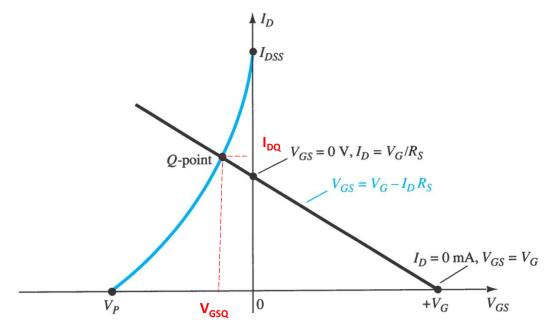
Network equation

DC equivalent circuit, NO need to Thevenin's....

Transfer Curve

The operating point I_{DQ} and V_{GSQ} can be found by superimposing the *network equation* on the *transfer curve*.

- 1. $V_{GS} = V_G I_D R_S$ Network Equation
- 2. For $I_D = 0$, $V_{GS} = V_G$ (1st point)
- 3. For $V_{GS} = 0V$, $I_D = V_G/R_S$ (2nd point)
- 4. I_{DQ} and V_{GSQ} can be found from the intersection with the transfer curve at the Q point.



Network equation and transfer curve

Output Loop:

$$V_{DS} = V_{DD} - I_{D}(R_{D} + R_{S})$$

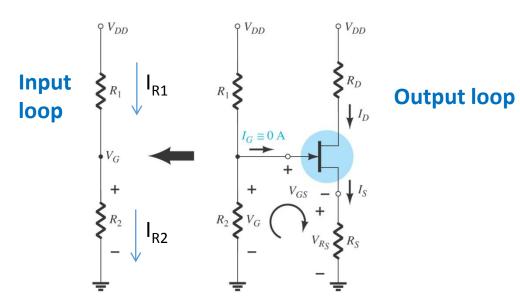
$$V_{D} = V_{DD} - I_{D}R_{D}$$

$$V_{S} = I_{D}R_{S}$$

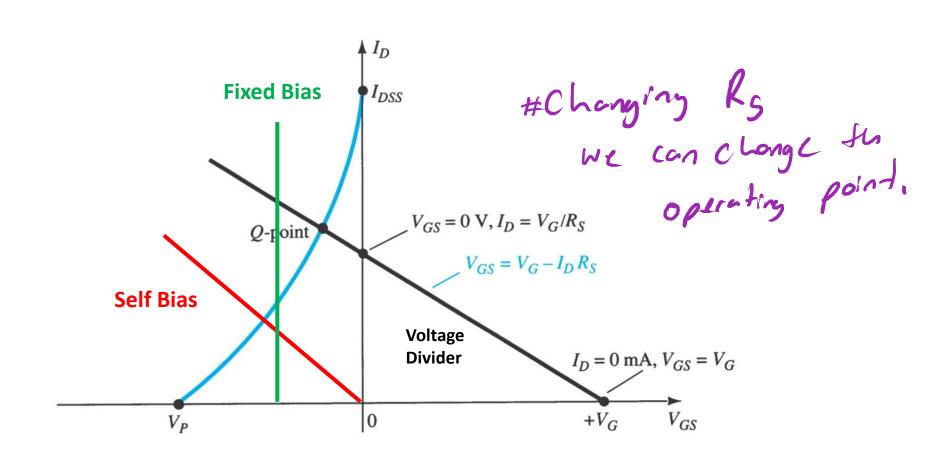
Input loop:

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

 $I_G = 0mA$



Network equation and biasing configuration



Depletion type MOSFET biasing circuits

Same analysis as JFET

DMOSFET, n channel permit operating point
with positive V_{GS} and I_D could be > I_{DSS}

DC analysis:

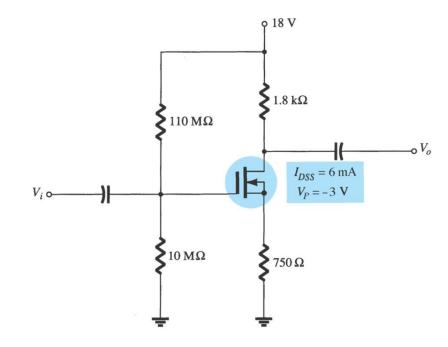
1. Draw the transfer curve using Shockley equation

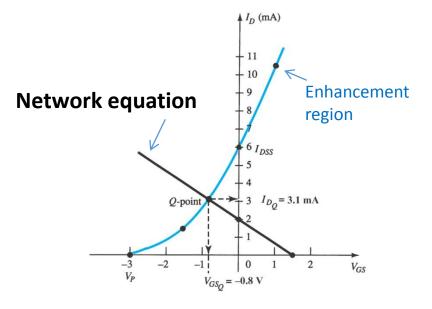
For
$$V_{GS} = \frac{1}{2} V_{P} = -1.5V$$

 $I_{D} = I_{DSS}/4 = 1.5 \text{mA}$
 $I_{D} = 0$, for $V_{GS} = V_{P} = -3V$
 $I_{D} = I_{DSS}/2$, $V_{GS} = 0.3V_{P} = -0.9V$
 $I_{D} = I_{DSS} = 6 \text{mA}$ at $V_{GS} = 0.5V$

For
$$V_{GS} = +1V$$
, (enhancement region)
 $I_D = I_{DSS} (1 - \frac{V_{GS}}{V_p})^2$

$$I_D = 6mA(1 - \frac{+1V}{-3V})^2 = 10.67mA$$





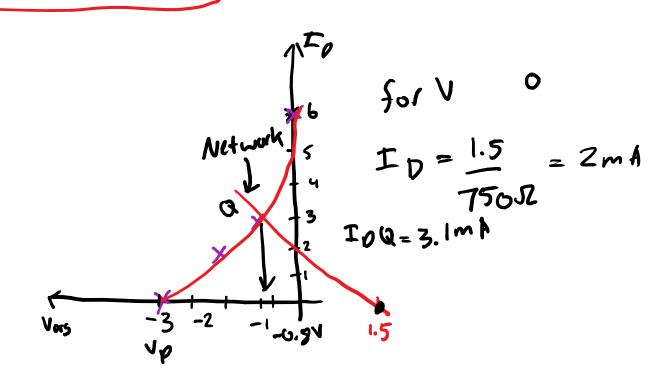
$$V_{GS} = V_{GS} - V_{S}$$

$$V_{G} = V_{DD} \frac{R_{Z}}{R_{1} + R_{2}} = 19V \frac{10M}{10M + 110M}$$

$$V_{G} = + 1.5V$$

$$V_{G} = I_{D}R_{S}$$

$$V_{GS} = 1.5 - I_{D}R_{S}$$



Network equation

2. Draw the network equation

$$V_{GS} = V_G - V_S = V_G - I_D R_S$$

$$V_G = V_{DD} \frac{R_2}{R_2 + R_1} = \frac{18 \times 10M}{110M + 10M} = 1.5V$$

$$V_{GS} = 1.5 - I_{D} \times 750\Omega$$

Setting I_D =0, V_{GS} = V_G = 1.5V Setting V_{GS} = 0, I_D = V_G/R_S = 1.5V/ 750 Ω = 2 mA The intersection of the network equation with transfer curve gives the operating point:

$$I_{DQ} = 3.1 \text{mA}, V_{GSQ} = 0.8 \text{V}$$

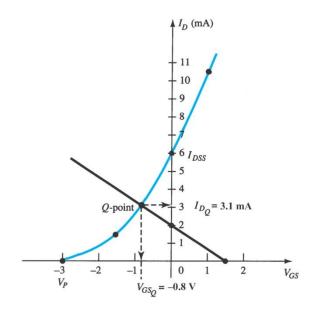
From the drain source output loop:

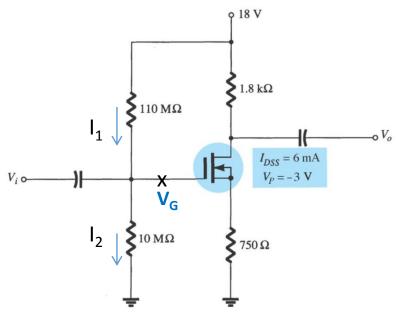
$$V_{DS} = V_{DD} - I_{D}(R_{D} + R_{S})$$

 $V_{DS} = 18 - 3.1 \text{ mA}(1.8 \text{k} + 750 \Omega) = 10.1 \text{ V}$

From the input loop:

$$I_1 = I_2 = \frac{18V}{110M + 10M} = 0.15\mu A$$





Enhancement type MOS biasing circuits

EMOSFET's have different transfer curve compared to JFET's and DMOSFET's

Shockley equation does not apply for EMOS.

$$I_D = 0 \text{ mA for } V_{GS} < V_T$$

For $V_{GS} > V_T$ $I_D = k(V_{GS} - V_T)^2$

From the output characteristics

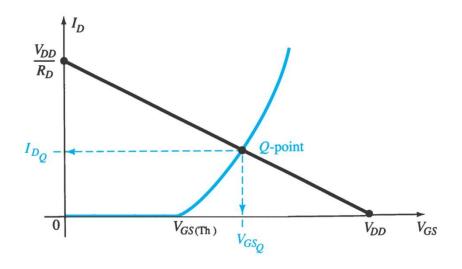
$$V_{DSsat} = (V_{GS}-V_{T})$$

 $V_{DS} > (V_{GS}-V_{T})$ Saturation region
 $V_{DS} < (V_{GS}-V_{T})$ Ohmic Region

To draw the transfer curve V_T is provided from the data sheet, also given is I_D (on) and V_{GS} (on)

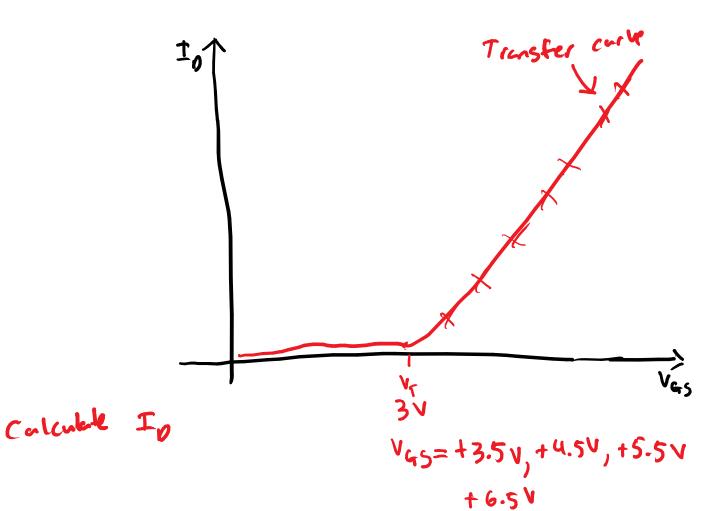
Then k can be calculated from:

$$K = \frac{I_{D(on)}}{[V_{GS(ON)} - V_T]^2}$$



Transfer curve(blue), load line(black) and Q point for EMOS

EMDSFET



VG=VD (no current flowing in RG, IG=0)

$$V_{00} = I_{0}R_{0} + V_{0S}$$

$$V_{0S} = V_{0} - V_{S}$$

$$V_{00} = \underline{T}_{0}R_{0} + V_{GS}, \quad V_{GS} = V_{00} - \underline{I}_{0}R_{0}$$

$$Ne + work = quarken$$

$$V_{GS} = +3.5V_{1} + 4.5V \quad \underline{T}_{0} = 0 \quad V_{0S} = V_{GS}$$

$$V_{65} = +3.5V_{1} + 4.5V_{10} = 0$$
 $V_{65} = 0$ $V_{65} = 0$, $I_{10} = \frac{V_{10}}{R_{10}}$ Calculate I_{10}

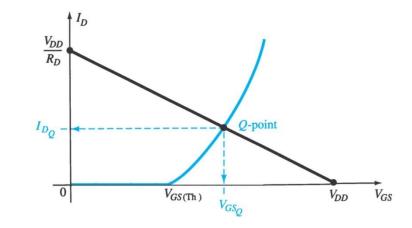
Feedback Bias for EMOS

$$I_G = 0mA$$

$$V_{RG} = 0V \quad (= I_G \cdot R_G)$$

$$V_D = V_G$$

$$V_{DS} = V_{GS} \quad (\text{no current flowing in the 10M resistor})$$



Output loop:

$$V_{DS} = V_{DD} - I_D R_D$$

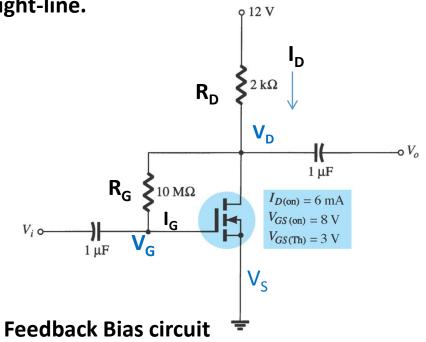
 $V_{GS} = V_{DD} - I_D R_D$ (network equation)

i.e. the relationship between V_{GS} and I_D is a straight-line.

Now for
$$I_D = 0$$

 $V_{GS} = V_{DD}$
For $V_{GS} = 0V$

$$I_D = \frac{V_{DD}}{R_D}$$



Voltage Divider Bias

Input loop:

I_G = 0mA gate is isolated

$$V_{G} = V_{DD} \frac{R_2}{R_2 + R_1}$$

$$V_{GS} = V_G - V_S$$

 $V_{GS} = V_G - I_D R_S$

Network equation

$$I_D = k(V_{GS} - V_T)^2$$

Transfer curve

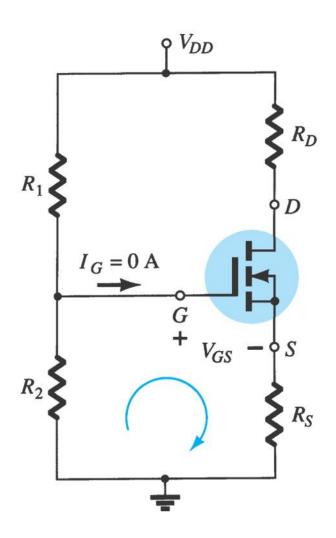
Substitute for V_{GSQ} from network equation into the transfer curve equation to find I_{DQ}

$$I_{DQ} = k\{ (V_G - I_{DQ} R_S) - V_T \}^2$$

Output loop:

$$V_{DD} - V_{RD} - V_{DS} - V_{RS} = 0$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$



EMOSFET biasing circuit