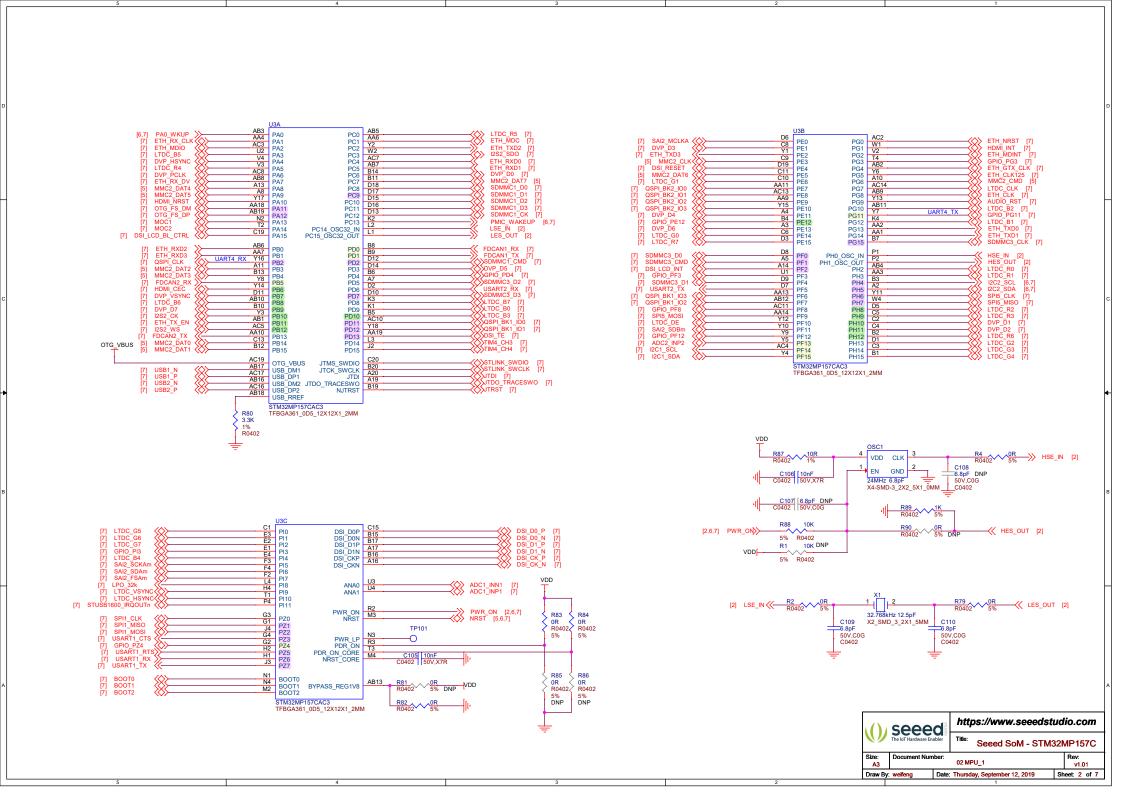
Schematic: Seeed SoM - STM32MP157C

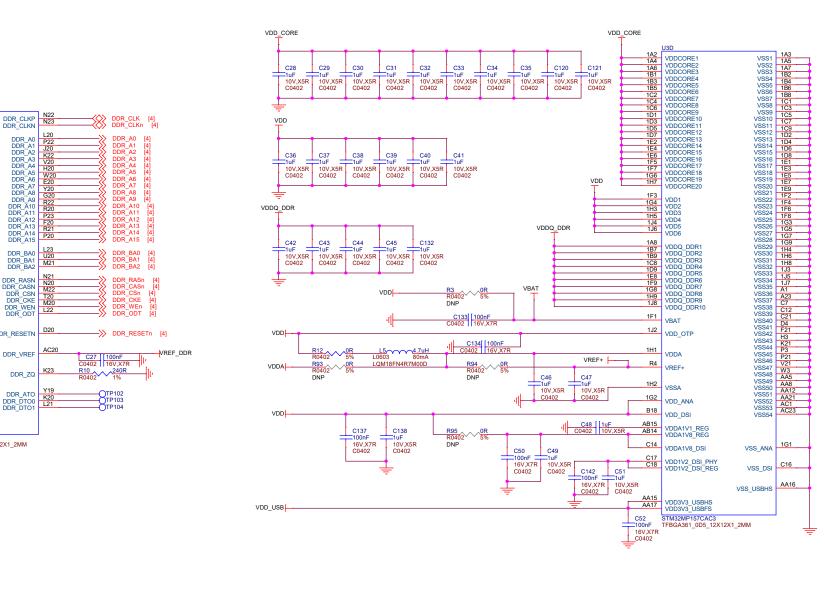
Revision History

SHEET	SHEET NAME
01	Title/Revision History
02	MPU_1
03	MPU_2
04	DDR3
05	eMMC
06	PMU
07	PINOUT/LED

DATE	REVISION	DESCRIPTION	
2019/05/21	Seeed SoM - STM32MP157C_v1.0_SCH_190521	Initial Release	
2019/09/04	Seeed SoM - STM32MP157C_v1.01_SCH_190904		
2019/12/13	Seeed SoM - STM32MP157C v1.01 SCH 191213	Change R5,R6 from 1k to 2k	







[4] DDR_D10 [4] DDR_D11 [4] DDR_D12 [4] DDR_D13 [4] DDR_D15 DDR_DQS1 DDR_DQSN1 W21 W23 T23 DDR_DQ10 DDR_DQ11 DDR_DQ12 DDR_DQ13 DDR_DQ14 DDR_DQ15 W22 Y21 U22 U23 DDR_BA0 DDR_BA1 DDR_BA2 DDR_DQS1P DDR_DQS1N DDR_DQM1 V22 DDR DQM1 B22 DDR_DOM1

X D22 DDR DO16

X D23 DDR DO16

X D23 DDR DO18

X D21 DDR DO19

X D21 DDR DO20

X D22 DDR DO20

X D22 DDR DO22

X D22 DDR DO22

X D23 DDR DO25

X D25 DDR DO25

X D27 DDR DO25

X D27 DDR DOS2P

X D27 DDR DOS2P DDR_CSN DDR_CKE M20
DDR_WEN L22
DDR_ODT DDR_RESETN XY23 Y22 AB21 AB20 DDR VREF DDR DQ24 DDR_DQ24
DDR_DQ25
DDR_DQ26
DDR_DQ27
DDR_DQ28
DDR_DQ29
DDR_DQ30
DDR_DQ31 DDR_ZQ AC22 AC21 AA23 AA22 AB22 AB23 AA20 DDR_ATO DDR_DTO0 DDR_DTO1 DDR_DQS3P DDR_DQS3N DDR_DQM3 STM32MP157CAC3 TFBGA361_0D5_12X12X1_2MM

DDR_DQ0
DDR_DQ1
DDR_DQ1
DDR_DQ2
DDR_DQ3
DDR_DQ4
DDR_DQ5
DDR_DQ6
DDR_DQ7
DDR_DQ7
DDR_DQ70
DDR_DQ80P

DDR_DQS0N DDR_DQM0

DDR_DQ8 DDR_DQ9 DDR_DQ10

E22

J21 J22 H22 G21

G22 G23 H23

DDR_D0 DDR_D1

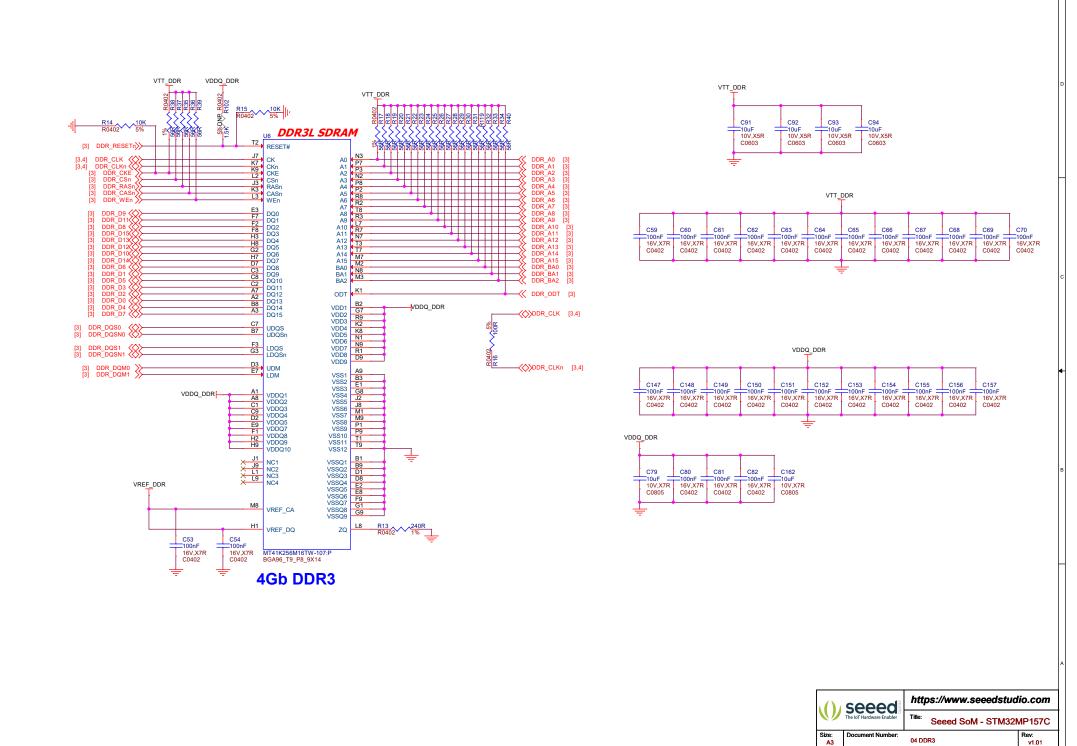
DDR_D2 DDR_D3

DDR_D8

DDR_D9 <

[4] DDR_D3 [4] DDR_D4 [4] DDR_D5 [4] DDR_D6 [4] DDR_D7 DDR_DQS0 DDR_DQSN0

https://www.seeedstudio.com seeed Seeed SoM - STM32MP157C Size: 03 MPU_2 v1.01 Sheet: 3 of 7 Date: Thursday, September 12, 2019 Draw By: weifeng



Sheet: 4 of 7

Date: Thursday, September 12, 2019

