Table 1 CMOS Process and Derived Parameters

	0.8 μm CMOS		0.5 μm CMOS		0.25 μm CMOS		0.18 μm CMOS		0.13 μm CMOS	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
t_{ox} (nm) *	15	15	9	9	6	6	4	4	2.7	2.7
V_{T0} (V) *	0.7	-0.7	0.7	-0.8	0.5	-0.6	0.5	-0.5	0.4	-0.4
μ_o (cm^2/Vs) *	600	220	500	180	460	160	300	100	300	100
C_{ox} ($fF/\mu m^2$) **	2.3	2.3	3.8	3.8	5.8	5.8	8.8	8.8	13	13
k′ ($\mu A/V^2$) **	138	51	190	68	267	93	264	88	390	130
V_{DD} (V) ***	5	5	3.3	3.3	2.5	2.5	1.8	1.8	1.3	1.3

* Data adapted from A.S. Sedra and K.C. Smith, Microelectronics, 6th Ed., 2011, p 530.

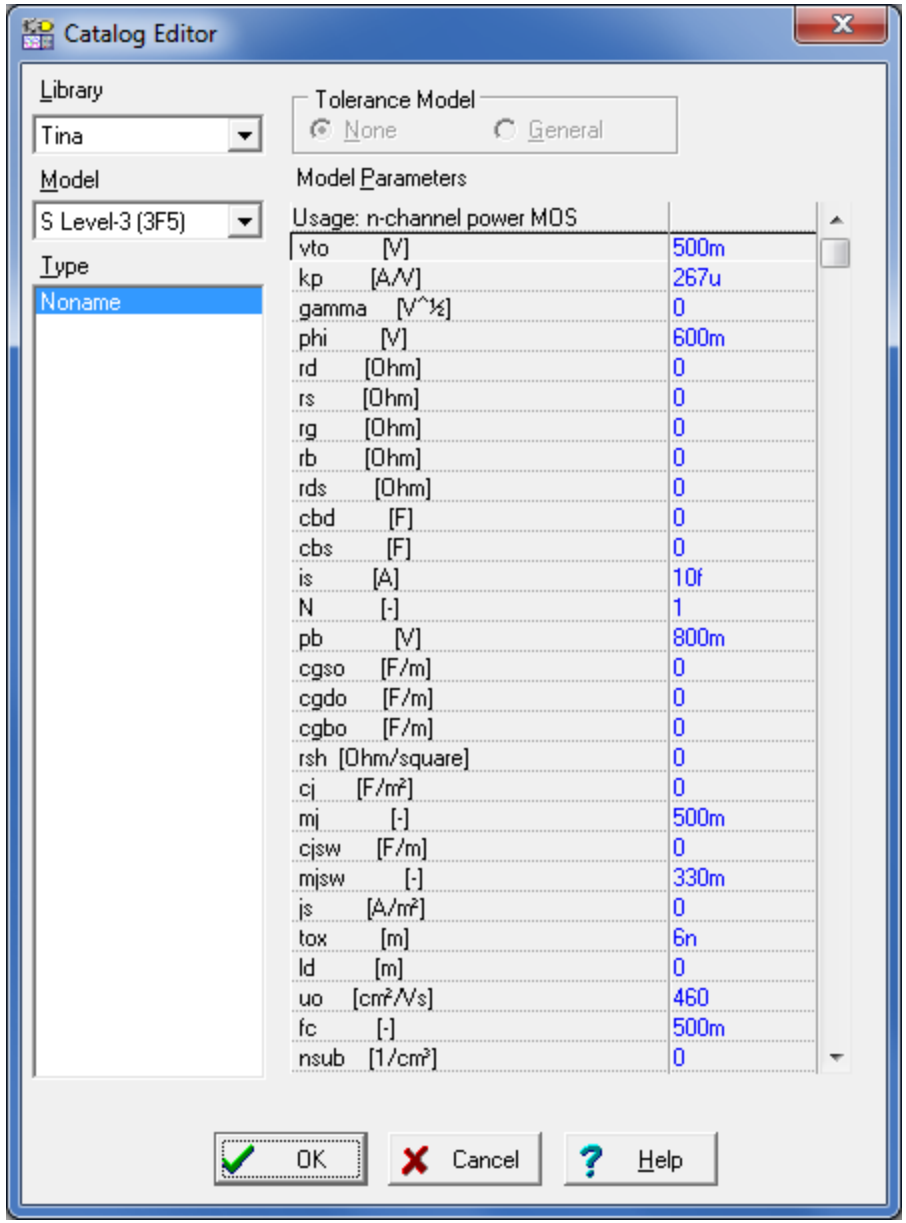
** Derived parameters: $C_{ox} = \varepsilon(SiO_2)/t_{ox}$ $k' = \mu_o C_{ox}$

*** Supply voltage limited by MOSFET breakdown.

$\varepsilon(SiO_2) = 3.97\varepsilon_o = 35$ pF/m

$\varepsilon(Si) = 11.7\varepsilon_o = 104$ pF/m

Table 2 TINA Enhancement Mode MOSFET Parameter Settings for 0.25 µm Process Minimum Settings (without junction and overlap capacitances)



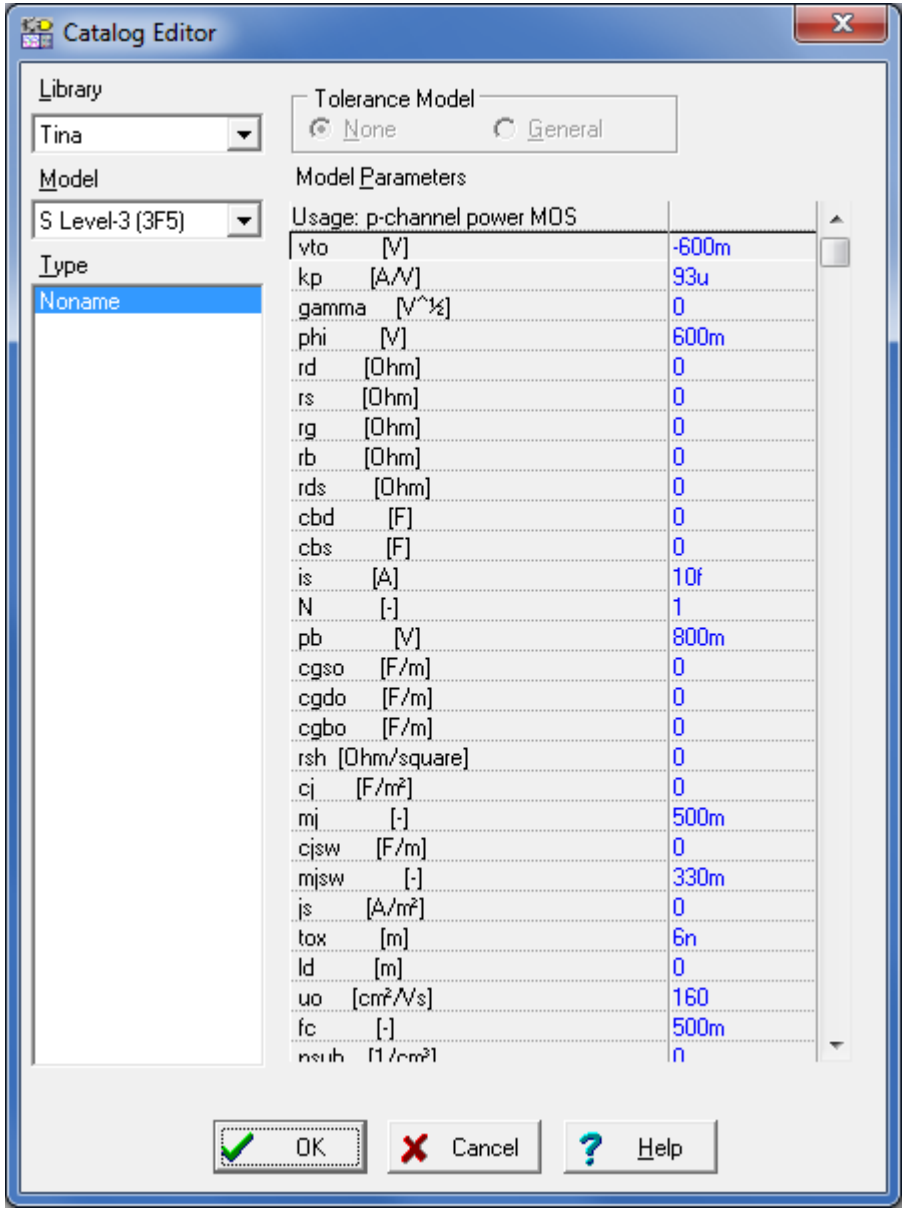


Table 3 TINA Enhancement Mode MOSFET Parameter Settings for 0.25 µm Process Comprehensive Settings