CPE301 – SPRING 2019

Design Assignment 1

Student Name: Cody Jones

Student #: 5002863328

Student Email: Jonesc30@unlv.nevada.edu

Primary Github address: https://github.com/Jonesc30/Submission

Directory: Submission

Submit the following for all Labs:

1. In the document, for each task submit the modified or included code (only) with highlights and justifications of the modifications. Also, include the comments.
2. Use the previously create a Github repository with a random name (no CPE/301, Lastname, Firstname). Place all labs under the root folder ESD301/DA, sub-folder named LABXX, with one document and one video link file for each lab, place modified asm/c files named as LabXX-TYY.asm/c.
3. If multiple asm/c files or other libraries are used, create a folder LabXX-TYY and place these files inside the folder.
4. The folder should have a) Word document (see template), b) source code file(s) and other include files, c) text file with youtube video links (see template).

1. **COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS**
2. **INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1/A**

.org 0 ;burn into ROM starting at 0

ldi R25, 0xFF ;load upper 8 bits of multiplicand

ldi R24, 0xFF ;load lower 8 bits of multiplicand

ldi R23, 0xFF ;load upper 8 bits of multiplier

ldi R22, 0xFF ;load lower 8 bits of multiplier

ldi R17, 0 ;initialize to zero

ldi R18, 0 ;initialize to zero

ldi R19, 0 ;initialize to zero

ldi R20, 0 ;initialize to zero

ldi R21, 0 ;used to carry into R20

L1:

add R17, R24 ;add lower 8 bits

adc R18, R25 ;add upper 9 bits

adc R19, R20 ;add carry

dec R23 ; decrement counter of upper 8 bits of multiplier

brne L1 ; loops while counter is greater than 0

L2:

add R18, R24 ;add lower 8 bits

adc R19, R25 ;add upper 9 bits

adc R20, R21 ;add carry

dec R22 ; decrement counter of lower 8 bits of multiplier

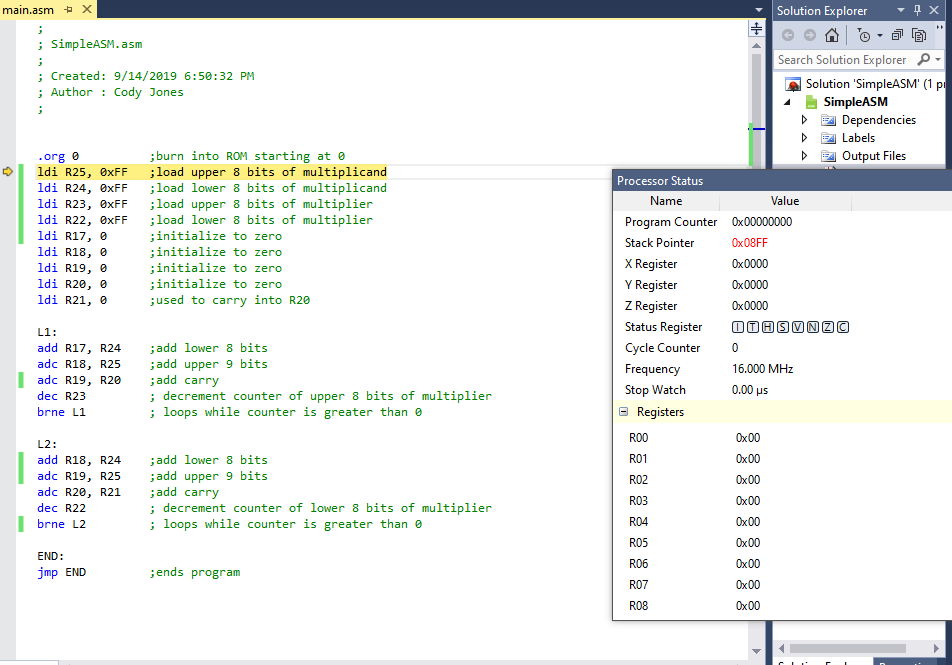
brne L2 ; loops while counter is greater than 0

END:

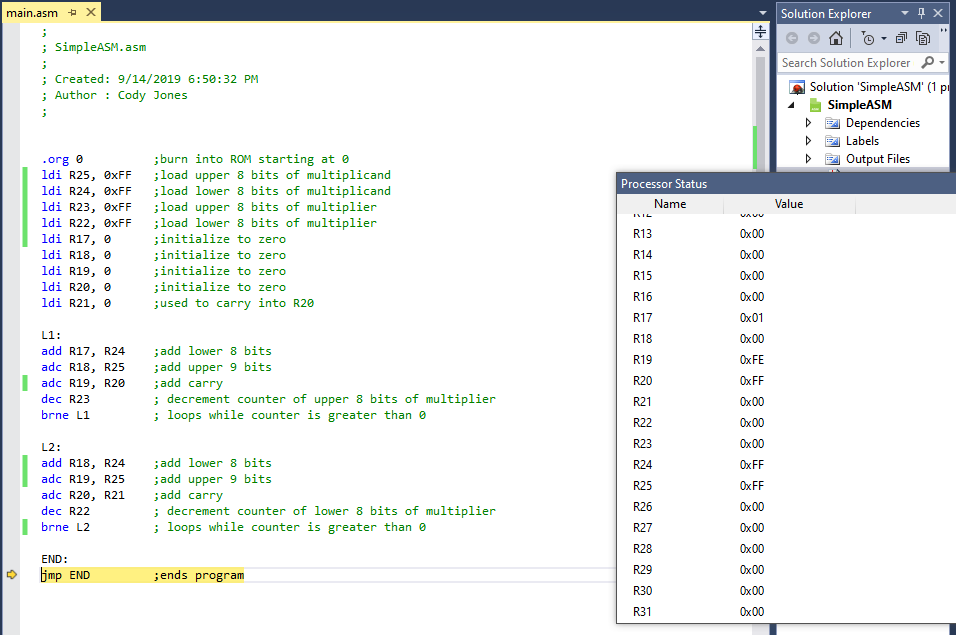
jmp END ;ends program

1. **DEVELOPED MODIFIED CODE OF TASK 2/A from TASK 1/A**
2. **SCHEMATICS**
3. **SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)**

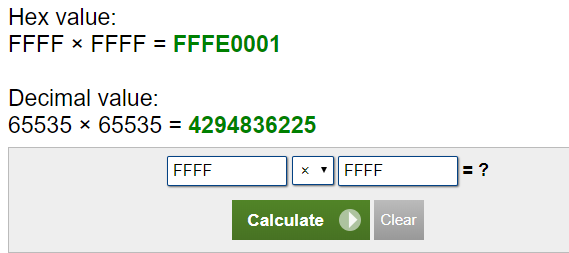
Atmel before running:



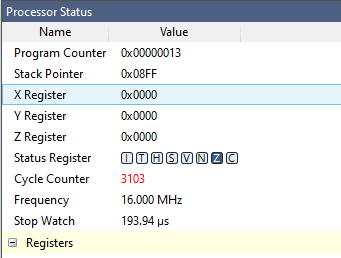
Atmel after running:



Higher level code/calculator verification:



Time that the simulation took at 16MHz and 3103 cycles is 193.94us



1. **SCREENSHOT OF EACH DEMO (BOARD SETUP)**
2. **VIDEO LINKS OF EACH DEMO**
3. **GITHUB LINK OF THIS DA**

<https://github.com/Jonesc30/Submission/tree/master/DesignAssignments/DA1A>

**Student Academic Misconduct Policy**

<http://studentconduct.unlv.edu/misconduct/policy.html>

“This assignment submission is my own, original work”.

Cody Jones