CPE301 – SPRING 2019

Design Assignment 1

Student Name: Cody Jones

Student #: 5002863328

Student Email: Jonesc30@unlv.nevada.edu

Primary Github address: https://github.com/Jonesc30/Submission

Directory: Submission

Submit the following for all Labs:

1. In the document, for each task submit the modified or included code (only) with highlights and justifications of the modifications. Also, include the comments.
2. Use the previously create a Github repository with a random name (no CPE/301, Lastname, Firstname). Place all labs under the root folder ESD301/DA, sub-folder named LABXX, with one document and one video link file for each lab, place modified asm/c files named as LabXX-TYY.asm/c.
3. If multiple asm/c files or other libraries are used, create a folder LabXX-TYY and place these files inside the folder.
4. The folder should have a) Word document (see template), b) source code file(s) and other include files, c) text file with youtube video links (see template).

1. **COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS**

List of Components used

Block diagram with pins used in the Atmega328P

1. **INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1/A**

.org 0 ; location for reset

jmp MAIN

.org 0x02 ; location for external interrupt INT0

jmp EX0\_ISR

MAIN:

ldi R20, HIGH(RAMEND) ; initialize stack

out SPH, R20

ldi R20, LOW(RAMEND)

out SPL, R20

ldi R20, 2 ; make INT0 falling edge triggered

sts EICRA, R20

sbi DDRB, 3 ; set PORTB.3 as output

sbi PORTB, 3 ; set LED off

sbi PORTD, 3 ; turn on pull-up

cbi DDRC, 3 ; set PORTC.3 as input

sbi PORTC, 3 ; enable pull up

ldi R20, 1<<INT0 ; enable INT0

out EIMSK, R20

sei ; enable interrupts

WHILE:

cbi PORTB, 3 ; set LED on

; Delay 4 000 000 cycles

; 250ms at 16.0 MHz

ldi r18, 21

ldi r19, 75

ldi r20, 191

L1: dec r20

brne L1

dec r19

brne L1

dec r18

brne L1

nop

sbi PORTB, 3 ; set LED off

; Delay 6 000 000 cycles

; 375ms at 16.0 MHz

ldi r18, 31

ldi r19, 113

ldi r20, 31

L2: dec r20

brne L2

dec r19

brne L2

dec r18

brne L2

nop

jmp WHILE ; wait for interrupt

EX0\_ISR:

cbi PORTB, 3

; Delay 21 328 000 cycles

; 1s 333ms at 16.0 MHz

ldi r18, 109

ldi r19, 51

ldi r20, 106

L1: dec r20

brne L1

dec r19

brne L1

dec r18

brne L1

reti ; return from interrupt

#define *F\_CPU* 16000000UL

#include <avr/io.h>

#include <avr/interrupt.h>

#include <util/delay.h>

int main(void)

{

DDRB = (1<<3); // set PORTB.3 for output

PORTB = (1<<3); // set LED low

PORTD = (1<<2); //pull-up activated

EIMSK = (1<<INT0); // enable external interrupt 0

EICRA = 0x2; // make INT0 falling edge triggered

sei (); // enable interrupts

while (1)

{

*\_delay\_ms*(250); // delay for 40% DC

PORTB &= ~(1<<3); // set LED on

*\_delay\_ms*(375); // delay for remaining 60%

PORTB |= (1<<3); // set LED off

}

}

ISR (INT0\_vect) { // ISR for external interrupt INT0

PORTB &= ~(1<<3); // turns on PORTB.3 (LED)

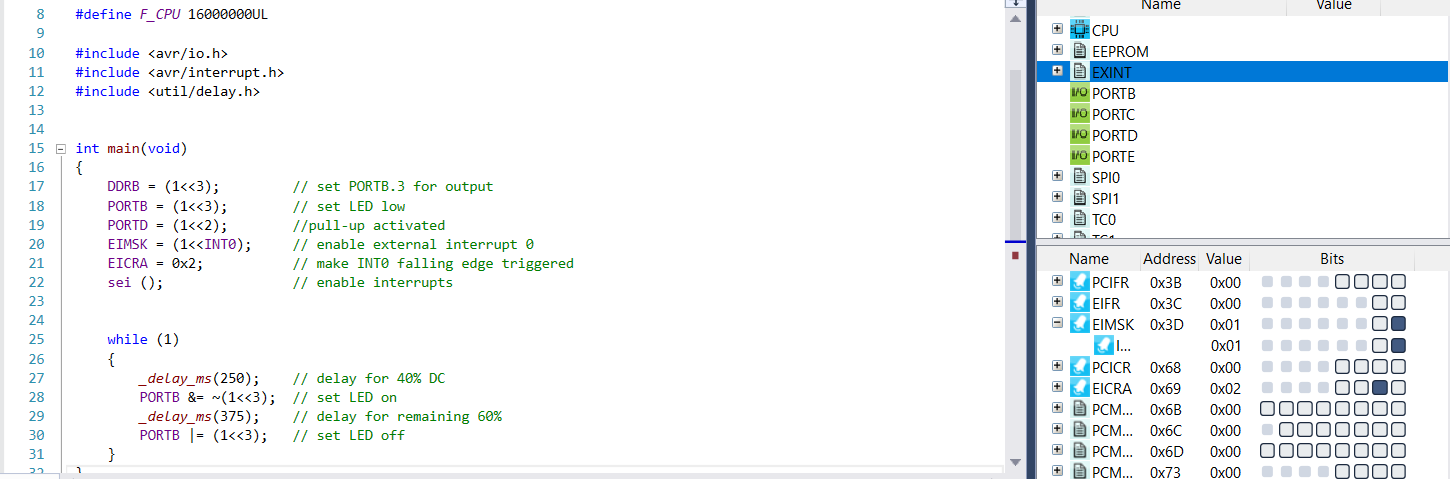
*\_delay\_ms*(1333); // delay for 1.33 sec

}

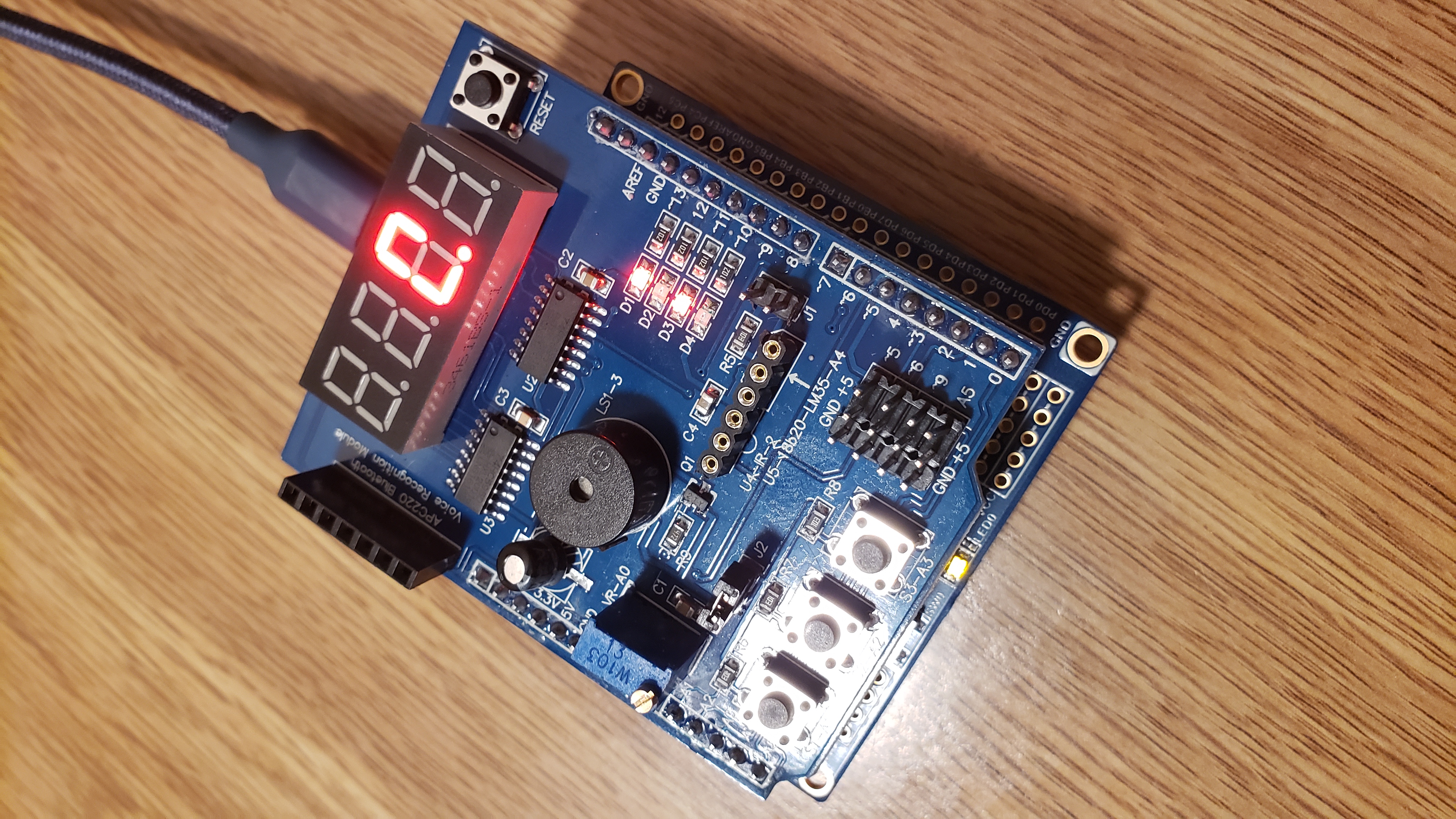
1. **SCHEMATICS**

Use fritzing.org

1. **SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)**



1. **SCREENSHOT OF EACH DEMO (BOARD SETUP)**



1. **VIDEO LINKS OF EACH DEMO**

<https://www.youtube.com/watch?v=kvSSHEG52GU>

1. **GITHUB LINK OF THIS DA**

<https://github.com/Jonesc30/Submission/tree/master/DesignAssignments>

**Student Academic Misconduct Policy**

<http://studentconduct.unlv.edu/misconduct/policy.html>

“This assignment submission is my own, original work”.

NAME OF THE STUDENT