

Term Project Proposal

Exploring End-to-End Bottlenecks in NVMe SSDs

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1. Motivation & Goal

Modern NVMe SSDs expose massive internal parallelism while relying on deep host queues and on-board DRAM buffers to hide flash latency. However, it is often unclear which component actually becomes the bottleneck for a given workload: host-side NVMe queues, the SSD's DRAM data buffer/cache, or the backend flash parallelism (channels/ways). This project aims to explore the bottlenecks using an SSD simulator, and to classify regimes where performance is limited by (1) host queueing, (2) DRAM buffering, or (3) flash parallelism.

2. Simulator & Configurations

- Simulator: **MQSim**

Starting from the baseline(Using the “MQ-SSD” configuration described in the **original MQSim paper as a baseline**), we change the following parameters:

- NVMe queueing (host-side) : IO_Queue_Depth $\in \{1, 8, 32, 128, 256\}$
- DRAM data buffer/cache - Data_Cache_Capacity (on-board DRAM buffer size):
 - {0 MB (DRAM-less), 128 MB, 256 MB (baseline), 1 GB}.
- Flash parallelism (channels/ways)
 - Flash_Channel_Count: 4 , 8 (baseline), 16.
 - Chip_No_Per_Channel (number of ways): 2, 4 (baseline), 8.

3. Workloads & Metrics

3.1 Workloads

Synthetic workloads (fio-like patterns via MQSim)

- 4 KiB random read, 4 KiB random write and 70/30 mixed read/write with varying queue depth
- 128 KiB sequential read/write (throughput-oriented) with varying queue depth

Trace-driven workloads

- TPCC trace - Part of Microsoft Enterprise Traces

3.2 Metrics

For each (configuration, workload) combination, we collect the following metrics:

- I/O statistics
 - Throughput, IOPS, Latency.
- Internal SSD statistics
 - Statistics of user vs. GC vs. mapping transactions in the TSU queues
 - Per-package time fractions spent in command execution, data transfer, overlapped operation, and idle mode.
- Power and energy (approximate)
 - Using the above transaction counts and package busy/idle time fractions together, estimate relative energy-per-I/O