Project 3: Cover Page

Name: Samson Hruday Chinta
Student ID: 5949682

Parameter	**Value**	**Unit**
Clock Period	0.0549963	ns
Minimum Delay(critical path)	0.053872	ns
Layout Area		μm^2

	GRADE
Delay [25]	
Area [15]	
Creativity [5]	
Report [5]	
Total [50]	

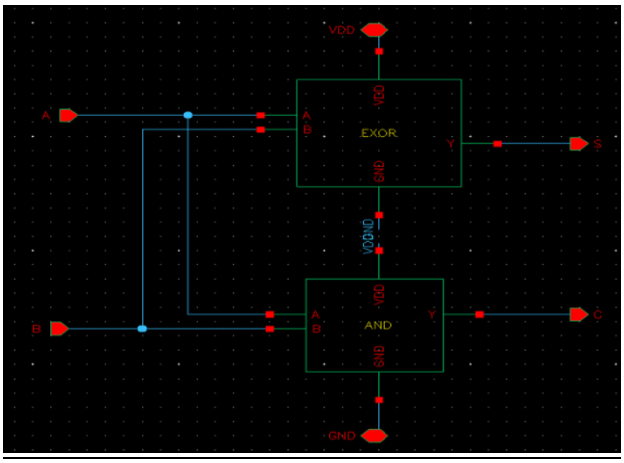
EE5323 VLSI Design I
Project 3
Submitted by: Keshav Krishnamurthy
Email ID: krish412@umn.edu

Objective:

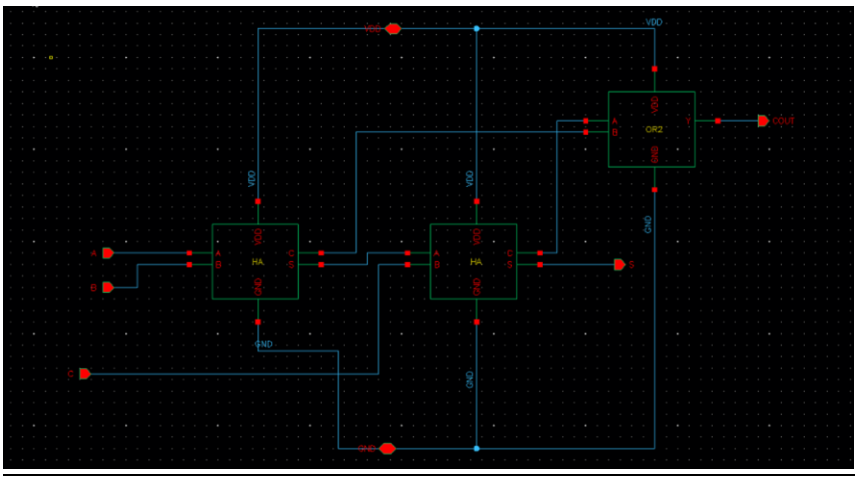
To design a high-performance **4-to-1 Integrate-and-Fire** neuron that maximizes speed.

Schematics:

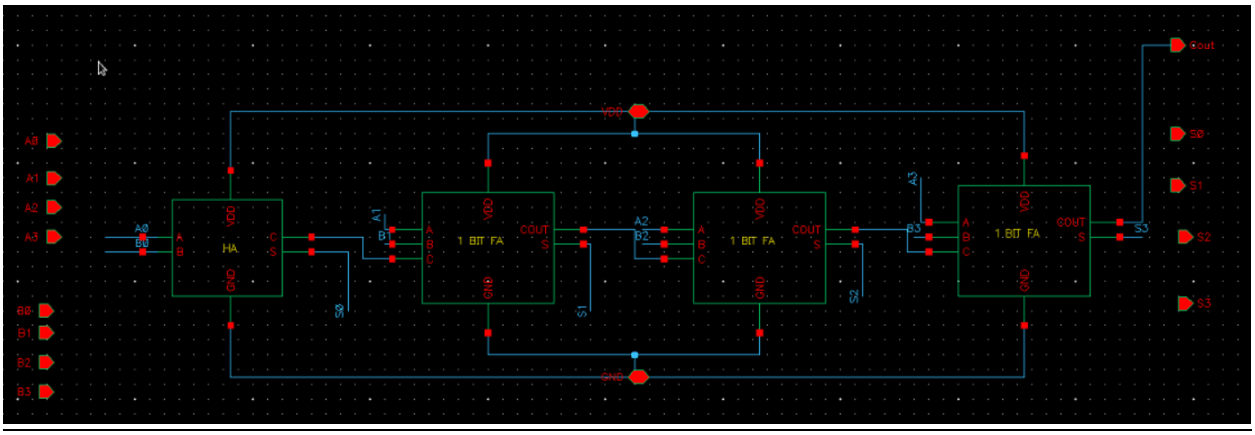
Half Adder:



1-bit Full Adder:



4-bit Full Adder:



D Flip Flop(C2MOS):

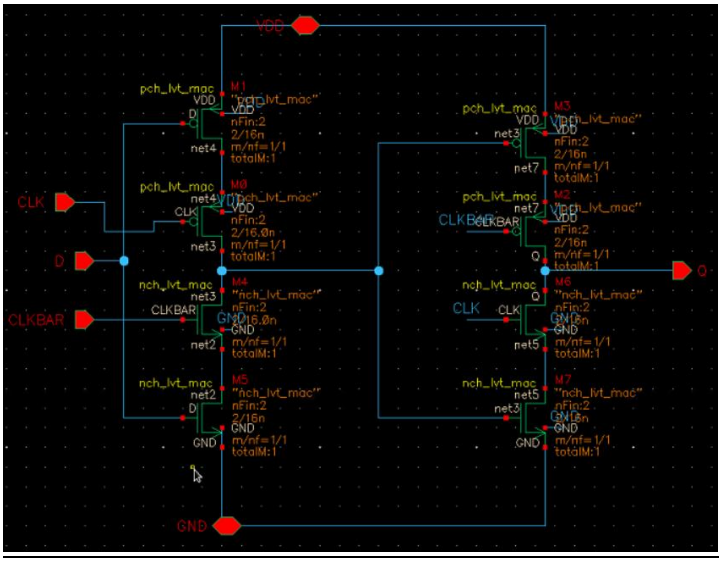
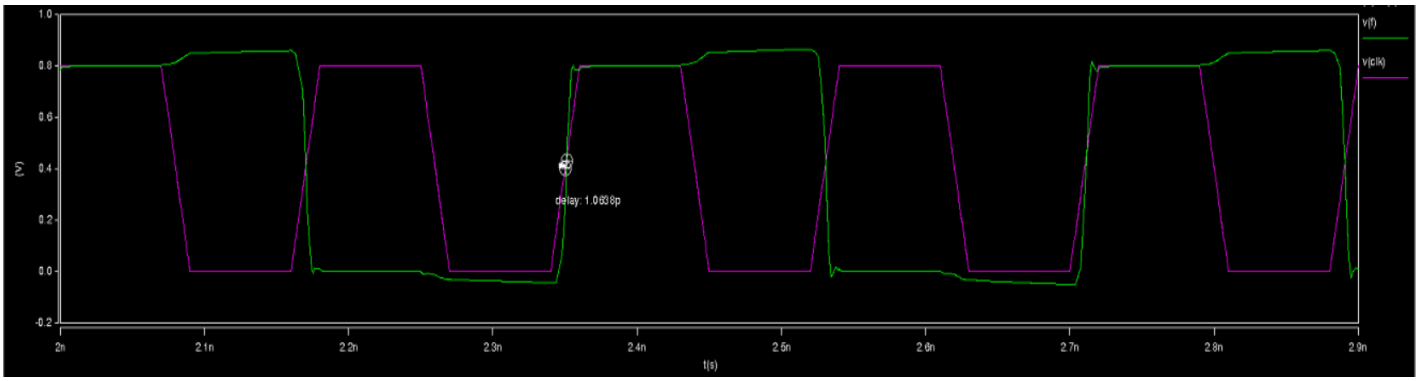
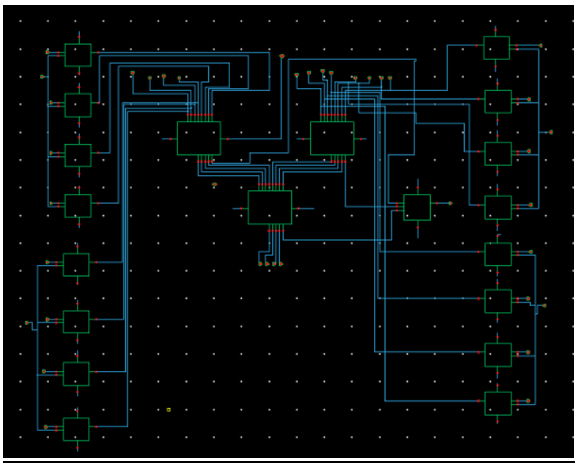


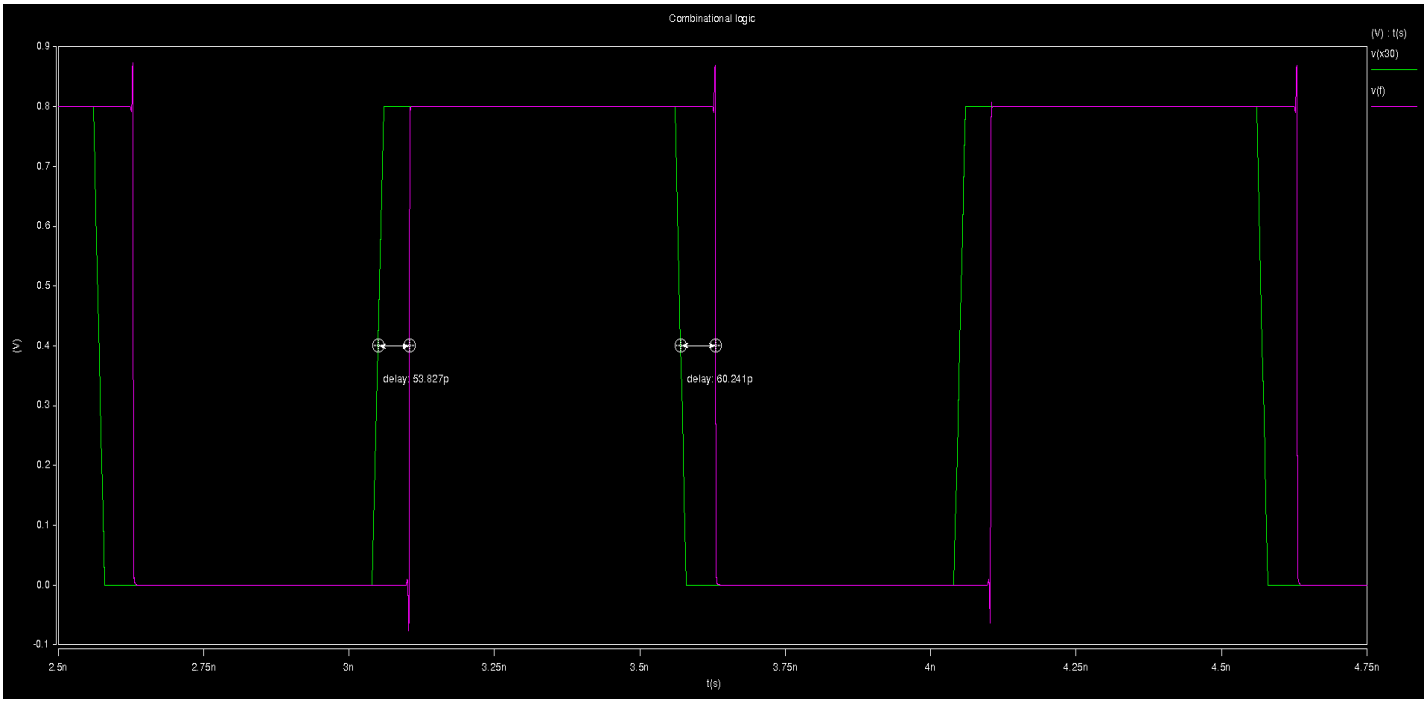
Image For Clock to Q Delay .



Tclock to Q delay :1.063ps

Combinational Logic of the Neuron:

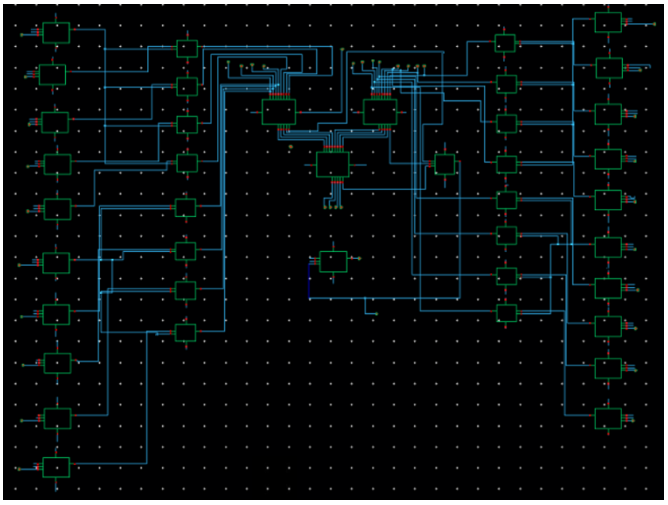




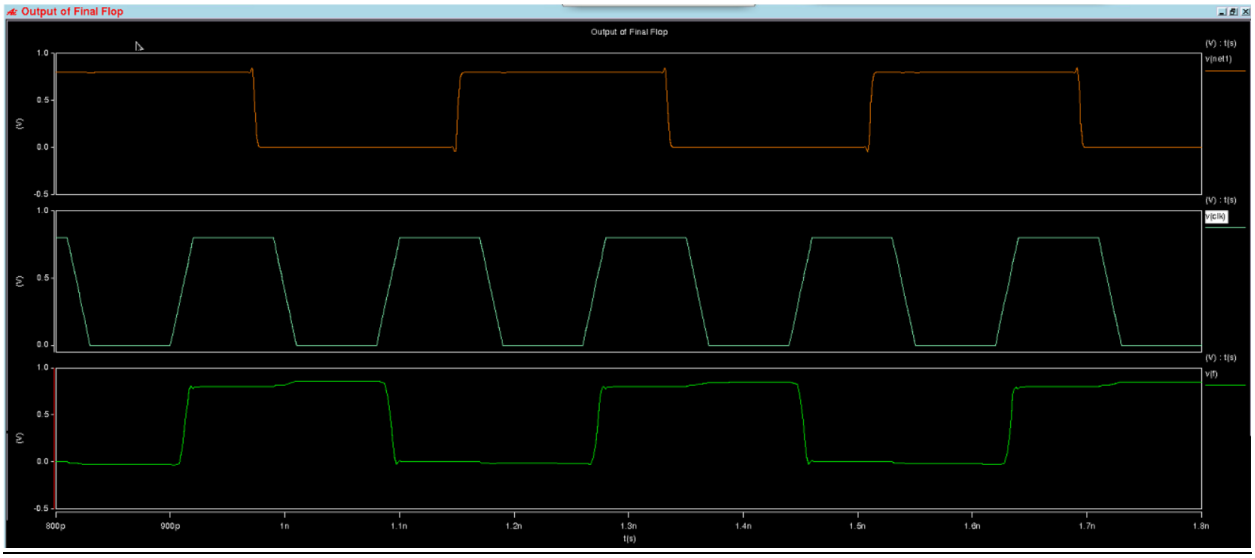
T raise (Tplh):53.827ps

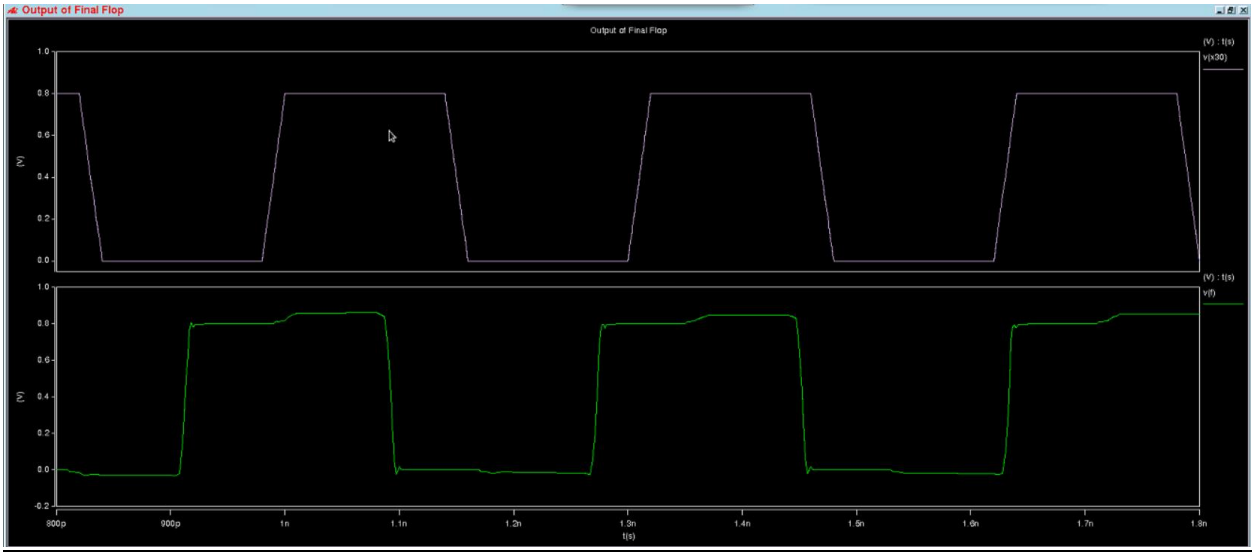
T Fall (Tphl): 60.241ps

Complete Schematic of the Neuron:



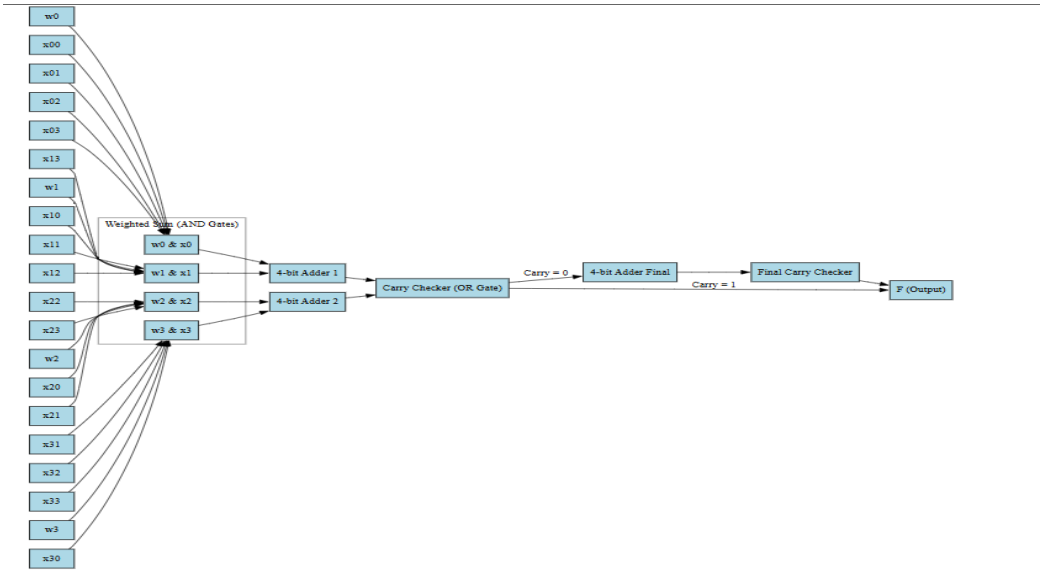
Final Flop Output :





Architecture of the Neuron:

The architecture is designed to evaluate a weighted sum using AND gates and detect specific carry conditions for triggering the output FFF. The weighted sum block consists of 16 AND gates, where four input weight signals (w0,w1,w2,w3) are combined with corresponding input signals to produce weighted outputs. These outputs are then grouped into two 4-bit adders, which compute partial sums. A carry checker (implemented as an OR gate) monitors the carry outputs of the two adders. If any carry is detected, F is triggered immediately. If no carry is present, the sums of the two adders are passed to a final 4-bit adder, whose carry output is checked by a second carry checker to determine F. To make computation more sequential and synchronized , we add a D – Flop for all the inputs and One at output . This modular design ensures efficient computation and minimizes unnecessary operations by early termination when a carry condition is met.



Input Stimulus To trigger Critical Path :

For i range from 0 to 3:

X0i = 1101

X1i = 0010

X2i = 0000

X3i = 0001(1-->0) and wi=1

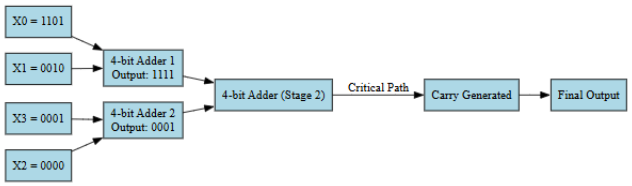
There are many stimulus vector that can trigger the critical path . Critcial path is the one which passes through the second stage of 4 bit adder and carry is being generated in the second stage .

When X0 and X1 are added we get output of 1111 at one of the 4bit adder in stage 1 and when X2 and X3 are added we get output of 0001 at another adder . Then we send both of the outputs as inputs for the second stage 4 bit adder which triggers the carry of the final output . we set all the weights as 1 . Flip Flop Architecture used C2MOS .

Calculation of max Clock Frequency , and Time period :

T clock >= TCombo + T c2q + 10% of T c2q (setup)

53.827ps +1.063ps + 0.1* 1.063ps =54.9963ps



Optimizations and work Done :

1.Make sure that critical path is near to the output switchings in every connection such that it gives you least delay on the critical path which makes path delay less and our neuron can work perfectly as fast as possible .

2. Use Lvt cells on the critical path for more faster circuit and svt for the Normal paths for power Optimizations .

Conclusion: *The waveforms of each module were successfully verified, confirming the correct functionality of the design. The circuit operates reliably with a time period of 54.9963 ps± 2% , which corresponds to a high operating frequency of approximately 17Ghz ±1% variation .This demonstrates the efficiency and robustness of the design, making it suitable for high-speed applications.*