UNIVERSITY OF MINNESOTA

EE5324 VLSI Design-II

Project report

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Submitted by :
Sivaramireddy Chittam -5927791
Samson Hruday Chinta -5949682

Submitted to :
Prof . Yang (Katie) Zhao
Teaching Asst. Sayantan Ghosh
Department of Electrical and Computer Engineering,
University of Minnesota, Twin Cities

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Project 1 Standard cell Design - OAI21D4

1.1 Objective

This report presents the design, verification, and layout of the OAI21D4BWP16P90 standard cell using the TSMC 16 nm (N16ADFP) PDK . The cell is an OAI21 gate, which logically implements:

$$Z = \overline{(A1 + A2) \cdot B}$$

Figure 1: Boolean Logic

1. Creating a schematic with correct transistor sizing (4 fins each).
2. Performing pre-layout simulations to validate functionality using an FO4 load.
3. Generating a layout that meets foundry design rules.
4. Verifying the layout with DRC and LVS checks.
5. Demonstrating a 3×3 array of the cell and confirming it meets DRC requirements.

1.2 Cell Function and Truth Table

A1	A2	B	Z
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Table 1: Truth table for the OAI21 logic.

1.3 Schematic Design Connections :

As a team, we approached the schematic design of the OAI21D4 standard cell methodically using Cadence Virtuoso. Our primary goal was to translate the Boolean logic of the OAI21 gate into a correct transistor-level implementation, while adhering to the 16nm TSMC (N16ADFP) process design rules. To realize this, we constructed a pull-up network with PMOS transistors in a configuration that reflected the NOR operation of the ANDed inputs with B. Specifically, we placed two PMOS transistors (for A1 and A2) in series and connected them in parallel with a PMOS for input B. For the pull-down network, we arranged NMOS

transistors such that A1 and A2 were in parallel, followed by a series connection with B to realize the OR-AND-Invert logic. All transistors were sized uniformly with 4 fins each to ensure consistency in drive strength and layout compatibility. We carefully labeled each node according to the standard cell naming convention: *Inputs: A1, A2 and B ,Output: ZN* and *Power/Ground: VDD and VSS*.
Throughout the schematic development, we collaborated closely to validate connectivity, device orientation, and hierarchy cleanliness. Before proceeding to simulation, we ensured that the schematic was logically sound and clean from connectivity or device errors.

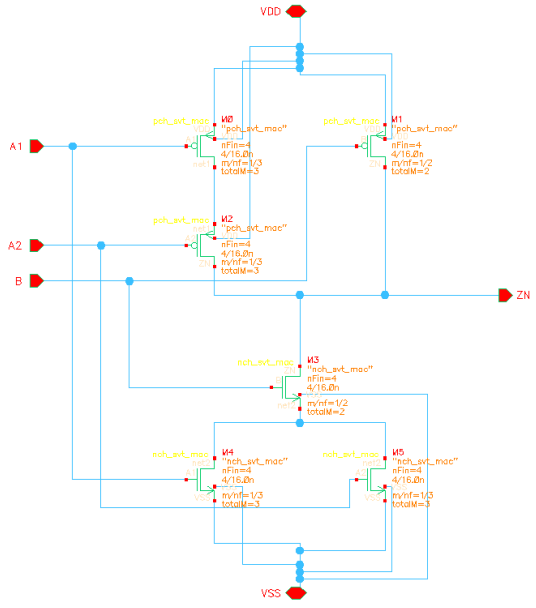

Figure 2: Transistor Level Schematic

1.4 Symbol Creation

The Following symbol has been created for the logic.

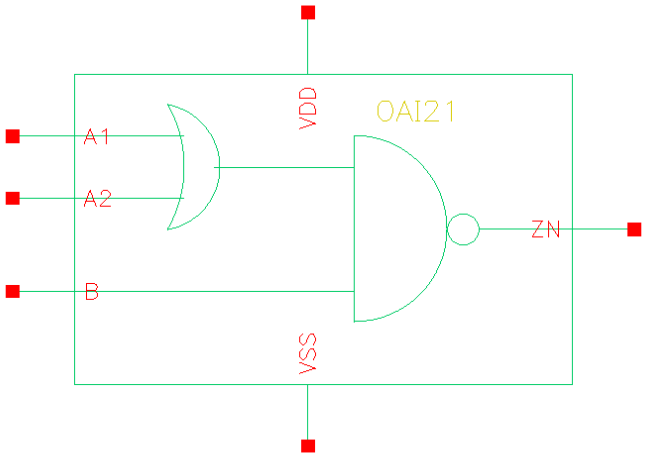

Figure 3: OAI21 Symbol

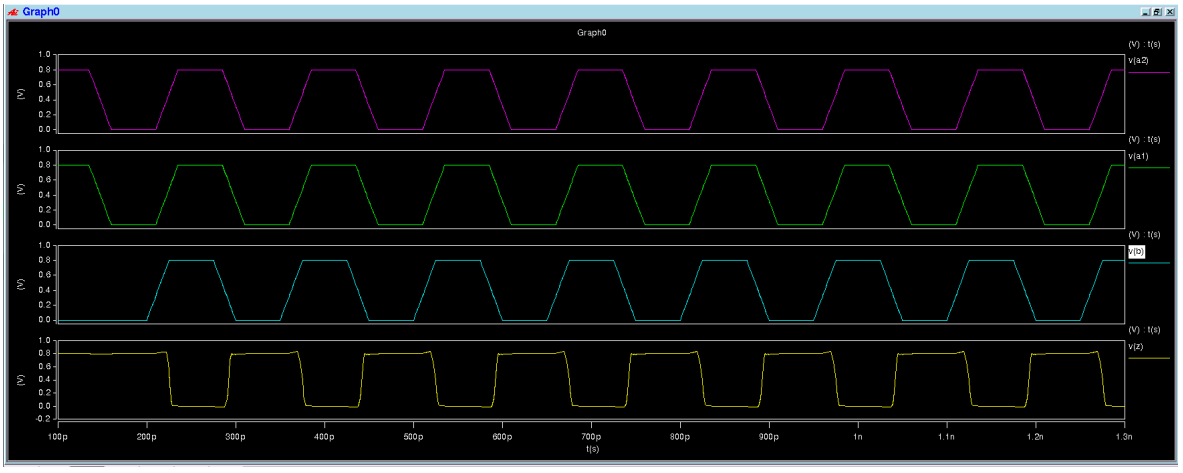

Figure 4: Waveform result for the testcases 110, 111 and 000

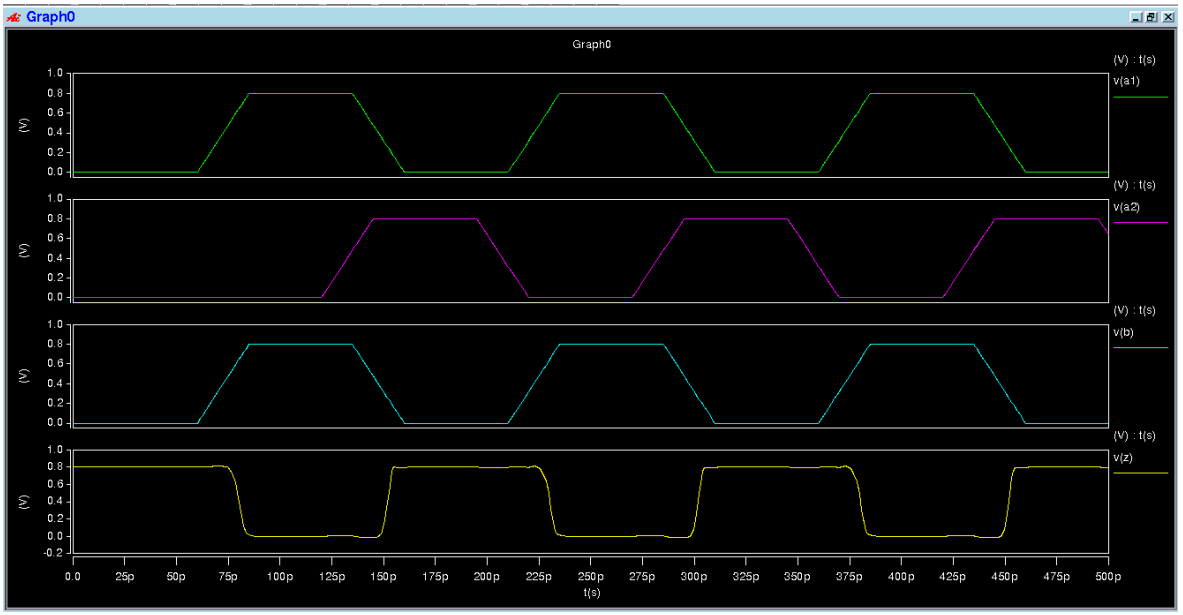

Figure 5: Waveform result for the testcases 101, 010

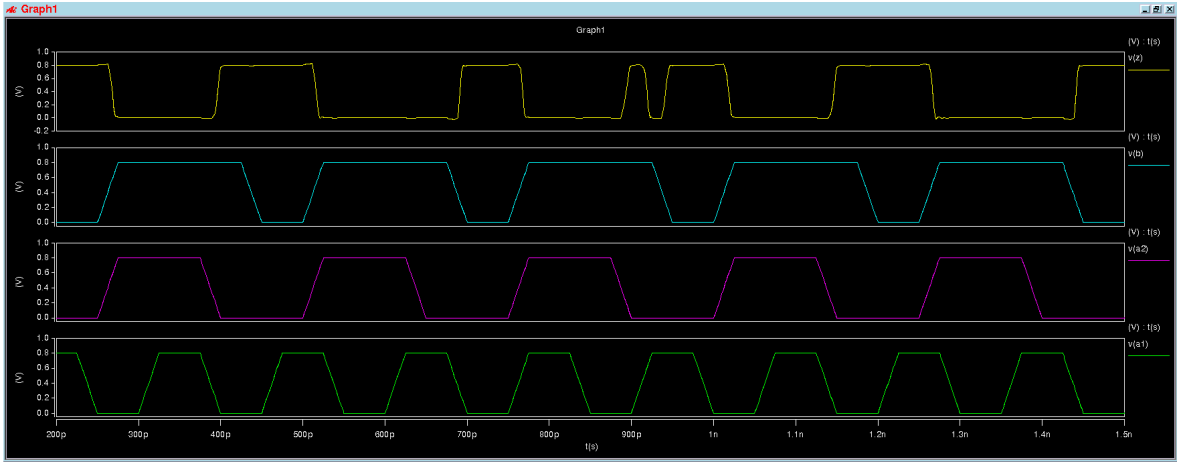

Figure 6: Waveform result for the testcases 100, 011

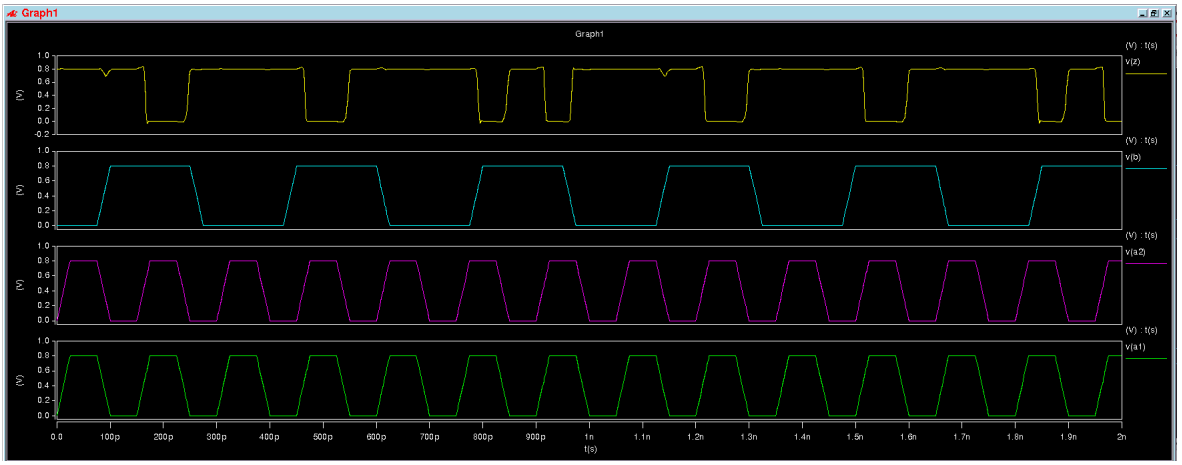

Figure 7: Waveform result for the testcase 001

1.5 Simulation Setup and Testbench with FO4 (fanout4) Load :

1. A testbench is created in Virtuoso, connecting Pulse sources (or digital voltage sources) to inputs A1, A2, and B, each with a 25 ps rise and fall time.
2. The OAI21 circuit (device) under test.
3. An FO4 load, implemented as four standard inverters or equivalent capacitive loading, at the output node Y.

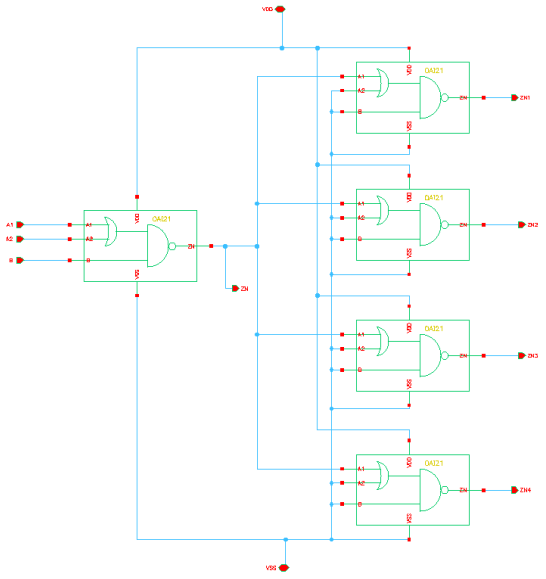

Figure 8: OAI Schematic with FO4

1.6 Simulation waveforms for functional verification:

For functional verification, our team developed a comprehensive simulation testbench in Cadence Virtuoso to test the OAI21D4 cell under both standard and loaded conditions. We aimed to validate the truth table exhaustively and evaluate the delay behavior under realistic fanout scenarios.

We configured the testbench with pulse sources driving the inputs A1, A2, and B. Each input waveform was configured with a 25 ps rise and fall time . We created 8 input combinations to fully verify the truth table of the OAI21 gate.

To emulate realistic load conditions, we applied a FO4 (fanout-of-4) load at the output. This was implemented using Same gate as load connected at the output node Z. The FO4 condition helps estimate the intrinsic delay and drive capability of the cell, which is essential for timing characterization.

The simulation waveforms clearly validated the correct logical behavior of the cell across all input cases. The output transitions matched the expected truth table values without glitches or timing issues, thereby confirming our schematic and functional correctness. Additionally, the FO4 output waveforms provided insight into the propagation delay and signal integrity, further ensuring the robustness of our design.

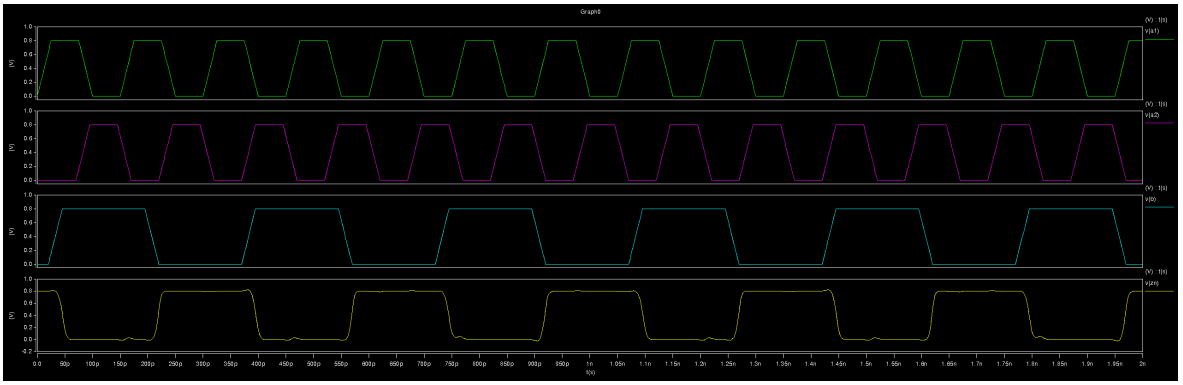

Figure 9: Waveform result for the testcases 110, 001, 000 and 111 under fanout (FO4) load

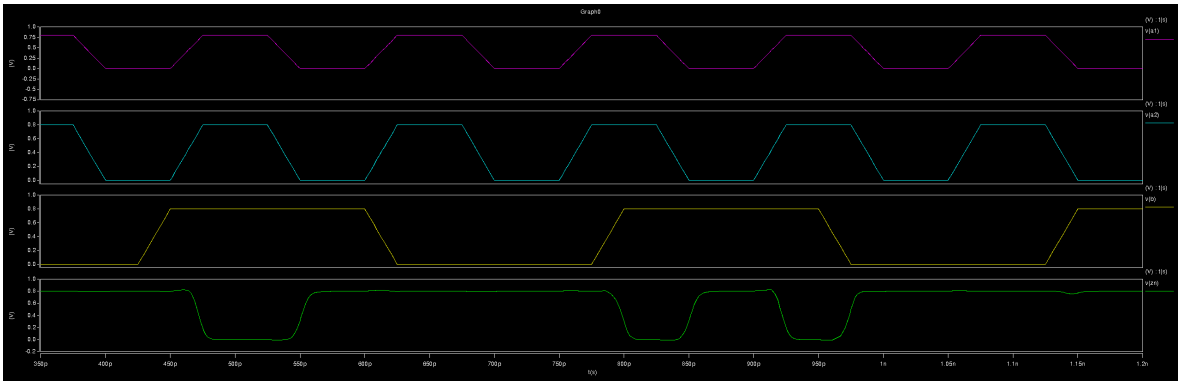

Figure 10: Waveform result for the testcases 011, 010 100 and 101 under fanout (FO4) load

1.7 Layout Methodology

As a team, we adopted a systematic and guideline-driven approach to layout design for the OAI21D4 standard cell using the TSMC 16nm PDK. Our goal was to ensure a DRC-clean and LVS-clean layout that aligns with the foundry's design rule manual (DRM) while maintaining layout symmetry, compactness, and tiling compatibility for standard-cell placement.

We began by placing the PMOS and NMOS transistors with 4 fins each, aligning with our schematic sizing. Careful attention was given to the well spacing, device orientation, metal layer usage, and pin accessibility to ensure standard-cell row compliance. We followed the N16ADFP layout conventions for cell height, VDD/VSS rail alignment, and pin placement.

After initial layout construction, we performed Design Rule Checks (DRC) and addressed all violations meticulously. Some minor DRCs were observed, such as PO.S.16, PP.W.1.T, and NP.W.1.T, which were related to tap cell spacing and poly width violations. Based on discussions in the course Canvas and the provided project guidelines, we confirmed that these specific violations could be safely waived, as they pertain to layout structures outside the scope of the standalone standard cell or will be resolved in top-level integration with tap cells and guard rings.

To validate tiling capability, we constructed a 3×3 array of the standard cell and verified it for DRCs. This confirmed that the cell abides by standard row placement rules without introducing new violations, which is essential for cell integration in real designs. Overall, our final layout passed all required checks and conformed to the design intent.

1.8 Single-Cell Layout

Layout screenshot

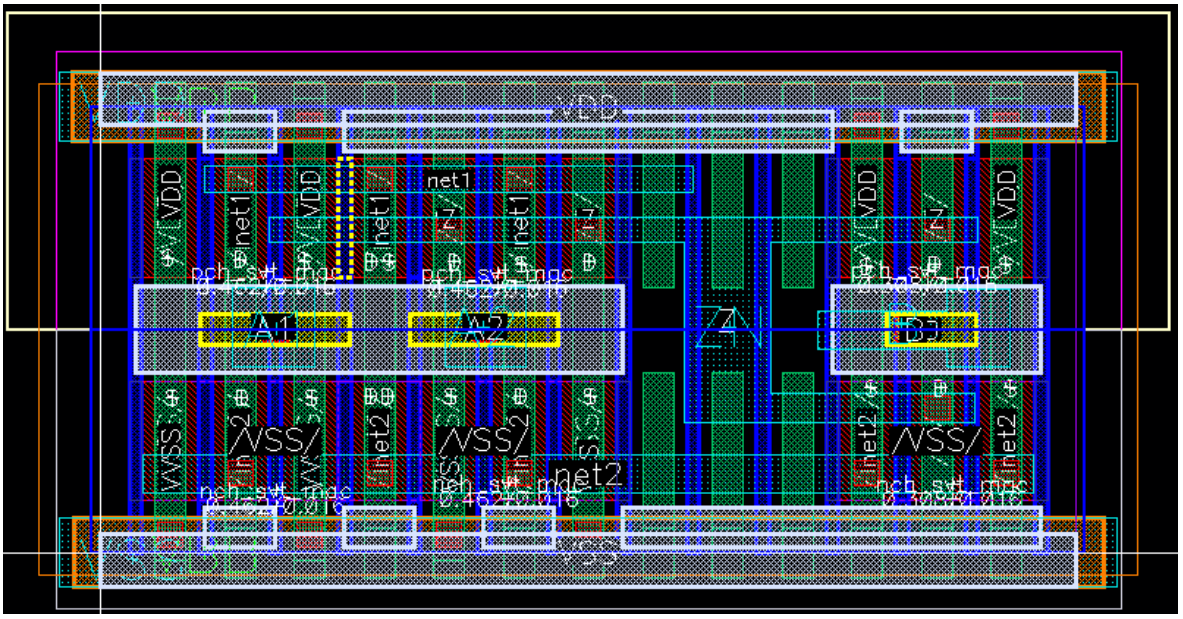

Figure 11: OAI21 Single cell Layout without Tapcell

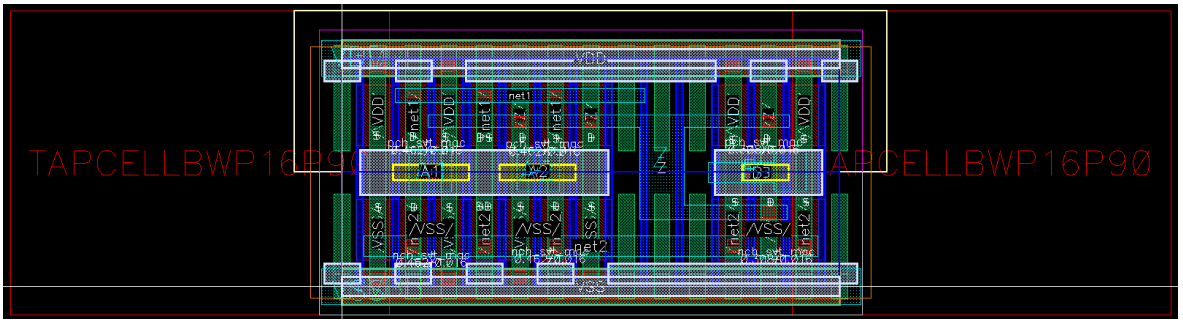

Figure 12: OAI21 Single cell Layout With Tapcell

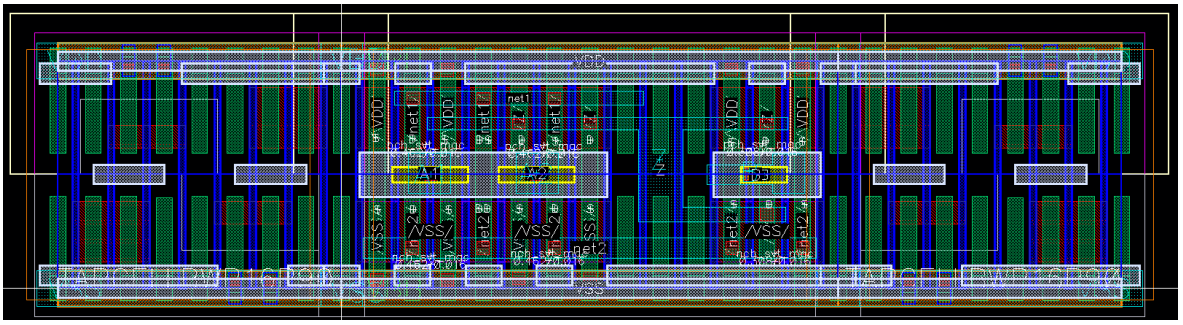

Figure 13: OAI21 Single cell Layout with Tapcell

DRC checking & screenshot

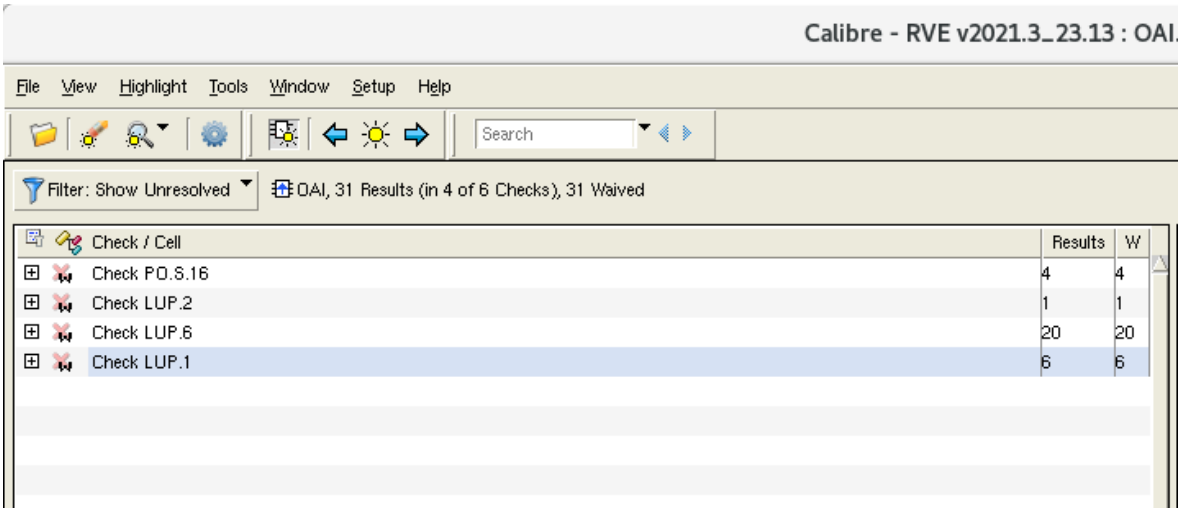

Figure 14: OAI21 Single cell DRC without Tapcell

LVS verification & screenshot

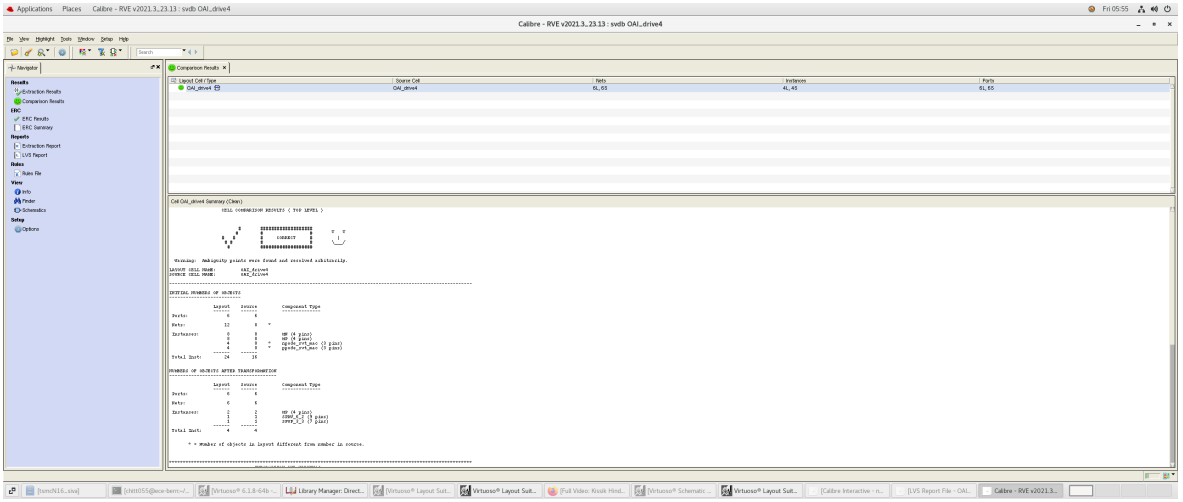

Figure 15: OAI21 cell LVS clean screenshot

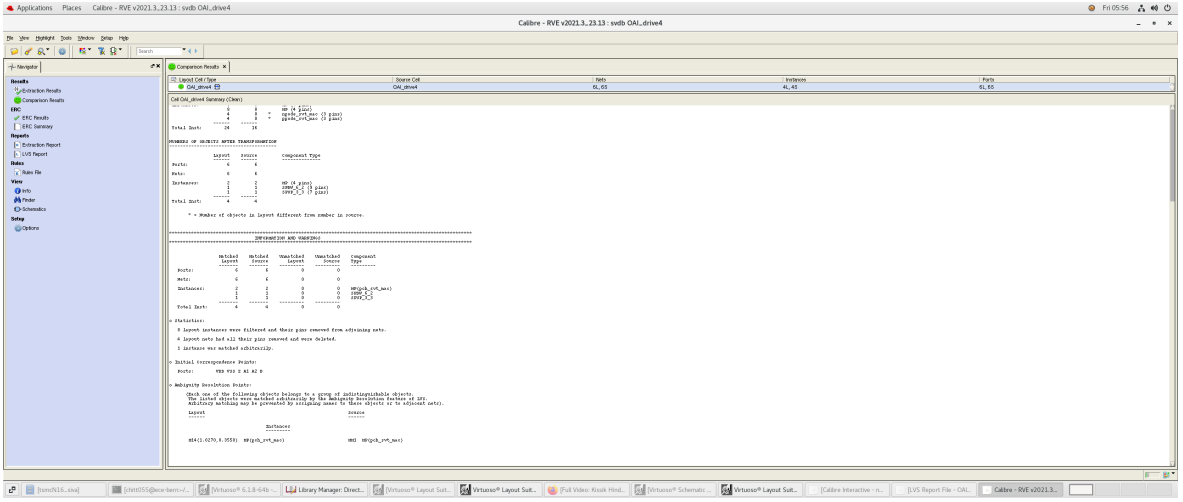

Figure 16: LVS Cleaned screenshot

1.9 3x3 Layout

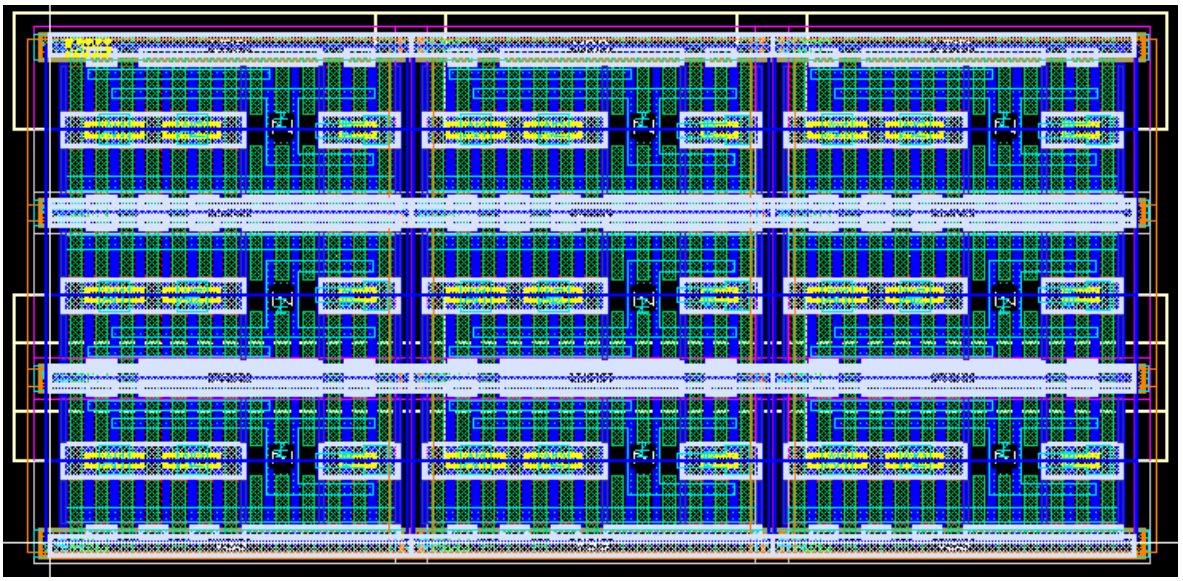

Figure 17: OAI21 3x3 Array without Tapcell

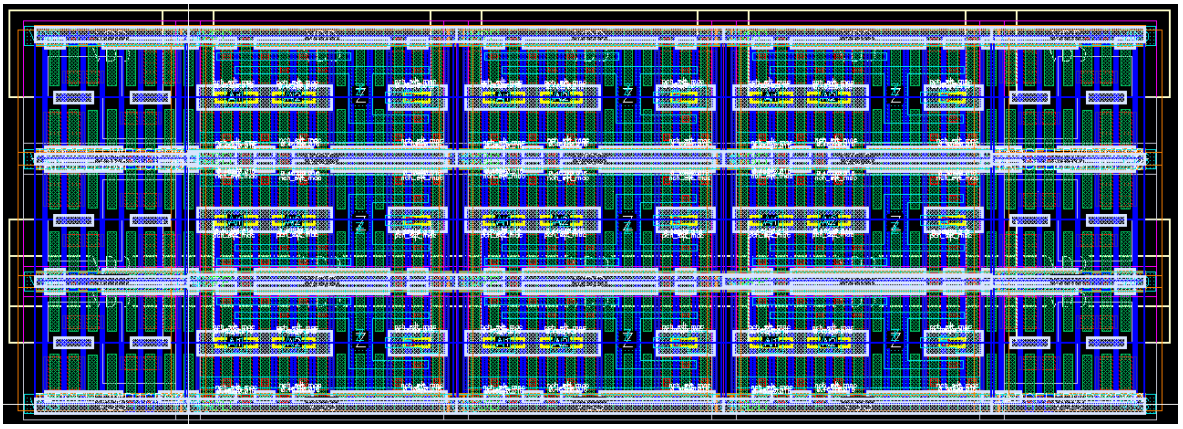

Figure 18: OAI21 3x3 Array with Tapcell

DRC Checks for the 3×3 Layout & Screenshot

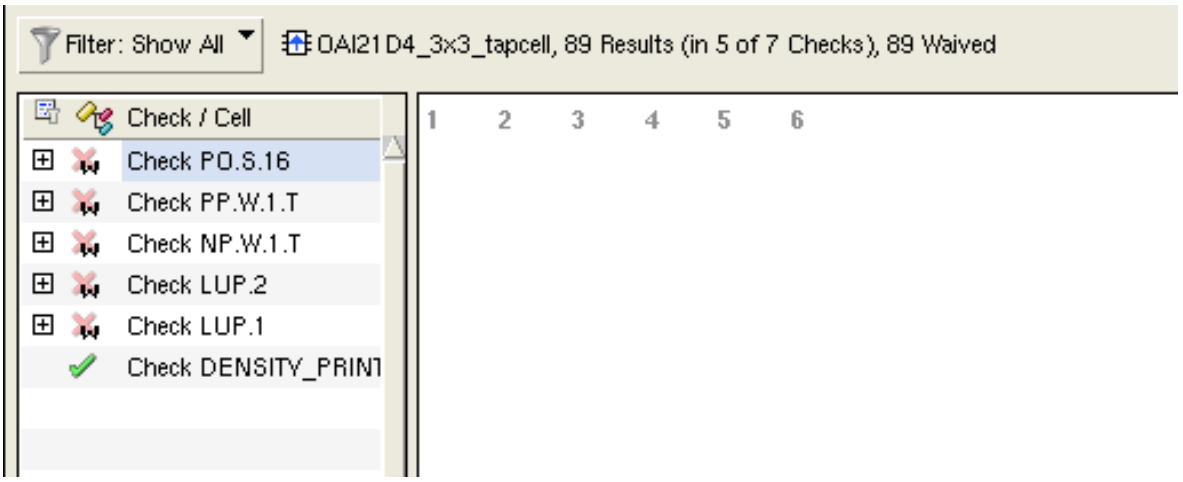

Figure 19: DRC result screenshot

1.10 Explanation of existing of DRCs

PO.S.16: Poly-to-Poly spacing violation – Space between two PO shapes is less than the minimum required.Occurred due to close placement of poly gates while optimizing area in the cell boundary.As per Canvas discussions and project guidelines, this can be waived off in standard cells since the full PR flow will insert filler cells and maintain spacing at the chip-level.

PO.S.16	TrGATE to 2nd PO space rule (Lg ≤ 0.036 µm): TrGATE of core device [channel length ≤ 0.036 µm] space to the second CrtPO in S/D and outside OD direction. (The second PO is required to be placed beside the Gate.)

Figure 20: PO.S.16

PP.W.1.T/NP.W.1.T:Tap cells (or bulk ties) not included in standalone cell view, causing diffusion shape to be narrower than required. Can be waived off as per discussions

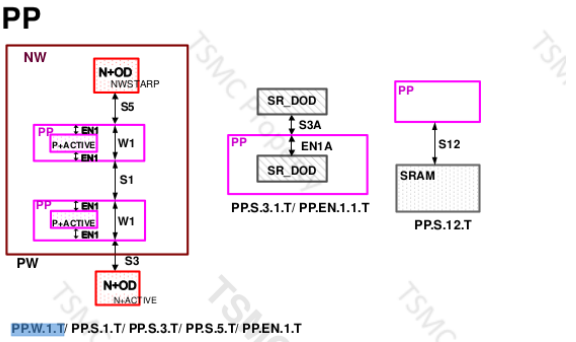

Figure 21: PP.W.1.T

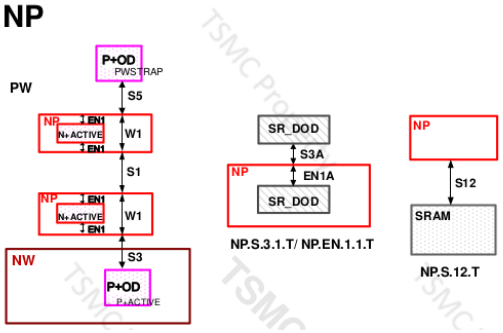

Figure 22: NP.W.1.T

LUP.1/LUP.2: The NMOS and PMOS clusters should be surroumded by the guard rings .

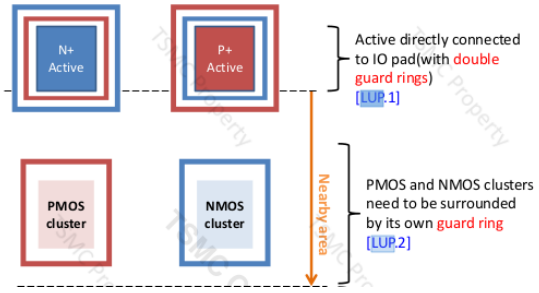

Figure 23: LUP.1/LUP.2

1.11 Path of File:

/home/class/chitt055/tsmcN16_siva/OAI21D4_VD2Project1
Contains the following files: Symbol , Schematic, Layout ,3x3 Layout,Testbench Schematic with FO4, .mto, report.pdf .

1.12 Conclusion

Successfully completed the standard cell design project for the OAI21D4 gate using the TSMC 16nm (N16ADFP) PDK. All design steps—from schematic creation, symbol generation, and functional simulation with FO4 loading, to full layout implementation—were carried out in accordance with the project guidelines.

We verified the functionality through simulations covering all possible input combinations, and our layout passed all essential DRC and LVS checks. The few remaining DRCs were reviewed and waived based on Canvas discussions and official project instructions, as they pertain to tap cell insertions typically handled at the integration level.

In conclusion, the project was compiled and completed successfully, demonstrating both functional and physical design correctness, and adherence to the design rule manual (DRM) requirements.