EE 5324 Spring 2025
Project #1
Due 02/28/25, Friday, 11:59pm. Submitted to Canvas.

Follow the submission and documentation instructions carefully to receive credit.

Use the TSMC 16nm PDK and the typical corner for all simulations. Use the Virtuoso schematic and layout editor, HSPICE and Cscope/WaveViewer for this exercise. Please refer to the Design Rule Manual by opening the symbolic link 'N16ADFP_DRM_V1.1_1.pdf' present in your run directory ('<Your_Folder_Name>') for the layout rules. Use Typical corners for all simulations.

Note: (1) Your cells will be checked for DRC correctness. (2) Your cells will be checked for LVS correctness (Note: By 2/12/24, LVS errors, the same as in the "Cadence Tutorial 2025.pdf" file, do not need to be fixed. We will update the tutorial once we figure out how to resolve these errors. Until the update, LVS errors similar to those in the tutorial will be considered acceptable.)

Find the cells that have been assigned to your group in the given document "EE5324_S25_Lab1_Cell_Assignment.pdf". You have to submit one report in the form of a ppt or pdf for the cell that you are assigned. You also need to attach all design files of the assignment. Each group only needs to submit one report, with one student of each group submitting the report on behalf of the group. For each cell follow the below steps.

1. **Schematic and pre-layout simulation:**
   - Make a schematic of the cell in Virtuoso Schematic editor, make sure your schematic is clear and legible. Follow the pin naming convention in the 'N16ADFP_StdCell' library provided to you.
   - All transistors should be of 4 fins (layout layer: ref)
   - Simulate the schematic (pre-layout) netlist with an appropriate FO4 (fanout = 4) load for the output drive strength of your gate. Use a voltage source with 25ps (0%→100%) rise and fall time for your data inputs.

   Provide the following in your report for this part:
   a) Truth table for your cell
   b) Schematic with visible sizing
   c) Symbol
   d) Simulation waveforms showing functionality for the schematic
   e) Testbench schematic that includes your cell + load (FO4)

2. **Layout:**
   - Design the layout of your cell using the Virtuoso layout editor (Layout XL), **ensuring that the height, width, and placement of input and output pins match those in the 'N16ADFP_StdCell' layout. The pin shapes should also be consistent with the reference layout.** Any deviation will eliminate credit for layout.
   - Verify the layout by running DRC and LVS. Note that this requires a tapcell. Do NOT forget to remove the tapcell when submitting your cell directory. Save the DRC and LVS summary pages for your report.
   - **Layout Guidelines**:
     a) Try using **parametric cells**
     b) **Running DRC/LVS (Add tap cell but remove it while submitting)**.

Please load the sunset file from the following locations and you will be able to run DRC/LVS smoothly.

DRC:

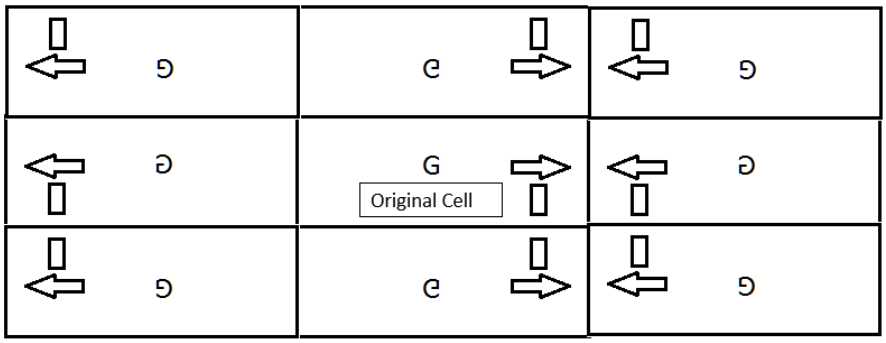
`/home/vlsilab2/TSMCHOME/Executable_Package/Collaterals/Tech/DRC/N16ADFP_DRC_Calibre/LOGIC_TopMr_DRC/N16ADFP_DRC_Calibre_11M.11_1a.encrypt`

LVS:

`/home/class/ee5323ta/N16ADFP_iPDK/N16ADFP_LVS_Calibre`

c) Extra DRC check (do NOT add tapcell)

Create a new cell view that is named "[cell_name]_test", instantiate your original standard cell (without the tapcell) and add mirror flipped copies of your original standard cell to make a 3x3 array (refer to figure below). Run DRC on this 3x3 layout. You also need to submit the DRC result screenshot of the 3x3 layout, as well as the single cell DRC screenshot.



Provide the following in your report for this part:

a) Cell layout screenshot
b) DRC and LVS report screenshots of your single standard cell
c) 3x3 layout screenshot and DRC screenshot for this 3x3 layout
d) Link to the folder which contains your cell
e.g. `/home/class/<YOUR_UMN_USERNAME>/<FOLDER_WITH_CELL>/<CELL_NAME>`

General Guidelines:

1. Start early.
2. Run simulations at 70° C
3. The load inverter (design using your assigned cells), which is used to achieve fanout of 4, should be included only in the testbench (not in layout or schematic).
4. In layout, all the vias, instances, wires and objects should be on the grid. Do not change the grid settings (x snap spacing and y snap spacing) while doing layout. An easy way to ensure everything is on grid is to check that the X and Y coordinates of any object do not have more than 3 significant digits after the decimal point.
5. Follow the naming convention and organize your files from the beginning.
6. Capture your schematics and layouts on white background, which can be done by File>Export Image in virtuoso.
7. First line in HSPICE is always a comment. Do not put anything there, so put your ".temp" command in the next line or thereafter.
8. Cscope/WaveViewer waveforms and schematics should be on white background and be clearly visible.

Submission Instructions:
Before submission, recheck your .bz2 file by extracting it on a different machine and whether all files open properly (DUT, or design under test, refers to your standard cell). The hierarchy must be as shown below.

<NAME>_<UMN_ID>_Project1.bz2
- *-Report_<CELL_NAME_1>.pdf*
- **-<CELL_NAME_1>**
  - *-schematic*
  - *-layout*
  - *-symbol*
- **-<CELL_NAME_1>_test**
  - *-3x3 layout*
  - *-testbench schematic (DUT + load)*
  - *-testbench netlist (DUT + load)*
  - *-HSPICE testbench*
  - *-*.mt0 files (measurement files)*

Compress them to one tar file by either right clicking on the top folder and going to compress option or use the following command:

tar -cjf <student_ID>_Project1.bz2 <student_ID>_Project1_

Submit the *.bz2 file to canvas. Attach the report separately on canvas.