

Implementation Guidelines

- Isolate sensitive asynchronous inputs such as Clock or Bidirectional Pins from other switching pads with Power/Ground Pads
- Group Bidirectional Pads together such that all are in the input/ output mode
- Avoid continuous placing of simultaneous switching pads
- 2 extra pins = 1 extra pad on 2 sides and 4 extra pins = 1 extra pad on each side
- Power supply pads must be evenly distributed
- The number of Power Pads required are calculated based on the IO Signal Pads power requirement and Core Power requirement (IR drop limit)
- No. of IO Power Pads required in a design, Thumb Rule: One Pair of Power Pads for every 4 or 6 Signal Pads
- No. of Core Power Pads required in a design,

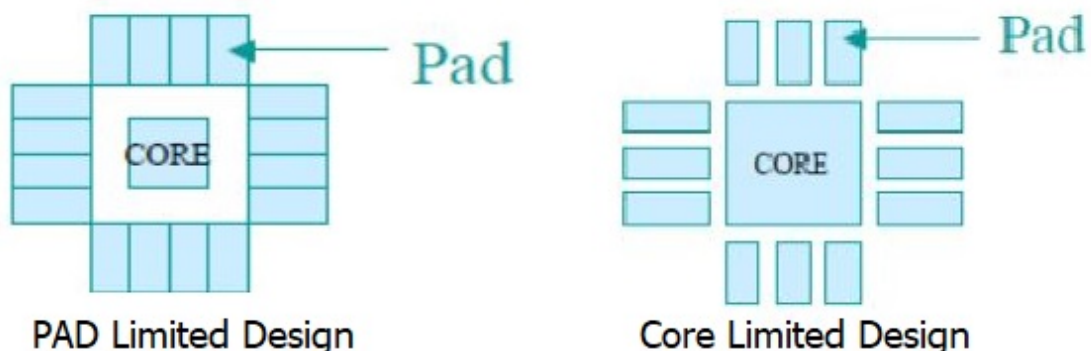
$$\text{Pads per side} = \frac{\text{TotalCorePower}}{(\#side * V_{\text{worst}} * \text{MaxAllowableCcurrentofPad})}$$

Pad Limited design

- The area of Pad limits the size of Die
- No. of IO pads are more or larger in size (technology dependent)
- Pad limited designs pose several challenges for design implementation and to the backend designers, if Die area is a constraint
- The Solution would be to use Flip Chip or Staggered IO placement techniques

Core Limited Design

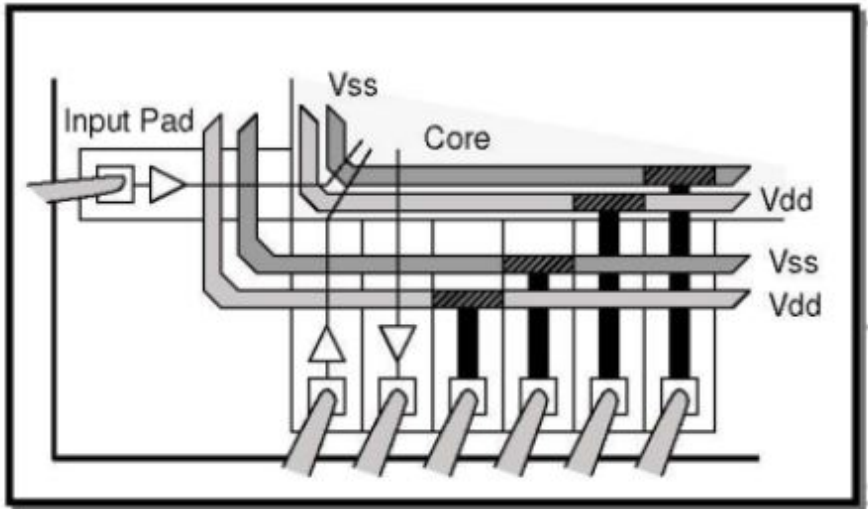
- The area of Core limits the size of Die
- No. of IO Pads are lesser
- In these designs Inline IOs will be used
- It can be either due to large no. of Macros the design or due to larger logic



Types of IO Pads

Types of Pads according to Logic directions

- Input Pad
- Output Pad
- Bidirectional Pad

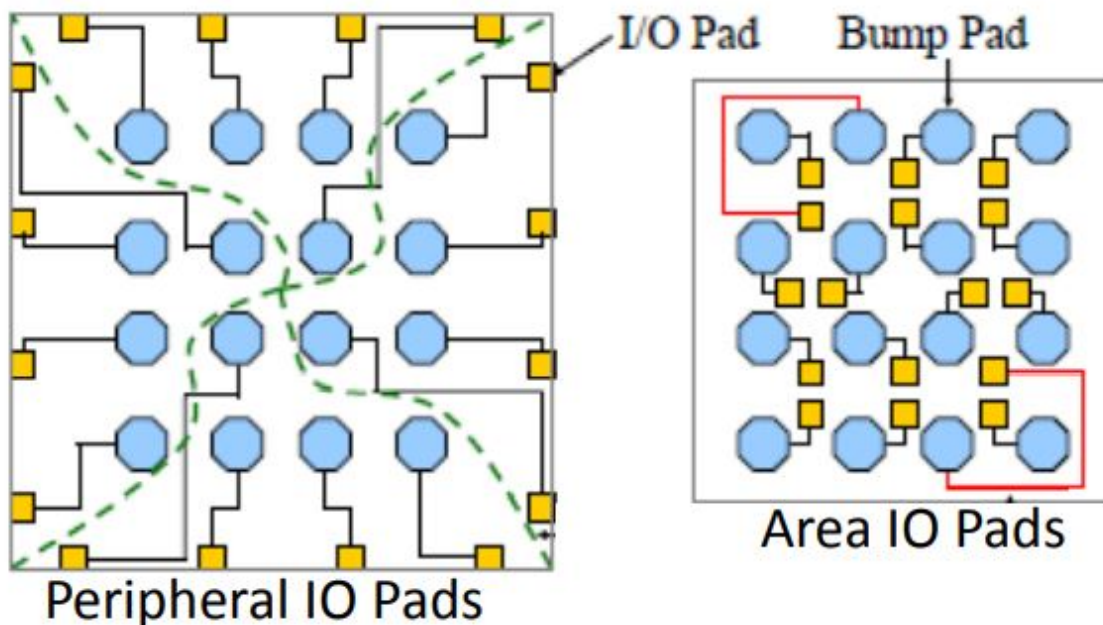


Types of Pads according to Logic Styles

- Signal Pads
- Power Pads (Core Power and IO Power)
- Corner Pads
 - Corner pads contains only connections in all metal layers defined in technology
 - These pad used only for IO Ring continuity and chip metal density on corners and to maintain yield
- Filler Pads
 - IO Filler Cells contains only the geometrical information of the Power Rings in all metal layers
 - Continuity of Power Rings which is responsible for uniform distribution of power
 - Electrostatic Discharge protection

According to the Pad locations

- Peripheral IO Pads
- Area IO Pads

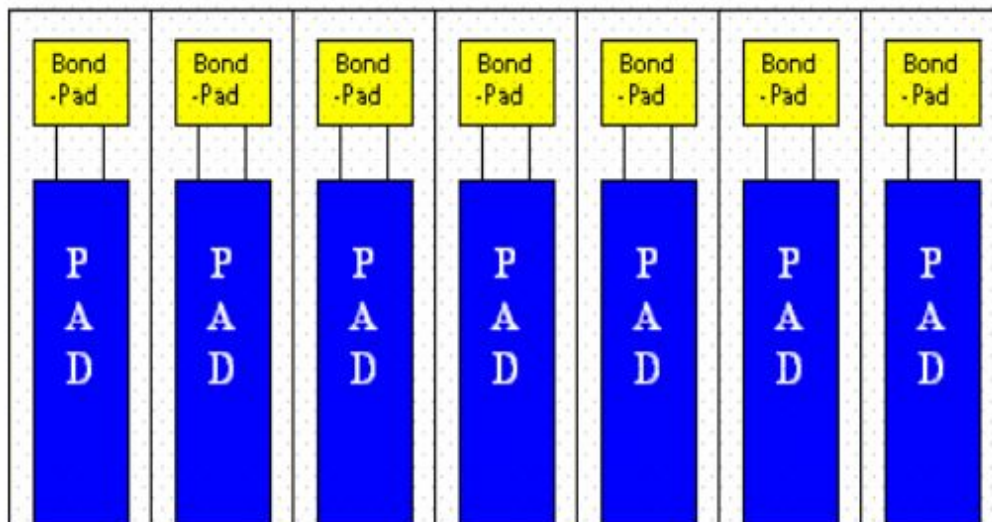


Types of Pads according to Implementation Styles

- Inline
- Staggered

- Staggered
 - CUP (Circuit-Under-Pad)
 - Non-CUP (Circuit-Under-Pad)
- Flip Chip

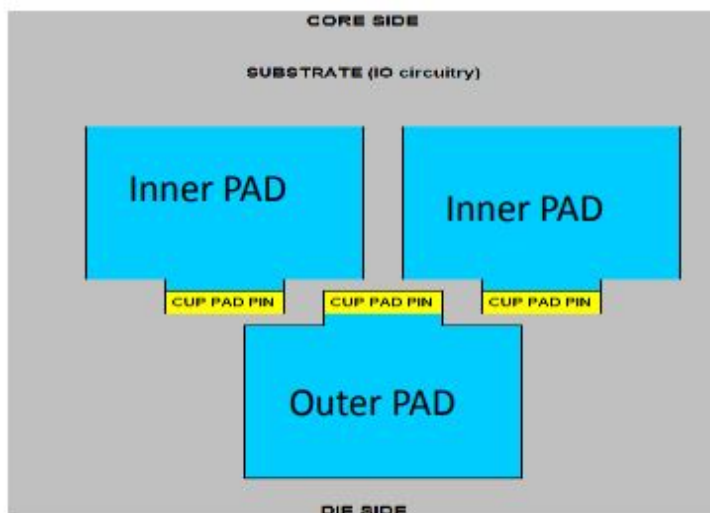
Inline IO Pads



- Pads are placed next to each other, with the corresponding bond pads lined up against each other having a small gap in between
- Minimum Pitch is determined by foundry/vendor and is technology dependent

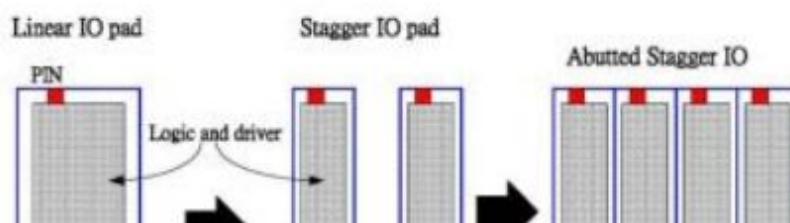
Staggered IO Pads

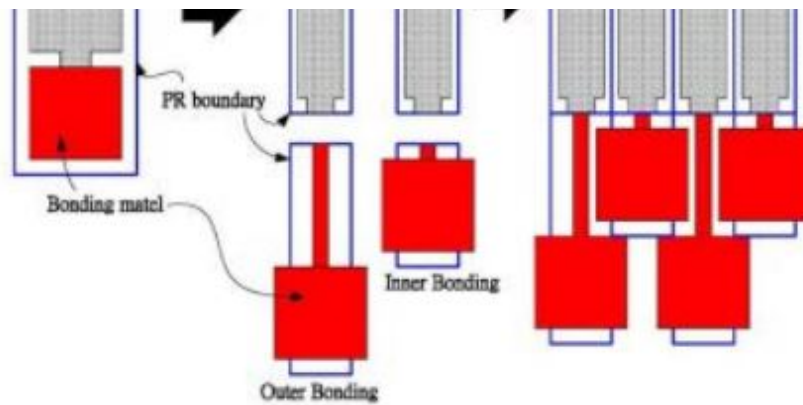
CUP (Circuit-Under-Pad)



- Bonding Pad over the IO body itself
- Bonding Pad have to connected to the PAD Pin of IO
- Pad pin is located close to the center of the IO body for easier routing, signal integrity, and space saving
- Reduce the die size since the Bonding Pad does not take any extra space in addition to the IO body itself
- Advantages include more no. of IO's, Optimal area utilization, Lower cost

Non-CUP (Circuit-Under-Pad)

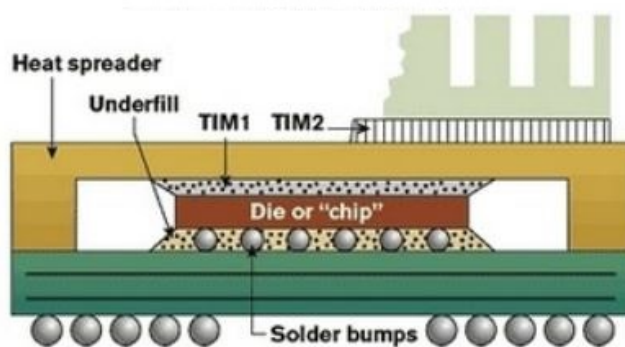




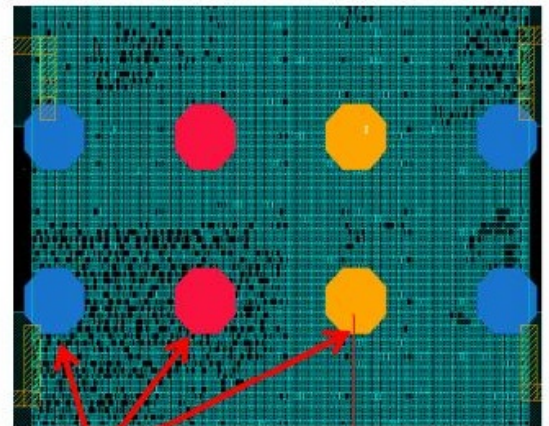
- Useful technique if design is “Pad Limited”
- Place an inner and outer Bond Pad alternately
- A larger number of pads can be accommodated
- Disadvantage is that the overall height of the pad structure increases significantly

Flip Chip IO Bumps

- It is simply a direct connection of a flipped electrical component onto a substrate, carrier, or circuit board by means of conductive Bumps instead of the conventional Wire-bond
- In Flip Chip, IO Bumps and driver cells may be placed in the peripheral or core area
- Note, the large octagonal area IO Bumps overlaying placed cells in the core area
- No chip area benefit for small chips – full Bump array redistribution is very difficult
- In advanced technology nodes a separate Re-distribution layer (RDL) is make use of for the Bump connections



Flip Chip Architecture



BUMPS

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