CMOS Fundamentals

Q1. Why low power has become an important issue in the present day VLSI circuit realization?

Answer:
In deep submicron technology the power has bec : In deep submicron technology the power has become as one of the most important issue because of: Increasing transistor count; the number of transistors is getting doubled in every 18 months based on getting doubled in every 18 months based on Moore,s Moore,s Law Higher speed of operation; the power dissipation is proportional to the clock frequency Greater device leakage currents; In nanometer technology the leakage component becomes a significant percentage of the total power and the leakage current increases at a faster rate than dynamic power in technology generations

Q2. How reliability of a VLSI circuit is related to its power dissipation dissipation?

Answer:
It has been observed that : It has been observed that every 10ºC rise in temperature ºC rise in temperature roughly doubles the failure roughly doubles the failure rate because various fa rate because various failure mechanism lure mechanism such as silicon interconnect fatigue, such as silicon interconnect fatigue, electromigrat electromigration diffusion, ion diffusion, junction diffusion and thermal runaway starts occurring as temperature increases.

Q3. How environment is affected by the power dissipation of VLSI circuits circuits?

Answer:
According to an estimate of the U.S. Environmental Protection Agency (EPA), 80% of the power consumption by office equipment are due to computing equipment and a large part from unused part from unused equipment. Moreover, the power equipment. Moreover, the power is dissipated is dissipated mostly in the form of heat. The cooling techniques, such as AC transfers the heat to the environment.

Q4. Why leakage power dissipation has become an important issue in deep submicron technology in deep submicron technology?

Answer:
In deep submicron technology deep submicron technology the leakage component the leakage component becomes a significant percentage of the total power and the leakage current increases at a faster rate than dynamic power amic power in new technology technology generations. That is why the leakage pow generations. That is why the leakage power has become an important issue.

Q5. Distinguish between energy and power dissipation of VLSI circuits. Which one is more important for

portable systems systems?

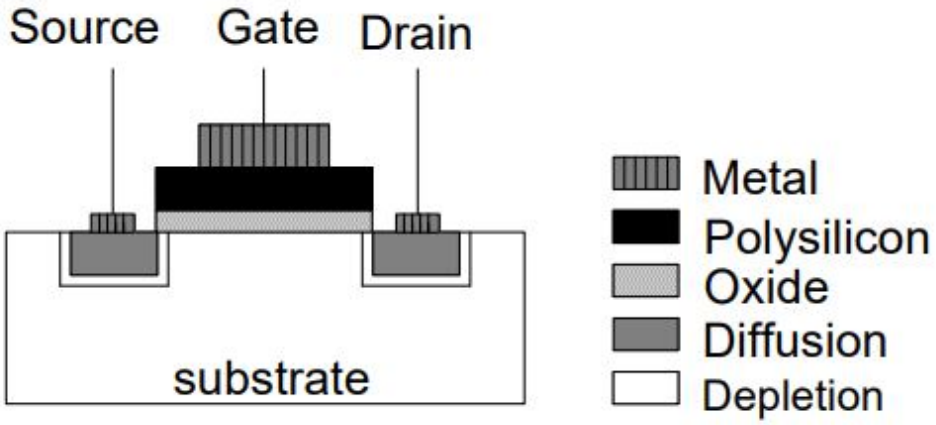
Answer:
Power (P) is the power dissipation in Watts at : Power (P) is the power dissipation in Watts at different fferent instances of time. On the other has energy (E) refers to the energy consumed in Joule over a period of time (E = P*t).

Q6. What are the commonly used conducting layers used in IC fabrication?

Answer:
Fabrication involves fabrication of Fabrication involves fabrication of patterned laye atterned layers of the rs of the three conducting materials: metal, poly-silicon silicon and diffusion by using a series of photolithographic techniques and chemical processes involving oxidation of silicon, diffusion of impurities into the silicon and deposition and etching of aluminum or polysilicon polysilicon on the silicon to provide interconnectio on the silicon to provide interconnection.

Q7. Show the basic structure of a MOS transistor.

Answer:
The basic structure of a MOS transistor is given below. On a lightly doped substrate of silicon two islands of diffusion regions called as source and drain, of opposite polarity of that of the substrate, are created. Between these two regions, a thin insulating layer of silicon dioxide is formed and on top of this a conducting material made of poly-silicon or metal called gate is deposited.



Q8. What is the latch up problem that arises in bulk CMOS technology?

Answer:
The latch : The latch-up is an inherent problem in both n up is an inherent problem in both n-well as well a well as well as pwell based CMOS circuits. The phenomenon is caused by the parasitic bipolar transistors formed in the bulk of silicon as shown in the figure for the n in the figure for the n-well process. well process. Latch-up can be defined as the formation of a low-impedance path between the power supply and formation

Latch-up can be defined as the formation of a low-impedance path between the power supply and formation of a low-impedance path between the power supply and ground rails through the parasitic ground rails through the parasitic npn and pnp bipolar transistors. bipolar transistors. As shown the BJTs are cross As shown the BJTs are cross-coupled to form the st coupled to form the structure of a ructure of a silicon silicon-controlled controlled-rectifier (SCR) providing a short rectifier (SCR) providing a short-circuit path circuit path between the power rail and ground. Leakage current through the parasitic resistors can cause one transistor to turn on, which in turn turns on the other transistor due to positive feedback and leading to heavy current flow and consequent device failure.

Q9. How the latch up problem can be overcome?

Answer:
There are several approaches to reduce the ten : There are several approaches to reduce the tendency of Latch of Latch-up. Some of the important techniques are up. Some of the important techniques are mentioned below:

- Use guard ring around p Use guard ring around p- and/or n and/or n-well with frequent well with frequent contacts to the rings
- To reduce the gain product B1XB2
- Moving the n Moving the n-well and the n+ source/drain further well and the n+ source/drain further apart
- Buried n+ layer in well to reduce gain of Q1
- Higher substrate doping level to reduce R Higher substrate doping level to reduce R-sub
- Reduce R Reduce R-well by making low resistance contact to well by making low resistance contact to GND

Q10. Distinguish between the bulk CMOS technology with the SoI technology fabrications. technology fabrications.

Answer:
In bulk CMOS technology, a lightly doped p : In bulk CMOS technology, a lightly doped p-type or n-type substrate is used to fabricate MOS transis type substrate is used to fabricate MOS transistors. On the other hand, an insulator can be used as a substrate to fabricate MOS transistors

Q11. What are the benefits of SOI technology relative to conventional bulk CMOS technology?

Answer:
Benefits of SOI technology relative to convent : Benefits of SOI technology relative to conventional silicon al silicon (bulk CMOS):

- Lowers parasitic capacitance due to isolation from the bulk silicon, which improves power consumption and thus high speed performance.
- Reduced short channel effects
- Better sub Better sub-threshold slope. threshold slope.
- No Latch up due to BOX (buried oxide).
- Lower Threshold voltage.
- Reduction in junction depth leads to low leakage current.

- Higher Device density.

Q12. What are the basic assumptions of the fluid model?

Answer:
There are two basic assumptions as follows: : There are two basic assumptions as follows: **(a)** Electrical charge is considered as fluid, which can move from one place to another depending on the difference in their level, of one from the other, just like a fluid.
(b) Electrical potentials can be mapped into the geometry of a container, in which the fluid can move around.

Q13. Explain the function of a MOS transistor in the Explain the function of a MOS transistor in the nonsaturation saturation mode using the fluid model mode using the fluid model.

Answer:
Gate voltage higher than the threshold voltage : Gate voltage higher than the threshold voltage and the drain d the drain voltage is slightly higher than source voltage. In such a situation, as the drain voltage is increased the slope of the fluid flowing out increases indicating linear increase in the flow of current.

Q14. Explain the three modes of operation of a MOS transistors ransistors.

Answer:
The three modes are:
(a) Accumulation mode when Accumulation mode when Vgs is much less than is much less than Vt.
(b) Depletion Depletion mode when mode when Vgs is equal to is equal to Vt.
(c) Inversion Inversion mode when mode when Vgs is greater than is greater than Vt.

Q15. What are the three regions of operation of a MOS transistor?

Answer:
The three regions are:
- **Cut-off region:** This is essentially the accumulation mode, where there is no effective flow of current between the source and drain.
- **Non-saturated region:** This is the active, active, linear or week inversion region, where the drain current is dependent on both the gate and drain voltages.
- **Saturated region:** This is the strong inversion region, where the drain current is independent of the drain drain current is independent of the drain-to-source voltage but urce voltage but depends on the gate voltage.

Q16. What is the threshold voltage of a MOS transistor? How it varies with the body bias?

Answer:
One of the parameters that characterizes the switching behavior of a MOS transistor is its threshold voltage Vt. This can be defined as the gate voltage at which a MOS transistor begins to conduct.

Q17. What is channel length modulation effect? How the voltage current characteristics are affected because of this effect?

Answer:
It is assumed that channel length remains constant as the drain voltage is increased appreciably beyond the on set of saturation. As a consequence, the drain current remains constant in the saturation region. In practice, however the channel length shortens as the drain voltage is inccreased. For long channel lengths, say more than 5μm, this variation of length is relatively very small compared to the total length and is of little consequence. However, as the device sizes are scaled down, the variation of length becomes more and more predominant and should be taken into consideration. As a consequence, the drain current increases with the increase in drain voltage even in the saturation region.

Q18. What is body effect? How does it influences the threshold voltage of a MOS transistor?

Answer:
All MOS transistors are usually fabricated on a common substrate and substrate (body) voltage of all devices is normally constant. However, as we shall see in subsequent chapters, when circuits are realized using a number of MOS devices, several devices are connected in series. This results in different source potentials for different devices. It may be noted that the threshold voltage Vt is not constant with respect to the voltage difference between the substrate and the source of the MOS transistor. This is known as the substrate-bias effect or body effect. Increasing the Vsb causes the channel to be depleted of charge carries and this leads to increase in the threshold voltage.

Q19. What is transconductance of a MOS transistor? Explain its role in the operation of the transistor.

Answer:
Trans-conductance is represented by the change in drain current for change in gate voltage for constant value of drain voltage. This parameter is somewhat similar to β, the current gain of bipolar junction transistors. The following equation shows the dependence of on various parameters. As MOS transistors are voltage controlled devices, this parameter plays an important role in identifying the efficiency of the MOS transistor.

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{DS}=V_{DS}} = \frac{i_d}{v_{gs}}$$

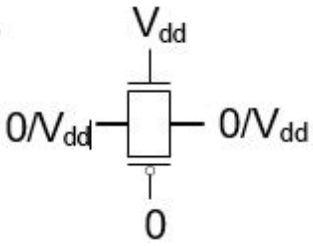
$$= (\mu_n C_{ox})\left(\frac{W}{L}\right)(V_{GS} - V_{th}) = (\mu_n C_{ox})\left(\frac{W}{L}\right)V_{OV}$$

$$= \sqrt{2(\mu_n C_{ox})\left(\frac{W}{L}\right)I_D}$$

$$= \frac{2I_D}{V_{ov}}$$

Q20. How one nMOS and one pMOS transistor are combined to behave like an ideal switch.

Answer:
To overcome the limitation of either of the transistors, one pMOS and one nMOS transistor can be connected in parallel with complementary inputs at their gates. In this case we can get both LOW and HIGH levels of good quality at the output. The low level passes through the nMOS switch and HIGH level passes through the pMOS switch without any degradation as shown in the figure



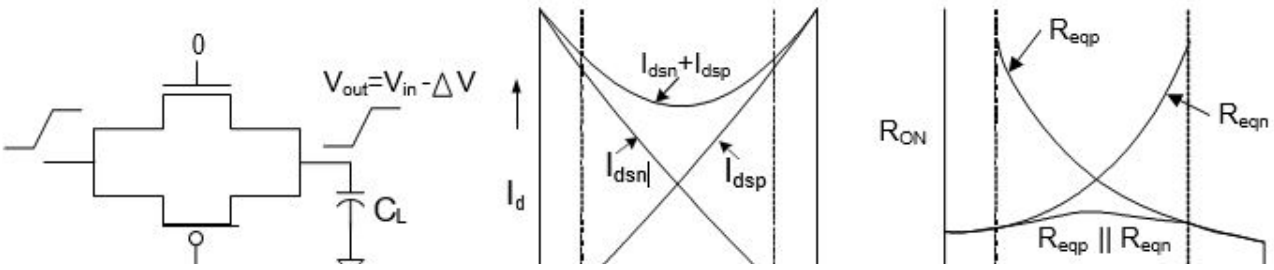
Q21. The input of a lightly loaded transmission gate is slowly changes from HIGH level to LOW level. How the currents through the two transistors vary?

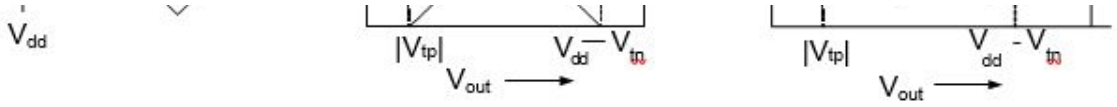
Answer:
Another situation is the operation of the transmission gate when the output is lightly loaded (smaller load capacitance). In this case, the output closely follows the input. In this case the transistors operate in three regions depending on the input voltage as follows:

- Region I: nMOS non-saturated, pMOS cut-OFF.
- Region II: nMOS non-saturated, pMOS non-saturated.
- Region III: nMOS cut off, pMOS non-saturated.

Q22. How its ON-resistance of a transmission gate changes as the input varies from 0 V to Vdd, when the output has a light capacitive load.

Answer:
The variation of ON resistance is shown in the figure. The parallel resistance remains more or less constant.

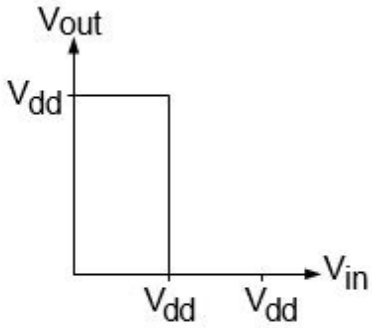


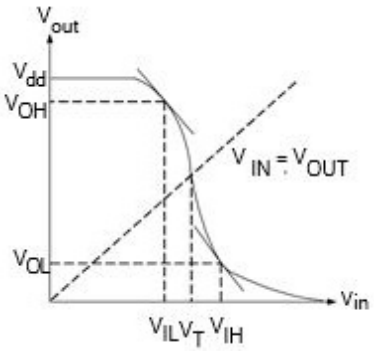


Q23. Draw the ideal characteristics of a CMOS inverter and compare it with the actual characteristics.

Answer:

The ideal and actual characteristics are given below. In the ideal characteristics, the output voltage is Vdd for input voltage from o to Vdd/ and 0 for input voltage from Vdd/ to Vdd. This is not true in case of the actual characteristics as shown below.





Q24. Compare the characteristics of the different types of MOS inverters in terms of noise margin and power dissipation.

Answer:

Various characteristic parameters are compared in the following table:

Inverters	V_{LO}	V_{HI}	*Noise-margin*	*Power*
Resistor	Weak	Strong	Poor for Low	High
nMOS depletion	Weak	Strong	Poor for Low	High
nMOS enhancement	Weak	Weak	Poor for both Low and High	High
Psuedo-nMOS	Weak	Strong	Poor for Low	High

Q25. What is the inversion voltage of an inverter? Find out the inversion voltage of a CMOS inverter.

Answer:

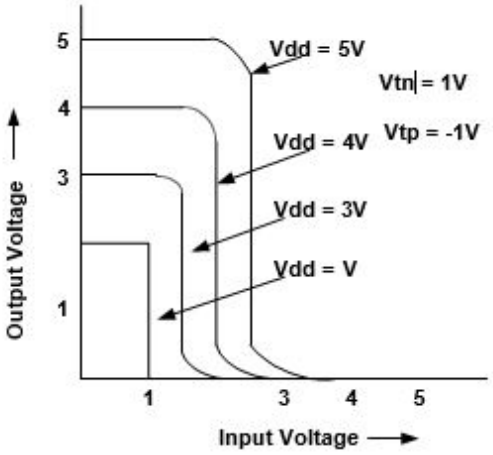
The inversion voltage Vinv is defined as the voltage at which the output voltage Vo is equal to the input voltage Vin. For a CMOS inverter it can be expressed in terms of the threshold voltages of the MOS

transistors and other parameters.

$$Vin = \frac{Vdd + Vtp + Vtn \cdot \sqrt{(\beta n / \beta p)}}{1 + \sqrt{(\beta n / \beta p)}}$$

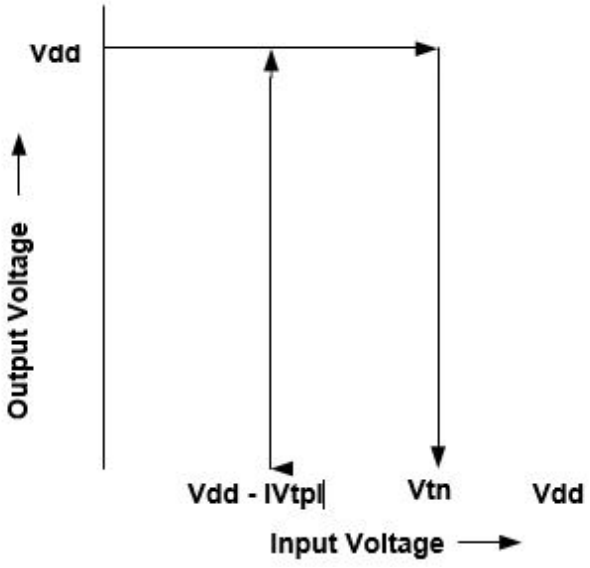
Q26. How the noise margin is affected by voltage scaling?

Answer:
As the supply voltage is reduced, the margin also decreases as shown in the figure.



Q27. What is the lower limit of supply voltage of a CMOS inverter. What happens if the supply voltage is further reduced?

Answer:
The lower limit of the supply voltage depends on the sum of the threshold voltages of the nMOS and the pMOS transistors. Vdd = Vtn +|Vtp|. As the supply voltage is reduced further, it leads to hysteresis in the transfer characteristic.



Q28. What is sheet resistance? Find out the expression of the resistance of rectangular sheet in terms of sheet resistance.

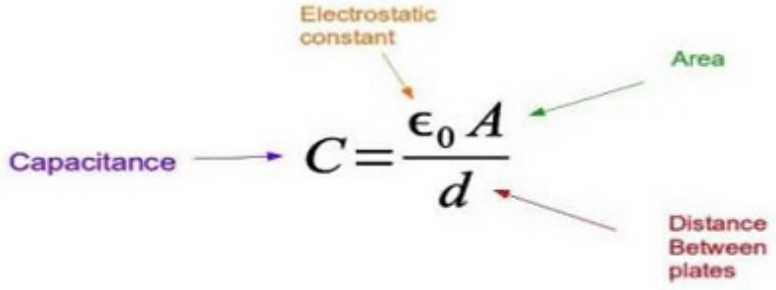
Answer:
The sheet resistance is defined as the resistance per unit area of a sheet of material. Consider a rectangular sheet of material with Resistivity = □, Width = W, Thickness = t and Length = L. Then, the resistance between the two ends is

$$R = R_{sh}\frac{L}{W} \text{ ohms}$$

$$R = \rho\frac{L}{A} = \rho\frac{L}{Wt} = \frac{\rho}{t}\frac{L}{W} \text{ Ohms}$$

Q.29 Find out the capacitance of a MOS capacitor.

Answer:
The capacitance of a parallel plate capacitor is given by



Q30. Explain the basic concept of super buffer.

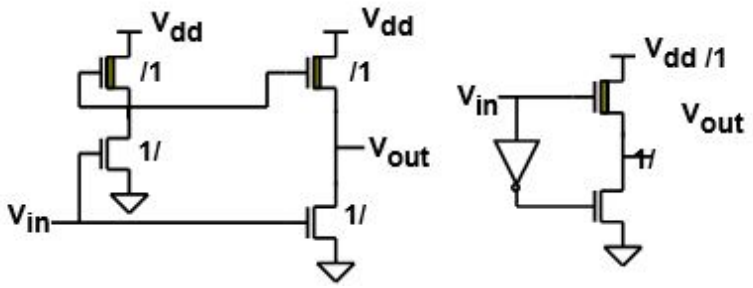
Answer:
There are situations when a large load capacitance such as, long buffers, off-chip capacitive load, or I/O buffer are to be driven by a gate. In such cases, the delay can be very high if driven by a standard gate. Limitations of driving by a simple nMOS inverter is the asymmetric drive capability of pull-up and pull-down devices (ratioed logic). Moreover, when the pull-down transistor is ON, the pull-up transistor also remains ON. So, the pull-down transistor should also sink the current of the pull-up device. Although this limitation is overcome in CMOS circuits, there is asymmetry in drive capability of pull-up and pull-down devices having the same minimum size

Q.31 Draw the schematic diagram of an inverting and non-inverting super-buffers and explain its operation.

Answer:

Answer:

The schematic diagrams of the super buffers are given below.

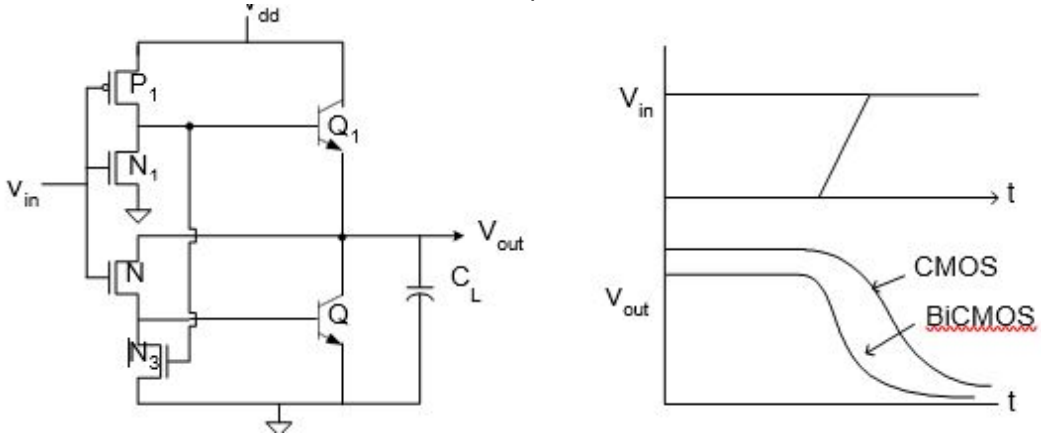


The average of the saturation currents for Vds = 5V and linear current for Vds = .5V is approximately 4.4 βpu for the standard inverter. On the other hand the, for the super-buffer, the average current is 19.06 βpu, which is 4 times that of standard inverter. Thus, the pull-up device is capable of sourcing about four times the current of the standard nMOS inverter.

Q32. Give the schematic diagram of a Bi-CMOS inverter. Explain its operation. Compare the switching characteristics of a BiCMOS inverter with respect to that for static CMOS for different fan out conditions.

Answer:

The schematic diagram of a BiCMOS inverter is given below. Higher current drive capability of bipolar NPN transistors is used in realizing bi-CMOS inverters. The delays of CMOS and BiCMOS inverters are compared for different fan-outs. It may be noted that for fan-out of 1 or CMOS provides smaller delay compared to BiCMOS. However, as fan-out increases further, BiCMOS performs better and better.



Q33. How the transfer characteristic of a CMOS NAND gate is affected with increase in fan-in?

Answer:

Transfer characteristic does not remain symmetric with increase in fan-in of the NAND gate. The inversion voltage moves towards right with the increase in fan-in.

Q34. How the transfer characteristic of a CMOS NOR gate is affected with increase in fan-in?

Answer:

Answer:
In case of NOR gate the transfer characteristic also does not remain symmetric and the inversion voltage moves towards left with the increase in fan-in.

Q35 How switching characteristic of a CMOS NAND gate is affected with increase in fan-in?

Answer:
When the load capacitance is relatively large, the fall time increases linearly with the increase in fan-in and the rise time is not affected much.

Q36. How switching characteristic of a CMOS NOR gate is affected with increase in fan-in?

Answer:
When the load capacitance is relatively large, the rise time increases linearly with the increase in fan-in and the fall time is not affected much. For the same area, NAND gates are superior to NOR gates in switching characteristics because of higher mobility of electrons compared holes. For the same delay, NAND gates require smaller area than NOR gates

Q37. How noise margin of a CMOS NAND/NOR gate is affected with increase in fan-in?

Answer:
Because of the change in the inversion voltage, the noise margin is affected with the increase in fan-in. For equal fan-in, noise margin is better for NAND gates compared to NOR gates. We may conclude that for equal area design NAND gates are faster and better alternative to NOR gates

Q38. For a complex/compound CMOS logic gate, how do you realize the pull-up and the pull-down networks?

Answer:
A CMOS logic gate consists of a nMOS pull-down network and a pMOS pull-up network. The nMOS network is connected between the output and the ground, whereas the pull-up network is connected between the output and the power supply. The nMOS network corresponds to the complement of the function either in sum-of-product or product-of-sum forms and the pMOS network is dual of the nMOS network .

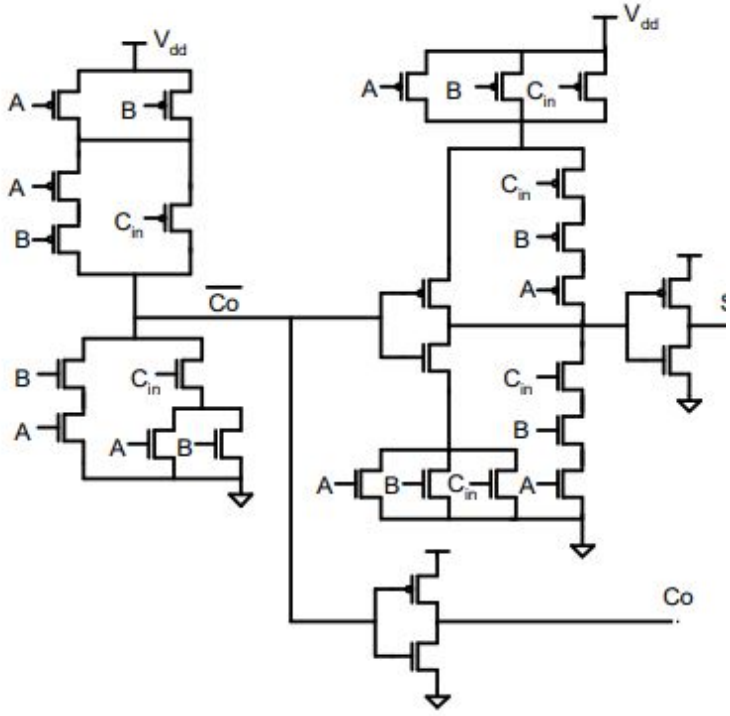
Q.39 Give the two possible topologies AND-OR-INVERT AND-OR- INVERT (AOI) and OR-AND-INVERT (OAI) to realize CMOS logic gate. Explain with an example.

Answer:

The AND-OR-INVERT network corresponds to the realization of the nMOS network in sum-of-product form. Where as the OR- AND-INVERT network corresponds to the realization of the nMOS network in product-of-sum form. In both the cases, the pMOS network is dual of the nMOS network .

Q40. Give the AOI and OAI realizations for the sum and carry functions of a full adder.

Answer:
AOI form of realization is shown in the figure.



Q41. How do you realize pseudo nMOS logic circuits. Compare its advantage and disadvantages with respect to standard static CMOS circuits.

Answer:
In the pseudo-nMOS realization, the pMOS network of the static CMOS realization is replaced by a single pMOS transistor with its gate connected to GND. An n-input pseudo nMOS requires n+1 transistors compared to n transistors of the corresponding static CMOS gates. This leads to substantial reduction in area and delay in pseudo nMOS realization. As the pMOS transistor is always ON, it leads to static power dissipation when the output is LOW.

Q42. In what way relay logic circuits differ from pass transistor logic circuits? Why the output of a pass transistor circuit is not used as a control signal for the next stage?

Answer:
Logic functions can be realized using pass transistors in a manner similar to relay contact networks.

However, there are some basic differences as mentioned below:
(a) In relay logic, output is considered to be '1' when there is some voltage passing through the relay logic. Absence of voltage is considered to be '0'. On the other hand, is case of pass transistor logic it is essential to provide both charging and discharging path for the output load capacitance.
(b) There is no voltage drop in the relay logic, but there is some voltage drop across the pass transistor network.
(c) Pass transistor logic is faster than relay logic.

Q43. What are the advantages and limitations of pass transistor logic circuits? How the limitations are overcome?

Answer:
Pass transistor realization is ratioless, i.e. there is no need to have L:W ration in the realization. All the transistors can be of minimum dimension. Lower area due to smaller number of transistors in pass transistor realization compared to static CMOS realization. Pass transistor realization also has lesser power dissipation because there is no static power and short-circuit power dissipation in pass transistor circuits. The limitations are (a) Higher delay in long chain of pass transistors (b) Multi-threshold Voltage drop (Vout = Vdd – Vtn) (c) Complementary control signals and (d) Possibility of sneak path because of the presence of path to Vdd and GND.

Q44. Why is it necessary to insert a buffer after not more than four pass transistors in cascade?

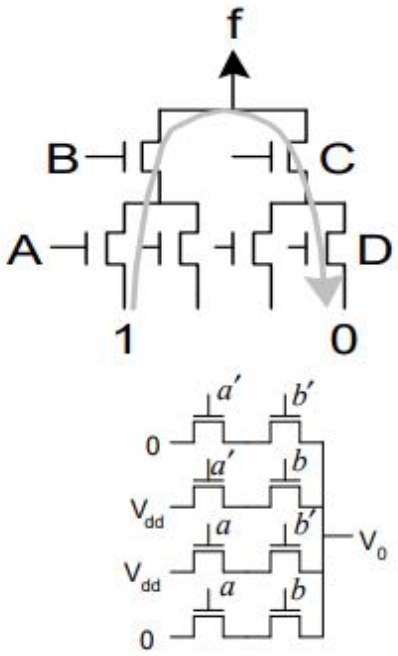
Answer:
When a signal is steered through several stages of pass transistors, the delay can be considerable. For n stages of pass transistors, the delay is given by the relationship. $\tau = CR_{eq}\frac{n(n+1)}{2}$ To overcome the problem of long delay, buffers should be inserted after every three or four pass transistor stages.

Q45. Why is it necessary to have swing restoration logic in pass transistor logic circuits? Explain its operation.

Answer:
In order to avoid the voltage drop at the output (Vout = Vdd – Vtn) , it is necessary to use additional hardware known swing restoration logic at the gate output. At the output of the swing restoration logic there is rail to rail voltage swing. The swing restoration can be done using a pMOS transistor with its gate connected to GND.

Q46. What is the 'sneak path' problem of pass transistor logic circuits? How sneak path is avoided in Universal Logic Module (ULM) based realization of pass transistor network. Illustrate with an example.

Answer:
As shown in the figure, the output is connected to both ‘1’ (Vdd) and ‘0’(GND). The output attains some intermediate Value between Vdd and GND. The MUX based realization allows connection of the output to only one input, which can be either 0 or 1.
Multiplexer realization of Is shown in the figure.

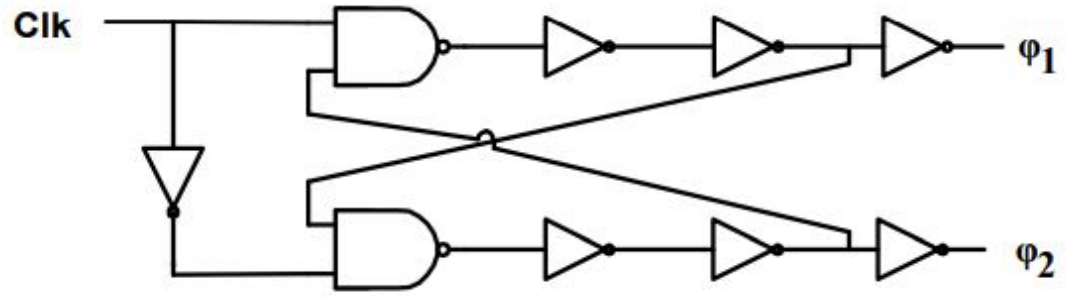


Q47. Explain the basic operation of a 2-phase dynam phase dynamic circuit? ic circuit?

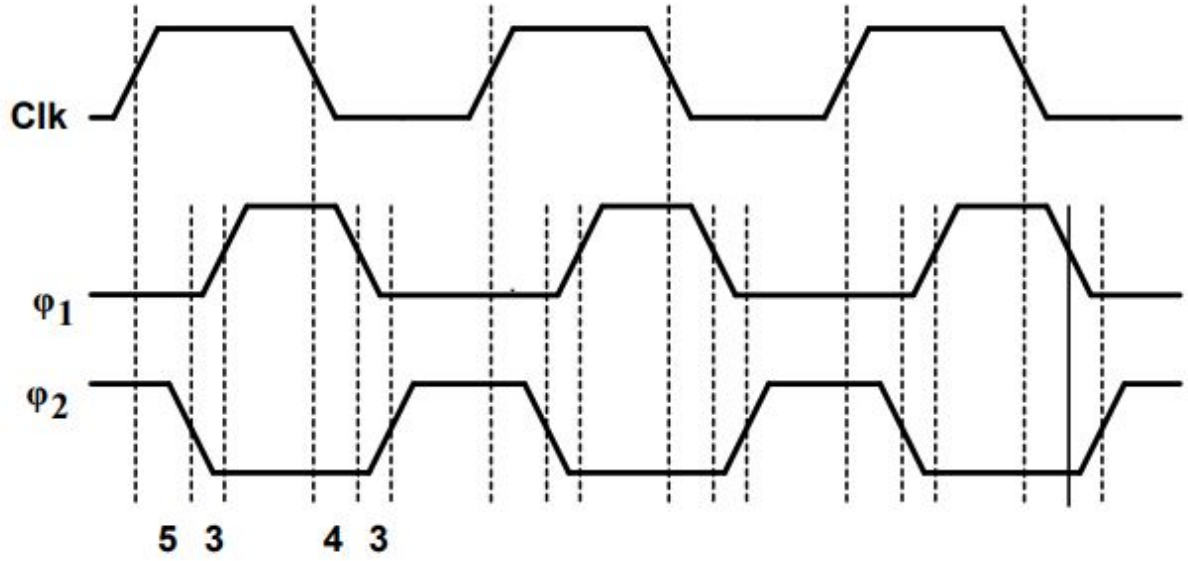
Answer:
The operation of the circuit can be explained : The operation of the circuit can be explained using precharge precharge logic in which the output is logic in which the output is precharged precharged to HIGH level during to HIGH level during φ2 clock and the clock and the output is evaluated during output is evaluated during φ1 clock 1 clock.

Q48. How phase clocks can be generated using inverters?

Answer:
As shown below, two phase clock can generated using inverters. The timing diagram is given in the next slide.



Timing diagram of the two-phase clock generated from a single-phase clock.



Q49. What makes dynamic CMOS circuits faster than static CMOS circuits?

Answer:
As MOS dynamic circuits require lesser number of transistors and lesser capacitance is to be driven by it. This makes MOS dynamic circuits faster.

Q50. Compare the sources of power dissipation between static CMOS and dynamic CMOS circuits?

Answer:
In both the cases there is switching power and leakage power dissipations. However, the short circuit and glitching power dissipations, which are present in static CMOS circuits, are not present in dynamic CMOS circuits.

Q51. What is charge leakage problem of dynamic CMOS circuits? How is it overcome?

Answer:
The source-drain diffusions form parasitic diodes with the substrate. There is reverse bias leakage current .The current is in the range 0.1nA to 0.5nA per device at room temperature and the current doubles for every 10°C increase in temperature . This leads to slow but steady discharge of the charge on the capacitor, which represent information. This needs to be compensated by refreshing the charge at regular interval.

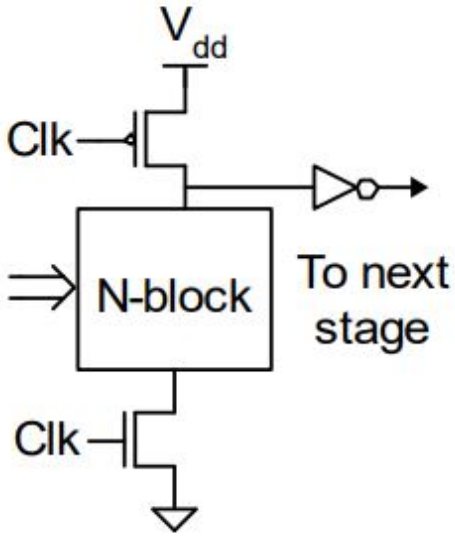
Q52. Explain the clock skew problem of dynamic CMOS circuits?

Answer:

Clock skew problem arises because of delay due to resistance and parasitic capacitances associated with the wire that carry the clock pulse and this delay is approximately proportional to the square of the length of the wire. When the clock signal reaches a later stage before its preceding stage, the precharge phase of the preceding stage overlaps with the evaluation phase of the later stage, which may lead to premature discharge of the load capacitor and incorrect output during evaluation phase

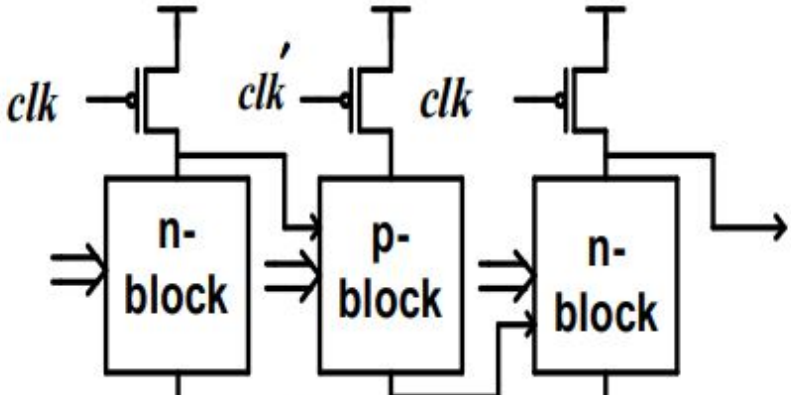
Q53. How clock skew problem is overcome in in domino CMOS circuits?

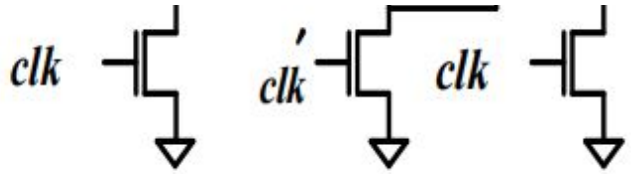
Answer:
In domino CMOS circuits the problem is overcome by adding an inverter as shown in the diagram. It consists of two distinct components: The first component is a conventional dynamic CMOS gate and the second component is a static inverting CMOS buffer. During precharge phase, the output of the dynamic gate is high, but the output of the inverter is LOW.As a consequence, it cannot drive an nMOS transistor ON. So, the clock skew problem is overcome.



Q54. How clock skew problem is overcome in in NORA CMOS circuits?

Answer:
The problem can be overcome using NORA logic, nMOS and pMOS transistor networks are alternatively used. The output of an nMOS block is HIGH during precharge, which cannot turn a pMOS transistor ON. Similarly, the output of an pMOS block is LOW during precharge, which cannot turn a nMOS transistor ON.

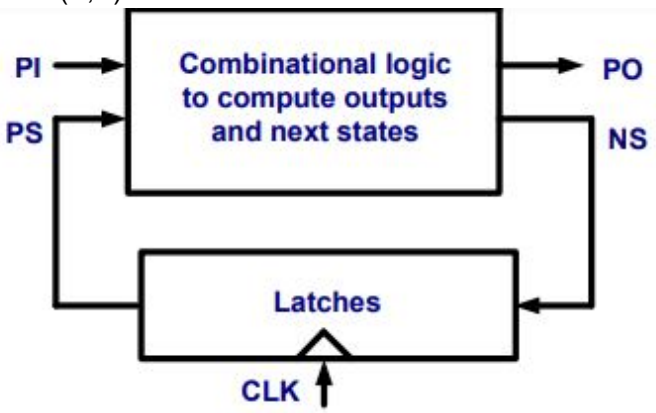




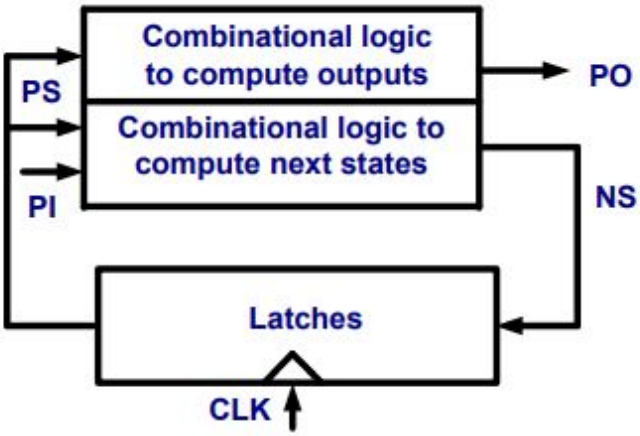
Q55. Distinguish between Mealy and Moore machines.

Answer:

In a Mealy machine the outputs are dependent on the inputs and present state. The Output transition function is represented by Z = λ(S,X).



Where as in a Moore machine the outputs are dependent only on present state. The output transition function is represented by Z = λ((S)



Q56. List various sources of leakage currents.

Answer:

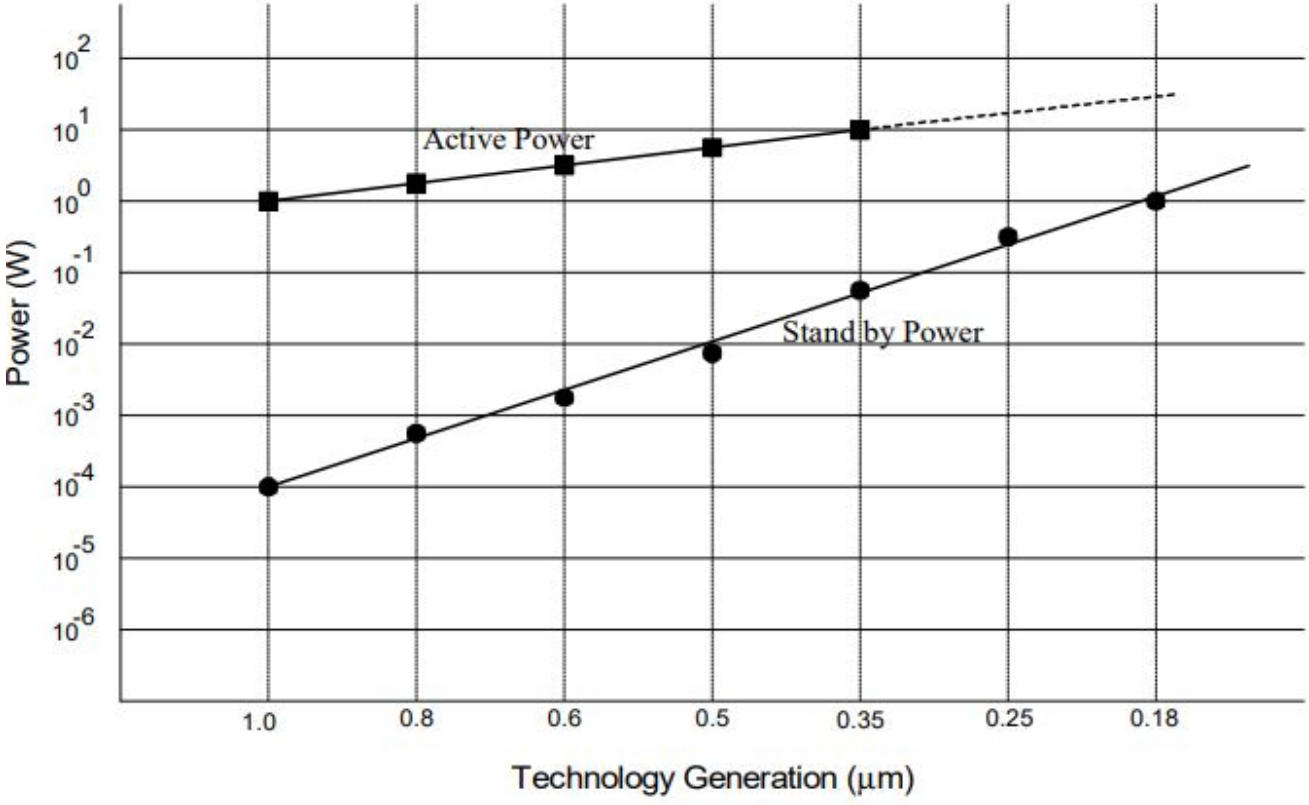
Various sources of leakage currents are listed : Various sources of leakage currents are listed below:

- I1= Reverse = Reverse-bias p-n junction diode leakage current n junction diode leakage current
- I2 = Band-to-band tunneling current band tunneling current
- I = Subthreshold leakage current
- I3 = Subthreshold leakage current
- I4 = Gate Oxide tunneling current
- I5 = Gate current due to hot Gate current due to hot-carrier injection carrier injection
- I6 = Channel punch Channel punch-through through

- I6 = Channel punch Channel punch through through
- I7 = Gate induced drain Gate induced drain-leakage current leakage current

Q57. Why leakage power is an important issue in deep submicron technology?

Answer:
In deep submicron technology, the leakage component is a significant % of total power as shown in the diagram. Moreover, the leakage current is increasing at a faster rate than dynamic power. As a consequence, it has become an important issue in DSM.



Q58. What is band-to-band tunneling current?

Answer:
When both n regions and p regions are heavily doped, a high electric field across a reverse biased p high electric field across a reverse biased p-n junction causes nction causes significant current to flow through the junction due to tunneling of electrons from the valence bond of the p of electrons from the valence bond of the p-region to the to the conduction band of n conduction band of n-region. This is known as band region. This is known as band-to-band tunneling.

Q59. What is body effect?

Answer:
As a negative voltage is applied to the substrate with respect to the source, the well respect to the source, the well-to-source junct source junction the device is ion the device is reverse biased and bulk depletion

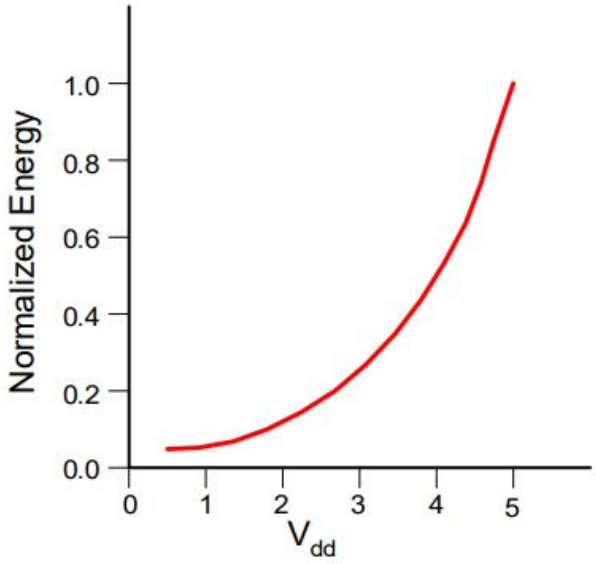
the well-to-source junct source junction the device is ion the device is reverse biased and bulk depletion region is widened. This leads to increase the threshold voltage. This effect is known as body effect.

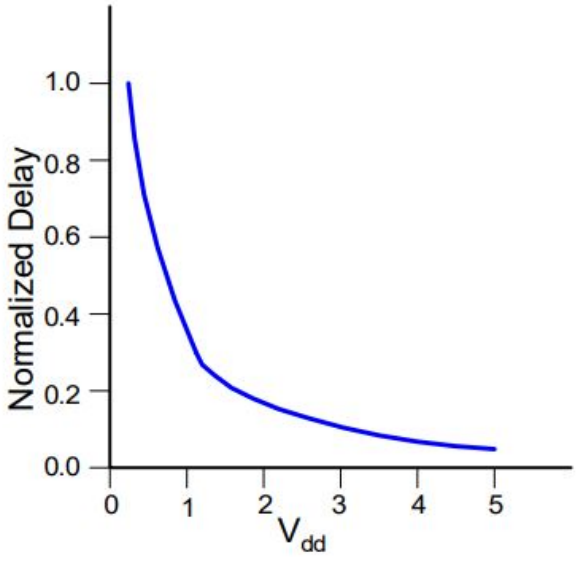
Q60. What is subthreshold leakage current? Briefly discuss various mechanisms responsible for this leakage current?

Answer:
The subthreshold subthreshold leakage current in CMOS circuits is due leakage current in CMOS circuits is due to carrier diffusion between the source and the drain regions of the transistor in weak inversion, when the gate voltage is below Vt. The behavior of an MOS transistor in the subthreshold operating region is similar to a bipolar device, and the region is similar to a bipolar device, and the subthreshold hreshold current exhibits an exponential dependence on the gate voltage. The amount of the The amount of the subthreshold subthreshold current may become significant current may become significant when the gate when the gate-to-source voltage is smaller than source voltage is smaller than, but very close , but very close to the threshold voltage of the device.

Q61. Explain the basic concepts of supply voltage scaling.

Answer:
Power dissipation is proportional the square of the supply voltage. So, a factor of two reduction in supply voltage yields a factor of four decrease in energy. But, as the supply voltage is reduced, delay increases as shown in the diagram. So, the challenge is to scale down the supply voltage without compromise in performance.





Q62. As you move to a new process technology with a scaling factor S = 1.4, how the drain current, power dissipation, power density, delay and energy requirement changes for the constant field scaling?

Answer:
Drain current reduces by a factor of S. Although po ough power dissipation decreases by a factor of S^2, the

Drain current reduces by a factor of S. Although po ough power dissipation decreases by a factor of S^2 , the power density remains the same. The delay decreases by a factor of S and the energy decreases by a factor of S^3 .

Quality	Before Scaling	After Scaling
Gate Capacitance	C_g	$C'_g = C_g / S$
Drain Current	I_D	$I'_D = I_D / S$
Power Dissipation	P	$P' = P / S^2$
Power Density	P/ Area	$P' / Area' = (P / Area)$
Delay	t_d	$t'_d = t_d / S$
Energy	$E = P.t_d$	$E' = \frac{P}{S^2} \times \frac{t_d}{S} = \frac{P.t_d}{S^3} = \frac{1}{S^3} E$

Q63. Distinguish between constant field and constant voltage feature size scaling? Compare their advantages and disadvantages.

Answer:

In this approach the magnitude of all the inte : In this approach the magnitude of all the internal electric fields l electric fields within the device are preserved, while the dimensions are scaled down by a factor of S. This requires that all potentials must be scaled down by the same factor. Accordingly, supply as well as threshold voltages are scaled down proportionately. But, in constant constant-voltage scaling, all the device dimension voltage scaling, all the device dimensions are scal s are scaled down by a factor of S just like constant down by a factor of S just like constant-voltage s voltage scaling, supply caling, supply voltage and threshold voltages are not scaled.

Q64. Compare Compare the constant constant field and constant constant voltage voltage scaling scaling approaches approaches in terms of area, delay, energy and power density density parameters parameters.

Answer:

Quality	Cons field Scaling	Constant Voltage Scaling
Gate Capacitance	$C'_g = C_g / S$	$C'_g = C_g / S$
Drain Current	$I'_D = I_D / S$	$I'_D = I_D.S$
Power Dissipation	$P' = P / S^2$	$P' = P.S$
Power Density	$P' / Area' = (P / Area)$	$P' / Area' = S^3 P / Area$

Delay	$t_d' = t_d / S$	$t_d' = t_d / S^2$
Energy	$E' = \frac{P}{S^2} \times \frac{t_d}{S} = \frac{P.t_d}{S^3} = \frac{1}{S^3} E$	$E' = E / S$

Q65. Explain how parallelism can be used to achieve low power instead of high performance in realizing digital circuits.

Answer:
Traditionally, parallelism is used to improve performance at the expense of larger power dissipation. But, instead of trying to improve performance, the power dissipation can be reduced by scaling down the supply voltage such that the performance remains unaltered.

Q66. Explain how multicore architecture provides low power compared to the single core architecture of the same performance.

Answer:
The idea behind the parallelism for low-power can be extended to multi-core architecture. The clock frequency can be reduced with commensurate scaling of the supply voltage as the number of cores is increased from one to more than one while maintaining the same throughput.

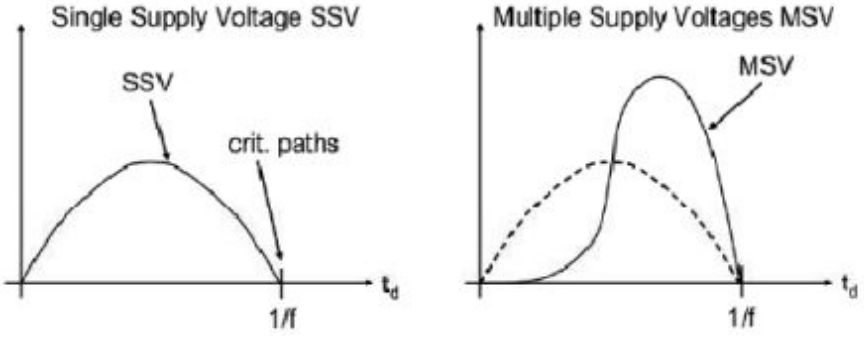
Q67. Explain the basic concept of multi level voltage scaling.

Answer:
This is an extension of SVS where two or few fixed voltage domains are used in different parts of a circuit,. As we know, high Vdd gates have less delay, but higher dynamic and st gates have less delay, but higher dynamic and static power dissipation and low power dissipation and low Vdd gates have larger delay but gates have larger delay but lesser power dissipation. Voltage islands can be generated at different levels of granularity, such as macro level and standard cell level. The slack of the off cell level. The slack of the off-critical path can critical path can be utilized for be utilized for allocation of macro modules of low allocation of macro modules of low-Vdd to off-critical critical-path macro modules. Total power dissipation can be reduced without degrading the overall circuit performance.

Q68. What is the impact of multiple supply voltages on the distribution of path delays of a circuit with respect to that for single supply voltage?

Answer:
Path delay for different paths in a circuit for single supply voltage is shown. The graph of a Gaussian is a characteristic symmetric "bell curve" shape that quickly falls off towards plus/minus infinity plus/minus infinity. However, when multiple supply voltages are used, the path delay distribution is not Gaussian because

modules having smaller delays are assigned with smaller supply voltage and their delay increases.



Q69. List and explain the important issues in the context of multiple supply voltage scaling?

Answer:
Important issues in the context of MVS are listed below:

- Voltage Scaling Interfaces
- Converter Placement
- Floor planning, Routing and Placement
- Multiple Supply Voltages
- Static Timing Analysis
- Power up and Power down Sequencing
- Clock distribution

Q70. What problem arises when a signal passes from low voltage domain to high voltage domain? How this problem is overcome?

Answer:
A high-level output from the low level output from the low-Vdd domain has output domain has output VddL, which may turn on both , which may turn on both nMOS and pMOS transistors of the transistors of the high-Vdd domain inverter resulting in short circuit between VddH to GND. A level converter needs to be inserted to avoid this static power consumption

Q71. Explain the design decision for the placement of converters in the voltage scaling interfaces.

Answer:
One important design decision in the voltage : One important design decision in the voltage scaling interfaces is the placement of converters . As the high the high-to-low level converters use low low level converters use low-Vdd voltage voltage rail, it is a appropriate to place them in the receiving or destination domain. It is also recommended to place the low place the low-to-high level converters in the r high level converters in the receiving eceiving domain. As the low domain. As the low-to-high level converters req high level converters require both low and high both low and high-Vdd supply rails, at least one of the supply rails, at least one of the supply rails needs to be routed from one domain to the other.

Q72. What problem arises when a signal passes from low voltage domain to high voltage domain? How this problem is overcome?

Answer:
A high-level output from the low level output from the low-Vdd domain has output domain has output VddL, which may turn on both , which may turn on both nMOS and pMOS transistors of the transistors of the high-Vdd domain inverter resulting in short circuit between VddH to GND. A level converter needs to be inserted to avoid this static power consumption