STA Numericals

Refer to **setup and hold** page to view STA basics and some more solved problems.

Problem 1:

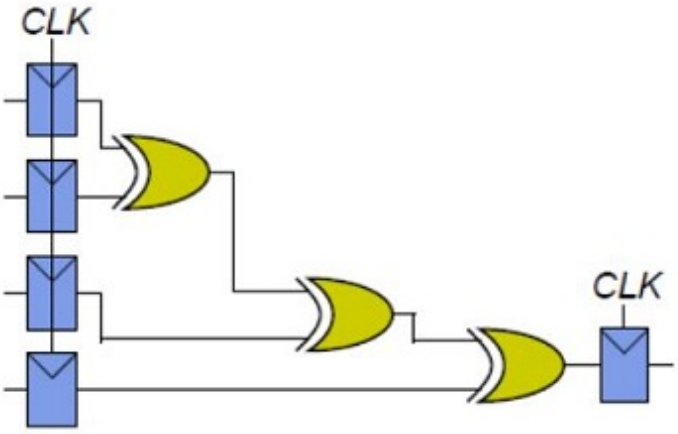
In the following circuit

Each flip flop has:

- Setup time of 60ps
- Hold time of 20ps
- Clock-to-Q maximum delay of 70ps
- Clock-to-Q minimum delay of 50ps

Each XOR gate has:

- Propagation delay of 100ps
- Contamination delay of 55ps



a. If there is no clock skew, what is the maximum operating frequency of this circuit?
b. How much clock skew can the circuit tolerate before it might experience a hold time violation?
c. Redesign the circuit so that it can be operated at 3GHz frequency. How much clock skew can your circuit tolerate before it might experience a hold time violation?

Solution

a.

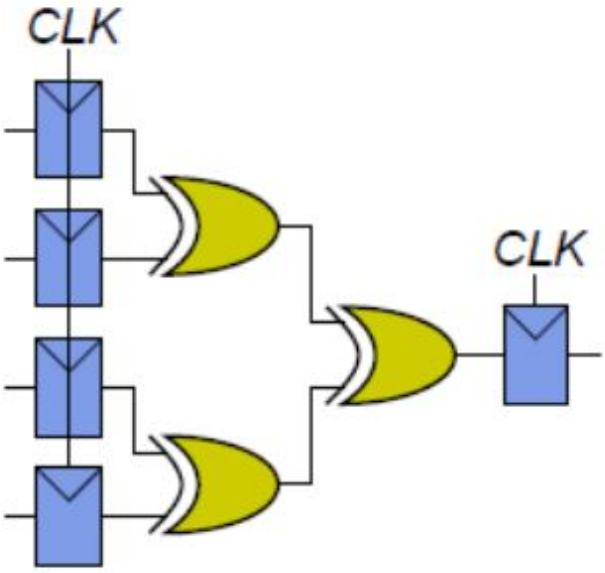
Tc ≥ Tpcq + Tpd + Tsetup
Longest path:
Tc ≥ Tpcq + 3*Tpd + Tsetup
Tc ≥ 70 + 3*100 + 60 = 430 ps
Max Frequency = 1/Tc = 2.33 GHz

b.

Tccq + Tcd≥Thold + Tskew
Shortest Path:
Tccq + Tcd ≥ Thold + Tskew
50 + 55 ≥ 20 + Tskew
Tskew ≤ 85 ps

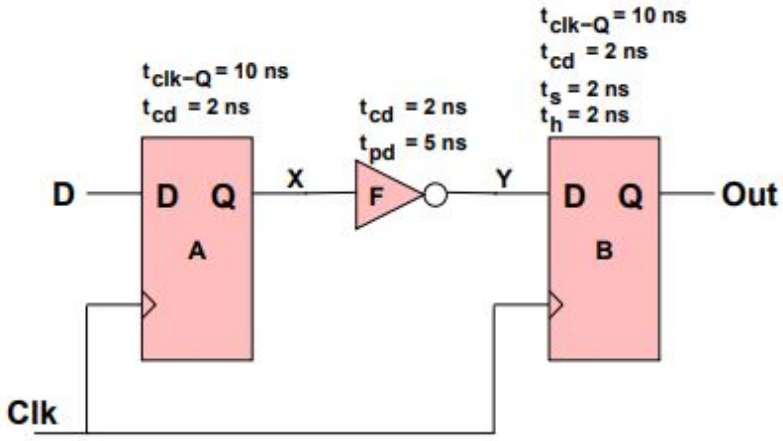
c.

Tc ≥ Tpcq + 2*Tpd + Tsetup + Tskew
Tc ≥ 330 + Tskew
Tccq + 2Tcd ≥ Thold + Tskew
Tskew≤ 140 ps



Problem 2:

Q. Determining the Max. Clock Frequency for a Sequential Circuit.



Solution

Before starting timing analysis, consider the flow of data in this circuit in response to a rising clock edge, starting at flip-flop A.

1. Following the rising clock edge on Clk, a valid output appears on signal X after tClk−Q = 10 ns.

2. A valid output Y appears at the output of inverter F, tpd = 5 ns after a valid X arrives at the gate. 3. Signal Y is clocked into flip-flop B on the next rising clock edge. This signal must arrive at least ts = 2ns before the rising clock edge.

As a result, the minimum clock period, Tmin of the circuit is:

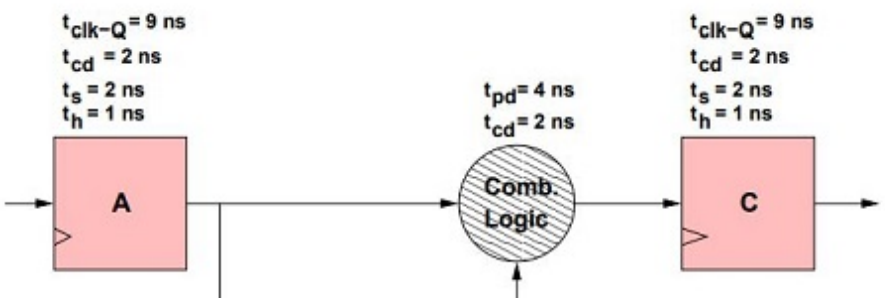
Tmin = tClk − Q(A) + tpd(F) + ts(B)

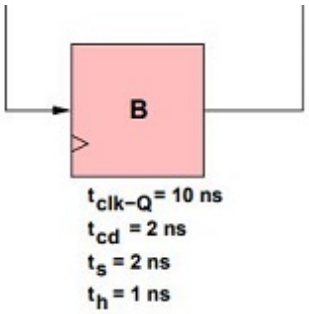
= 10ns + 5ns + 2ns = 17ns

maximum clock frequency of the circuit is 1/Tmin = 1/17ns = 58.8 MHz

Problem 3:

Q. Determining the Max. Clock Frequency the Sequential circuit shown below.





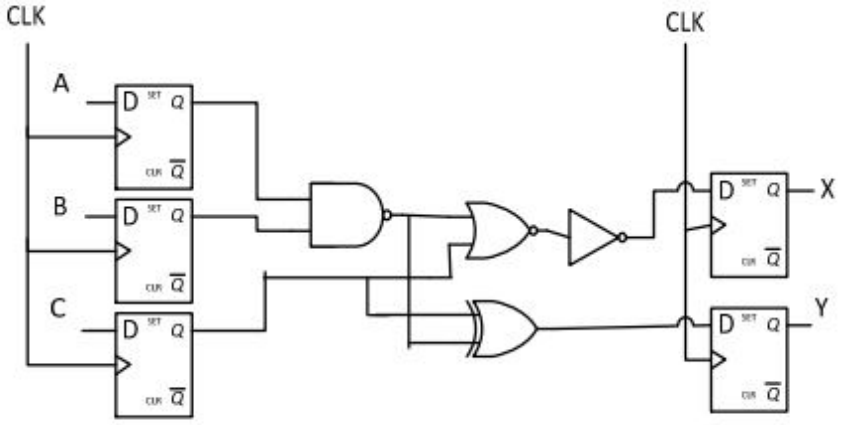
In a typical sequential circuit design there are often millions of flip-flop to flip-flop paths that need to be considered in calculating the maximum clock frequency. This frequency must be determined by locating the longest path among all the flip-flop paths in the circuit. For example, consider the circuit shown in above. there are three flip-flop to flip-flop paths (flop A to flop B, flop A to flop C, flop B to flop C),the delay along all three paths are:

TAB = tClk−Q(A) + ts(B) = 9 ns + 2 ns = 11 ns
TAC = tClk−Q(A) + tpd(Z) + ts(C) = 9 ns + 4 ns + 2 ns = 15 ns
TBC = tClk−Q(B) + tpd(Z) + ts(C) = 10 ns + 4 ns + 2 ns = 16 ns

Since the TBC is the largest of the path delays, the minimum clock period for the circuit is Tmin = 16 ns and the **maximum clock frequency** is 1/Tmin = 62.5 MHz.

Problem 4:

Q. For the circuit given below calculate.
• Maximum clock frequency for reliable operation.
• The amount of clock skew the circuit can tolerate if it needs to operate at 5 Ghz.
• How much clock skew the circuit can tolerate before it experiences a hold time violation?



Gate	Tpd(ps)	Tcd(ps)
2-input NAND	20	15
2-input NOR	30	20
2-input XOR	60	40
NOT	15	10

Flip-Flop (clock-to-q) propagation delay (tpcq) = 35 ps
Flip-Flop (clock-to-q) contamination delay (tccq) = 20 ps
Flip-Flop data setup time (ts) = 30 ps
Flip-Flop data hold time (th) = 10 ps

Solution

a.

Period > (FF propagation delay) + (max combination circuit delay) + (FF Setup time) + (max clock skew)
Period > 35 + (60+20) + 30 +0 ps
Period > 145 ps

F < 1/(145 ps)
F < 6.8965 GHz.

b.

At F= 5 GHz Period = 1/(5 Ghz) = 200 ps.
Max clock skew = Clock period – (FF propagation delay + max combination circuit delay + FF Setup time)
Max clock skew = 200 – (35 + (60+20) + 30) = 200 – 145 = 55 ps.

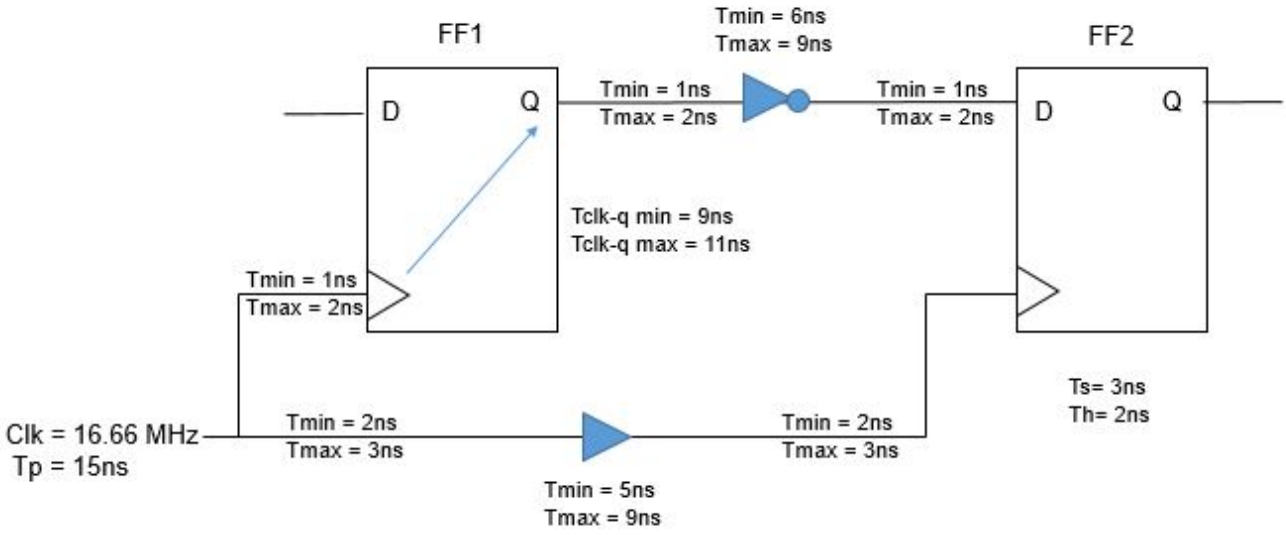
c.

For hold time violation to NOT occur.
Hold time <= (FF contamination delay) + (min combinational circuit delay) - (max clock skew)
So hold time will get violated when
Max clock skew > (FF contamination delay) + (min combinational circuit delay) – (Hold Time)
Max clock skew > 20 + (20+10) – 10
Max clock skew > 40 ps

Problem 5:

Q. For the circuit given below calculate.

a. setup slack
b. hold slack



Solution

before proceeding with the solution we should know :

setup slack = RTmin(minimum required time) - ATmax(maximum arrival time)
where; RTmin ≥ ATmax to satisfy setup time

Hold Slack = ATmin(minimum arrival time) - RTmax(maximum arrival time)

where; ATmax ≥ RTmin to satisfy hold time

Let's solve this..

a. Setup Slack

ATmax = 2 + 11 + 2 + 9 + 2 + 3 = 29ns
RTmin = 2+ 5 + 2 + 15(here 15ns is the time perid) = 24ns

Setup slack = ATmax - RTmin = 24 - 29 = -5ns

we can see setup is violating as ATmax is less than RTmin.

b. Hold Slack

ATmin = 1 + 9 + 1 + 6 + 1 - 2 (here Thold is considered and subtracted) = 16ns
RTmax = 3 + 9 + 3 = 15ns

Hold Slack = ATmin - RTmax = 16 - 15 = 1ns

here ATmax ≥ RTmin i.e 16 ≥ 15 (no violation)