



ECE 2285

Project #1 Power Supply Simulation

Learning Objectives:

- Design a regulated, DC 10V power supply to maintain output voltage for a specified load with provision for a missing load.

Requirements:

- Design a 10 V, Zener-diode-regulated, DC power supply capable of supplying an average of 10.0 V to a 1 k Ω load resistor and not exceeding rated maximum or minimum Zener diode currents at any time, including when the load resistor is absent.
- The input to the Zener diode voltage regulator will be modeled as a 17 VAC sinusoid at 60 Hz.
- Use a BZX84C10LT Zener diode (a surface mount device made by On semiconductor and having a model available in LTspice).
- The average power dissipation of the zener diode much not exceed its rated value of 250 mW with some safety margin.

Background Information:

DC power supplies are extremely common in the world of electronics. They are used for almost every type of electronic equipment (i.e. computers, TVs, stereos, cell phones, etc.). In addition to requiring a DC voltage, most equipment requires that the voltage be well-controlled or regulated.

A block diagram and waveforms for a simple power supply are shown below in **Fig.1**. The following circuit components staged together as shown in **Fig. 1** make a DC power supply:

- **Transformer** - The transformer provides the necessary voltage reduction for the DC circuit as well as isolation from the AC line. We will omit the transformer and use an AC (i.e., sinusoidal) voltage source as a substitute.
- **Rectifier** - A full-wave bridge rectifier will be employed to convert the AC output from the transformer to DC. The full-wave bridge rectifier converts both positive and negative voltage portions of a sinusoid into a positive voltage, causing less droop in a voltage regulator.
- **Filter** - Filtering will be required to limit the voltage ripple out of the rectifier. If the bridge-rectifier output is fed into a capacitor, the capacitor charges up to the peak voltage (minus two diode voltage drops of about 1.4 V) and acts like a battery when the bridge-rectifier output starts to drop. The voltage on the capacitor droops (or ripples) slightly while it supplies current to power the voltage regulator, however. The larger the capacitor, the smaller the ripple.
- **Regulator** - An ideal regulator provides a constant voltage regardless of the load on the power supply. Your voltage regulator must provide the specified level of regulation (see "Requirements", above) under no-load and full-load conditions.

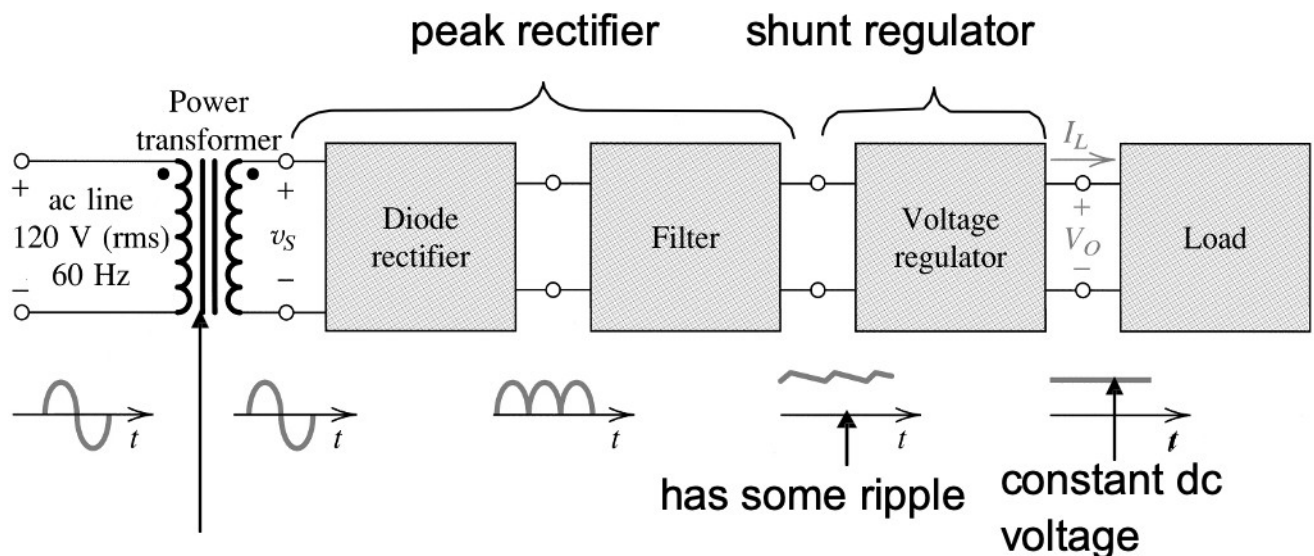
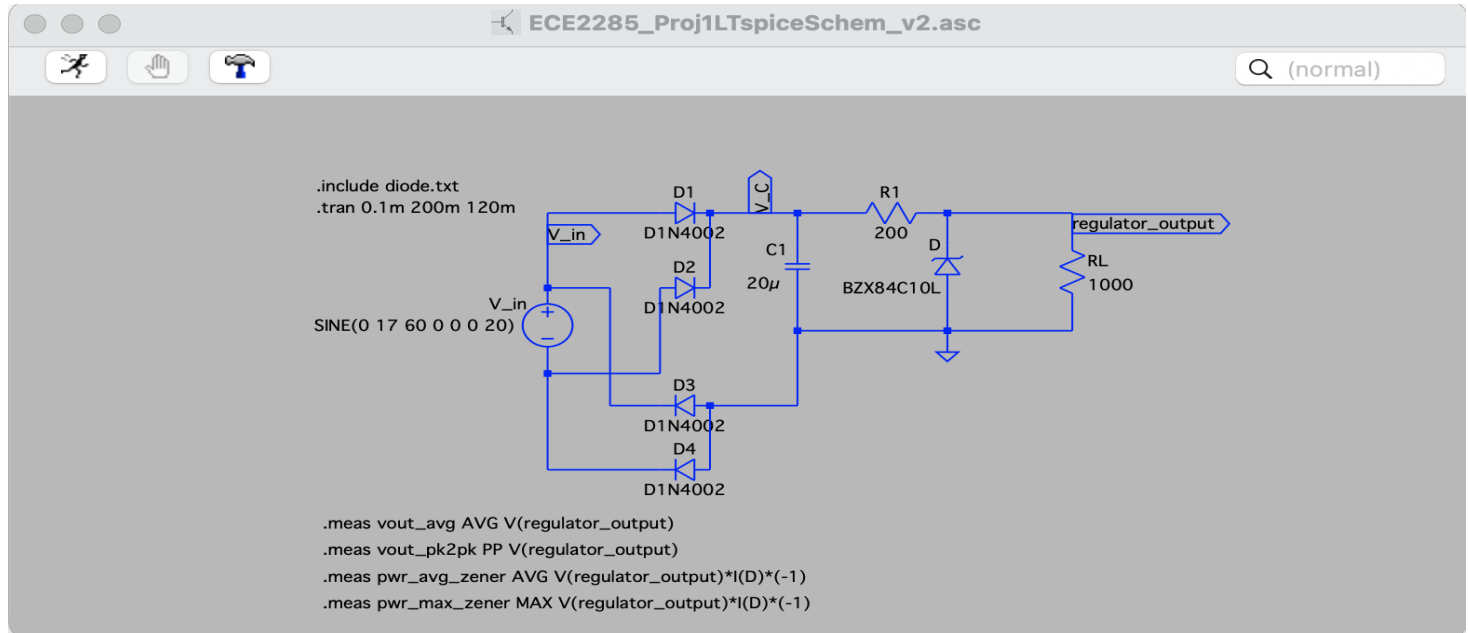


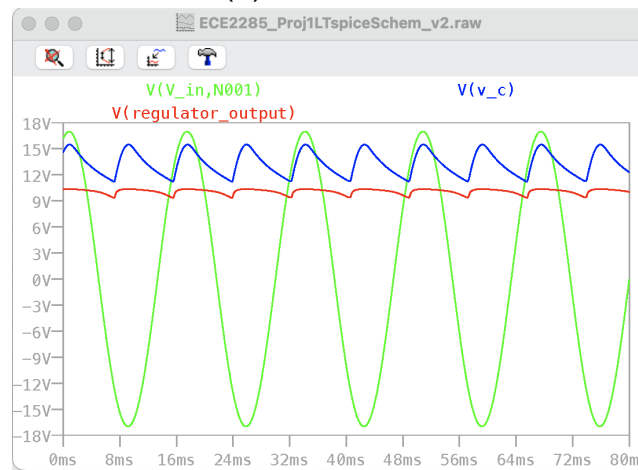
Fig. 1: Power Supply Block Diagram

Overview of Circuit Components for Power Supply:

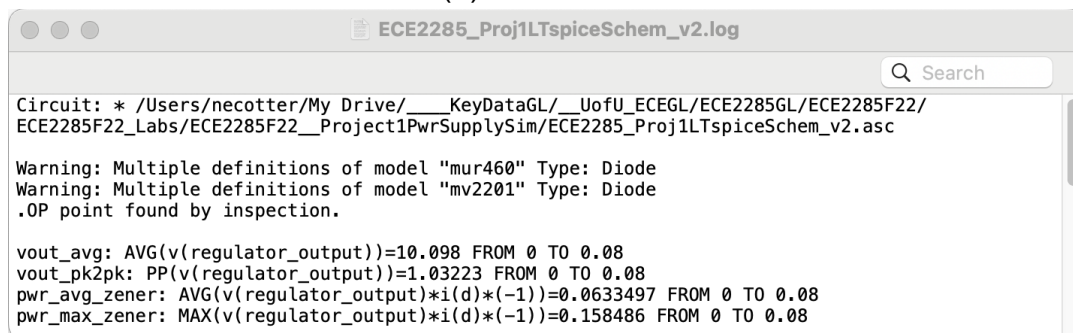
A schematic that we will use as a starting point for the design and simulation of the power supply circuit is shown below in **Fig. 2**, along with waveforms and measured values. The circuit uses a bridge rectifier.



(a) Schematic



(b) Waveforms



(c) Measurements

Fig. 2: Power Supply Schematic, waveforms, and measurements.

The following circuit components staged together as shown in **Fig. 2** make up our model circuit:

- Transformer (modeled as AC V-source) - Because transformers tend to be close to ideal and are difficult to model in LTspice, you will use an ideal voltage source in the analysis and simulation to “model” the transformer. Use an amplitude of 17 Volts for the sinusoidal input at a 60Hz frequency. Note that 17 VAC is the approximate amplitude for a sinusoidal waveform with a root-mean-square (rms) value of $12\text{V} = 17 / \sqrt{2}$. The factor of square-root of two is used to calculate what DC voltage would give the same average power as a sinusoid, given that power is proportional to V^2/R and the average value of a sinusoid squared is 1/2 the amplitude squared. AC voltage values are usually given in rms volts.
- Rectifier - For analysis, you may assume the bridge rectifier consists of diodes having an $V_D = 0.8\text{ V}$ drop. For simulation, you will use a full-wave rectifier made from the generic diode model in LTspice, unless you wish to use one of the models built into LTspice or drawn from the diode.txt file linked in this project assignment. The 1N4001 diode is recommended. If you use a particular diode from the diode.txt file, be sure to put the diode.txt file in the same folder as your .asc LTspice file. Then invoke the diode model you want by typing its exact name as the value of the diode. If you were to build the power supply, you should also check that the peak current rating for the diodes is not exceeded.
- Filter - You should require one capacitor for the finished circuit. For analysis, you may assume an ideal capacitor. For simulation, you may use a generic capacitor. Note that polarity of electrolytic capacitors is important if you build the power supply!
- Regulator - You will use a BZX84CL10L Zener diode made by On Semiconductor. See datasheet linked on this assignment page, and look for the row with an arrow for specs specific to this 10V Zener diode. The next section on *Design Analysis* goes into more detail.
- Resistors - Very important: note that resistors (and capacitors) only come in discrete values, with the step sizes depending on the % tolerance. For your final design and simulation, use standard 5% resistors, and use a standard capacitor value of 1, 2.2, 3.3, or 4.7 times some power of 10 in Farads.

(70 pts) **Design Analysis:**

The analysis and design of the power supply starts at the output and works backwards. The first step is to analyze the Zener diode voltage regulator to determine the maximum allowable capacitor-voltage ripple it can tolerate, and the second step is to size the capacitor to achieve that ripple constraint.

The output voltage is determined by the Zener diode, as shown in Fig. 3, and will be close to the desired 10 V value if the current flowing in the Zener diode circuit remains in the operating range for current, I_Z , specified on the Zener diode's datasheet. The design focuses on the effects of the V_{in} ripple, but another concern (addressed later) is whether the Zener diode will be damaged if R_L is missing.

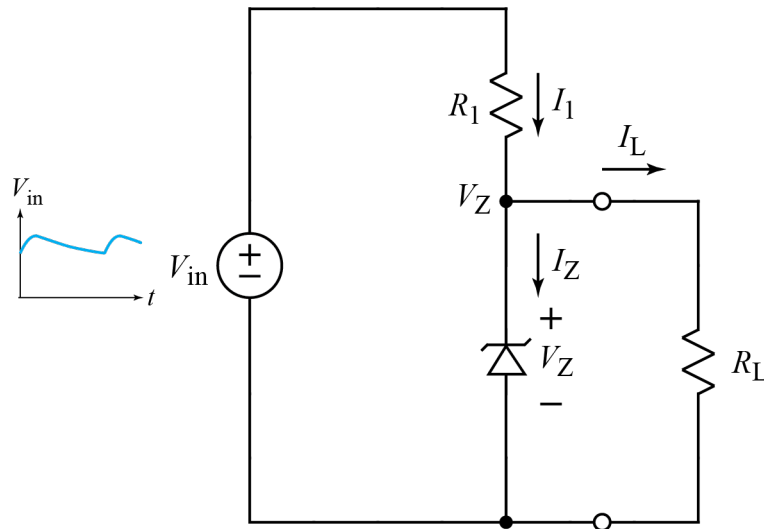


Fig. 3: Zener diode circuit.

The design approach presented here employs a voltage-source model of the Zener diode and superposition, as shown in Fig. 4. The Zener voltage source, V_{ZT} , has the nominal voltage of 10.0 V.

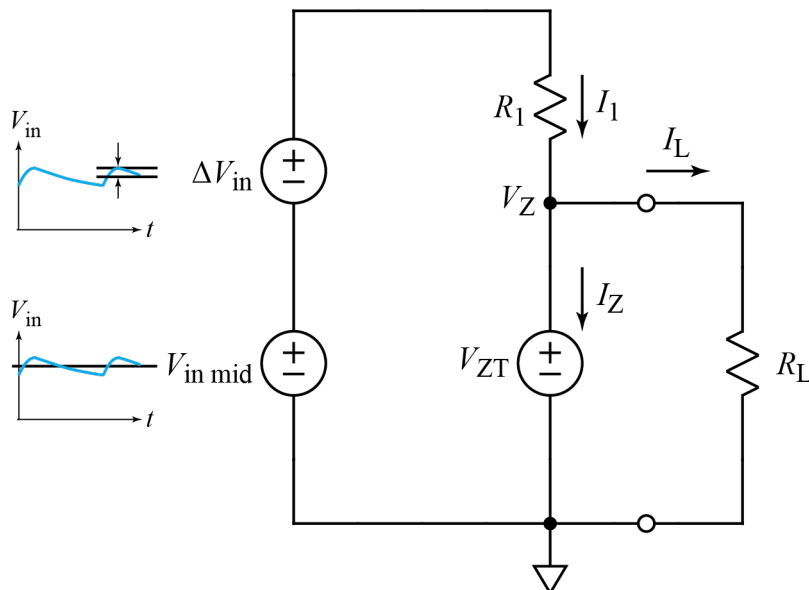


Fig. 4: Superposition V-src model for Zener diode circuit.

For the superposition, we treat the rippling capacitor voltage that feeds the circuit as a DC voltage source, V_{in_mid} , plus an "AC" voltage source, ΔV_{in} . The "AC" is in quotes here because the ripple is not a sinusoid. Nevertheless, we may use superposition to break our analysis down into a DC case plus an "AC" small-signal ripple case.

The following sections proceed through the design analysis process in steps. Insert your responses where indicated. The basic approach is to first determine a formula for the value of R_1 that gives the optimal current in the Zener diode for exactly a 10 V output for DC input voltage V_{in_mid} . Then we find the change in Zener current as a function of both R_1 and the size of the ripple voltage, $\pm \Delta V_{in}$. Keeping the Zener in its proper operating region gives a constraint on the maximum allowable ripple and the maximum value of R_1 . Finally, we use a filter capacitor large enough to limit the ripple to less than the maximum allowable value.

- 1) (5 pts) Characterize allowed current changes for the Zener diode. Fig. 5 shows the Zener diode i-v curve we use for design. The model is a reverse voltage drop, $V_{ZT} = 10V$. This model is only valid between some minimum and maximum Zener diode current. Use the On Semi datasheet for the BZX84C10L to find a values you can use for the minimum current limit. Here are some hints for determining the value:
 - The first columns on the datasheet are for the desired operating point of the Zener diode where its voltage is the most accurate. From the first section we deduce that the ideal operating current is $I_{Z0} = 5 \text{ mA}$.
 - The columns to the right of the first section on the datasheet are for min, max, or other operating conditions. In the absence of better information, we may use the smallest operating current listed on the datasheet as our I_{ZK} .
 - The precise *maximum* Zener diode current is missing from the datasheet, but the highest current shown on the datasheet is 20 mA. This value is the same for most of the Zener diodes, which means it is probably not the exact maximum but rather a convenient number for the datasheet. However, we will use $I_{ZT3} = 20 \text{ mA}$ as the maximum current for lack a better value.

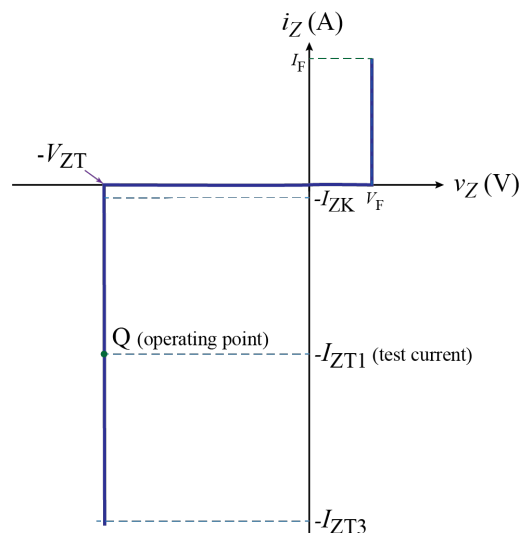


Fig. 5: Zener diode characteristic curve.

Insert your value for minimum Zener diode current, I_{ZK} , here. Explain how you chose this value.

The data sheet for the BZX84C10L provides the ideal operating current, I_{ZKT1} , to be 5 mA. We have already selected the maximum current to be 20 mA. The only other operating conditions specified are the ones provided for I_{ZK2} , which is 1 mA. Therefore, our I_{ZK} , is 1 mA. It also stands to reason that if 5 mA is the ideal operating current and 20 mA is the maximum, then $\text{min} < \text{ideal} < \text{max}$ or $1 \text{ mA} < 5 \text{ mA} < 20 \text{ mA}$.

Using the above information, write the value of $-\Delta I_Z = I_{ZK} - I_{ZT1}$, the maximum allowable negative deviation of Zener diode current from the optimal value of I_{ZK} , here:

$$\begin{aligned} -\Delta I_Z &= I_{ZK} - I_{ZT1} \\ -\Delta I_Z &= 1 \text{ mA} - 5 \text{ mA} = -4 \text{ mA} \\ \Delta I_Z &= 4 \text{ mA} \end{aligned}$$

Using the above information, write the value of $+\Delta I_Z = I_{ZK} - I_{ZT3}$, the maximum allowable positive deviation of Zener diode current from the optimal value of I_{ZK} , here:

$$\begin{aligned} +\Delta I_Z &= I_{ZK} - I_{ZT3} \\ +\Delta I_Z &= 1 \text{ mA} - 20 \text{ mA} = -19 \text{ mA} \\ +\Delta I_Z &= 19 \text{ mA} \end{aligned}$$

Set ΔI_Z to the smaller magnitude of the $-\Delta I_Z$ and $+\Delta I_Z$ values. List the value of ΔI_Z here: (Note that we use a positive value for ΔI_Z .)

$$\Delta I_Z = 4 \text{ mA}$$

- 2) (10 pts) Write an equation for R_1 in terms of DC input voltage V_{in_mid} . The design specification says that the average V_{in} (which we take to be V_{in_mid}) should result in exactly 10V across an ideal load resistor, $R_L = 1k\Omega$. Thus, the design should result in optimal current $I_{ZT1} = 5\text{ mA}$ in the Zener diode when V_{in} equals V_{in_mid} .

Using the superposition circuit diagram shown in Fig. 6, write an equation for R_1 as a function of V_{in_mid} and component values, as needed. Hints: Use a current summation at the V_{ZT} node. Then use Ohm's law. The final equation is fairly simple.

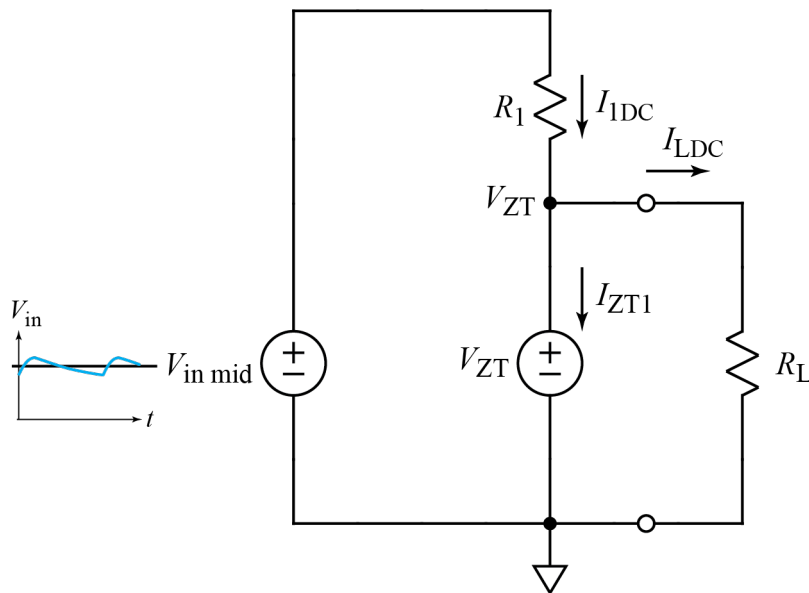


Fig. 6: DC superposition circuit for Zener regulator.

Insert your derivation of the equation for R_1 in terms of V_{in_mid} here:

2) Derive R_1 as a function of V_{in_mid}

$V_{RL} = 10\text{ V}$
 KCL at Node V_{ZT}
 $\sum I_{in} = \sum I_{out}$
 4) $I_{IDC} = I_{LDC} + I_{ZT1}$
 $\frac{V_{in_mid} - 10\text{ V}}{R_1} = 5\text{ mA} + 10\text{ mA}$
 $\frac{V_{in_mid} - 10\text{ V}}{R_1} = 15\text{ mA}$
 $R_1 = \frac{V_{in_mid} - 10\text{ V}}{15\text{ mA}}$

$I_{LDC} = \frac{V_{ZT} - 0\text{ V}}{R_L}$
 1) $I_{LDC} = \frac{10\text{ V}}{1\text{ k}\Omega} = 10\text{ mA}$
 2) $I_{ZT1} = 5\text{ mA}$
 3) $I_{IDC} = \frac{V_{in_mid} - V_{ZT}}{R_1}$
 $I_{IDC} = \frac{V_{in_mid} - 10\text{ V}}{R_1}$

- 3) (10 pts) Write an equation for ΔI_Z in terms of ΔV_{in} and R_1 . Fig. 7 shows the circuit for the "AC" portion of the superposition. We use $\pm \Delta V_{in}$ to denote the maximum deviations of V_{in} from the average value of V_{in_mid} . The ripple voltage, ΔV_{in} , will change the current flowing in the Zener diode, perturbing it from the optimal value of I_{ZT1} .

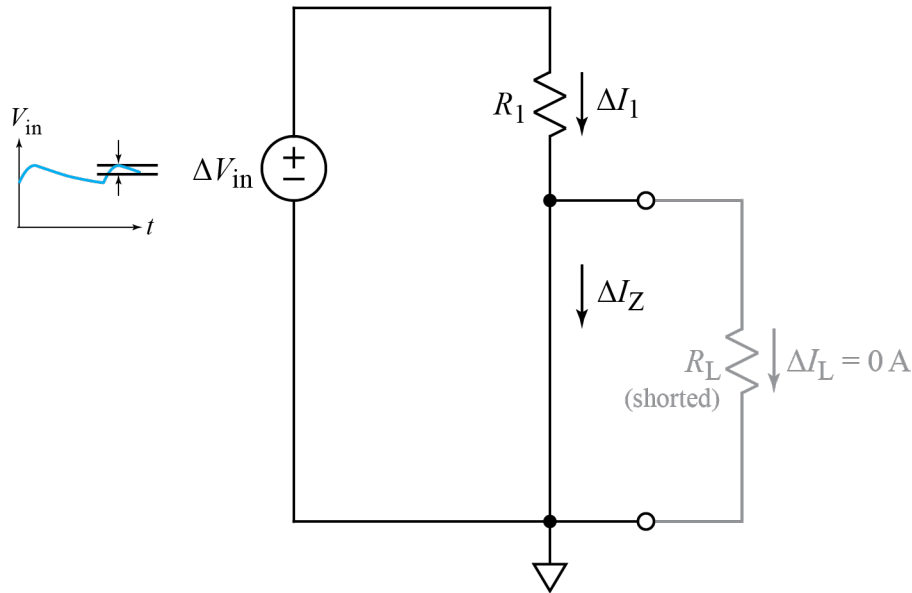


Fig. 7: AC superposition circuit for Zener regulator.

Write an equation for ΔI_Z in terms of ΔV_{in} and insert it here:

3) Derive ΔI_Z as a function of ΔV_{in}

$$\sum I_{in} = \sum I_{out}$$

$$\Delta I_1 = \Delta I_L + \Delta I_Z \quad \Delta I_L = 0A$$

$$\Delta I_1 = \Delta I_Z$$

$$\Delta I_Z = \frac{\Delta V_{in}}{R_1}$$

From previous

$$R_1 = \frac{V_{in_mid} - 10V}{15mA}$$

$$\Delta I_Z = \frac{\Delta V_{in}}{\frac{V_{in_mid} - 10V}{15mA}} = \Delta V_{in} \cdot \left(\frac{15E-3A}{V_{in_mid} - 10V} \right) [A]$$

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- 4) (25 pts) Solve for the maximum allowed ripple voltage, ΔV_{in} . The ripple voltage, ΔV_{in} , and the average input voltage, V_{in_mid} , sum to give the peak voltage of the input voltage, V_{in} , across the filtering capacitor.

$$V_{in_mid} + \Delta V_{in} = V_{in_pk}$$

This equation forms a bridge connecting the values of V_{in_mid} and ΔV_{in} to a known value of V_{in_pk} . That is, we know the value of V_{in_pk} is the peak transformer output voltage minus two diode-voltage drops.

$$V_{in_pk} = 17 \text{ V} - 2V_D$$

You may use a value of $V_D = 0.8 \text{ V}$ for the 1N4001 diodes in the bridge rectifier. Later on, you may improve the estimate of V_D if you wish.

$$V_{in_pk} = 17 \text{ V} - 2 \cdot 0.8 \text{ V} = 15.4 \text{ V}$$

Substituting this value gives the equation we need to complete the design.

$$V_{in_mid} + \Delta V_{in} = 15.4 \text{ V}$$

Using the preceding equation, known values from above, and the equations from parts (2) and (3), find the value ΔV_{in} . This is the maximum allowable ripple-voltage amplitude for V_{in} .

Insert your derivation of ΔV_{in} here. Show the derivation and the value you obtain. (Note that this is the maximum value allowed for ΔV_{in} .)

4) Solve for max ripple voltage ΔV_{in}

$$1) V_{in_{mid}} + \Delta V_{in} = 15.4V \quad 2) R_1 = \frac{V_{in_{mid}} - 10V}{15mA}$$

$$V_{in_{mid}} = 15.4V - \Delta V_{in}$$

$$\Delta I_Z = \frac{\Delta V_{in}}{R_1} = \Delta V_{in} \cdot \left(\frac{15mA}{V_{in_{mid}} - 10V} \right) \quad 3) \Delta I_Z = \frac{\Delta V_{in}}{R_1}$$

$$4mA = \Delta V_{in} \cdot \frac{15mA}{V_{in_{mid}} - 10V} \quad 4) \Delta I_Z = 4mA$$

$$4mA = \Delta V_{in} \cdot \frac{15mA}{(15.4V - \Delta V_{in}) - 10V} \Rightarrow 4mA = \Delta V_{in} \cdot \frac{15mA}{5.4V - \Delta V_{in}}$$

$$\frac{4mA}{15mA} = \frac{\Delta V_{in}}{5.4V - \Delta V_{in}} \Rightarrow \frac{4}{15} (5.4V - \Delta V_{in}) = \Delta V_{in} \Rightarrow$$

$$\frac{36}{25}V - \frac{4}{15}\Delta V_{in} = \Delta V_{in} \Rightarrow \frac{36}{25}V = \frac{19}{15}\Delta V_{in}$$

$$\Delta V_{in} \approx 1.136V$$

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Use the value of ΔV_{in} and your equations to solve for the maximum allowable value for R_1 and the minimum allowable value for $V_{in_{mid}}$. Show the derivations and the values you obtain here: (Note that a smaller value of R_1 or a higher value of $V_{in_{mid}}$ are viable for the design.)

4) Solve minimum allowable $V_{in_{mid}}$ and maximum allowable R_1
(Either smaller value of R_1 or higher value of $V_{in_{mid}}$ are viable.)

Let $\Delta V_{in} = +1.136V$

$$V_{in_{mid}} = 15.4V - (+1.136V)$$

$$V_{in_{mid}} = 14.264V$$

$$R_1 = \frac{14.264V - 10V}{15mA} = 284.26\Omega$$

Let $\Delta V_{in} = -1.136V$

$$V_{in_{mid}} = 15.4V - (-1.136V) = 16.536V$$

$$R_1 = \frac{16.536V - 10V}{15mA} = 435.73\Omega$$

$$\text{Let } V_{in_{mid}} = 14.264V, R_1 = 284.26\Omega$$

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- 5) (10 pts) The last design step is to determine the size of capacitor needed. We will assume that R_L is present. Fig. 8 shows the ripple waveform. The capacitor charges up as the input voltage peaks, but it discharges as it provides the current for the voltage regulator.

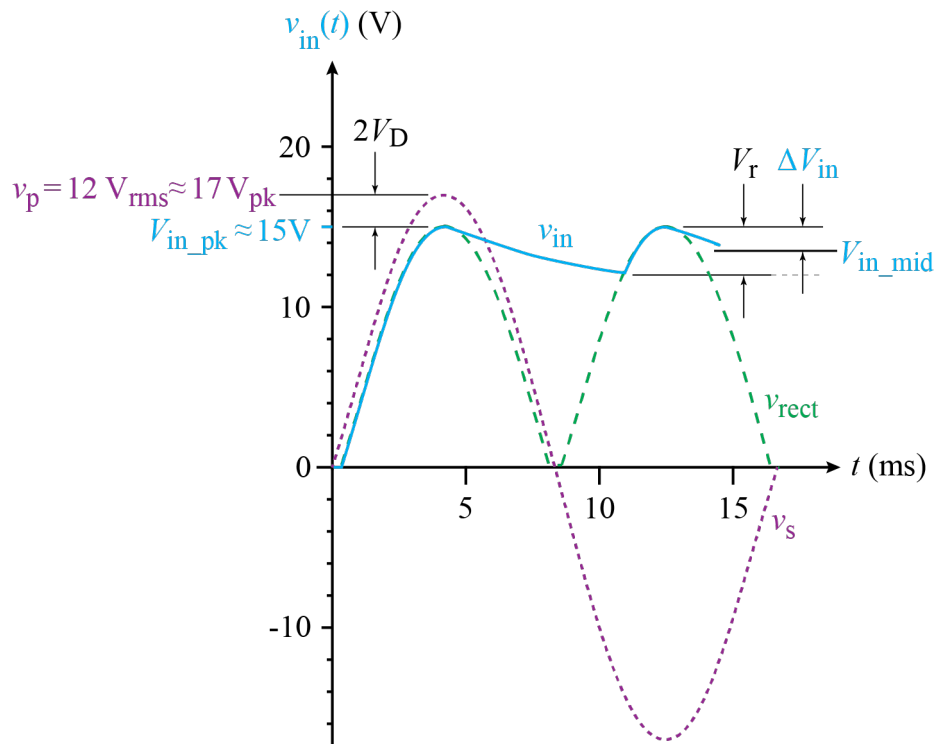


Fig. 8: Capacitor ripple voltage.

The calculation of the capacitor voltage is based on the equation relating charge to current and capacitance.

$$Q = CV$$

We express the total ripple, which is $2\Delta V_{in}$, in terms of the change in charge on the capacitor.

$$2\Delta V_{in} = \frac{1}{C} \Delta Q$$

The change in charge is calculated by integrating the current flowing out of the capacitor on each cycle of the transformer output voltage.

$$\Delta Q = \int_0^{\Delta t} i_C(t) dt$$

As indicated in Fig. 9, there are at least three progressively more accurate ways of calculating the time interval, Δt , and the current versus time, $i_C(t)$.

1. We may assume the current out of the capacitor is constant at the peak value until the next peak. This gives voltage V_{r1} in Fig. 9.

$$i_C(t) = \frac{V_{in.pk} - 2V_D - 10V}{R_L} \quad (\text{constant}) \quad \text{and} \quad \Delta t = \frac{1 \text{ sec}}{120}$$

This causes a linear drop in V_C with time. The change in Q is just I_C times Δt . The shortcoming of this method is that it is less accurate. The advantage of this method is that it is simple, and if the voltage droop is small it is quite accurate.

2. We may model the voltage regulator as a Thévenin equivalent and use an exponential RC solution until the next peak of the sinusoid input voltage. This gives voltage V_{re} in Fig. 9.

$$i_C(t) = \frac{V_{in_pk} - 2V_D - 10 \text{ V}}{R_1} e^{-\frac{t}{R_{Th}C}} \quad \text{and} \quad \Delta t = \frac{1 \text{ sec}}{120}$$

This causes an accurate drop in V_C with time. The shortcomings of this method are that it is more complicated and should stop when it hits the upward sinusoid. The advantage of this method is that it is straightforward, and if the voltage droop is small it is quite accurate.

3. We may model the voltage regulator as a Thévenin equivalent and exponential RC solution, as in (2), but stop the RC solution when it intersects with the rising sinusoid. The shortcoming of this method is that it is unnecessarily complicated for most cases. The advantage of this method is that it gives the most accurate voltage, V_r , in Fig. 9.

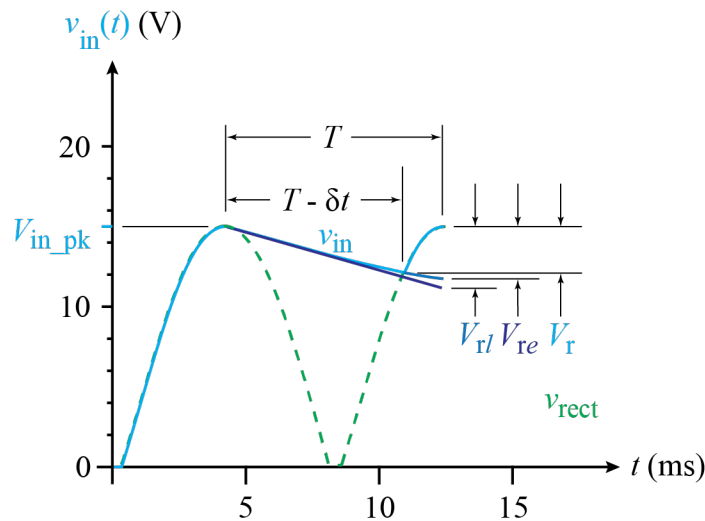


Fig. 9: Capacitor ripple voltage calculation options.

You may use any of the three methods above to derive a formula for the ripple voltage, ΔV_{in} , as a function of the capacitor value.

Insert your derivation of ΔV_{in} as a function of C here.

Derive equation for ΔV_{in} as a function of C

$$\Delta Q = \int_0^{\Delta t} i_C(t) dt \quad 2\Delta V_{in} = \frac{1}{C} \Delta Q$$

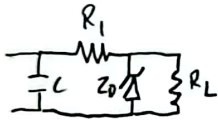
Method 1: $i_C(t)$ constant

$$i_C(t) = \frac{V_{inpk} - 2V_D - 10V}{R_1} \quad \Delta Q = \int_0^{\Delta t} i_C(t) dt = \frac{V_{inpk} - 2V_D - 10V}{R_1} \cdot \left(\frac{1}{120} s\right)$$

$$2\Delta V_{in} = \frac{1}{C} \Delta Q \Rightarrow 2\Delta V_{in} = \frac{1}{C} \cdot \frac{V_{inpk} - 2V_D - 10V}{R_1} \cdot \frac{1}{120} s$$

$$\Delta V_{in} = \frac{1}{2} \cdot \frac{1}{C} \cdot \frac{1}{120} \cdot \frac{V_{inpk} - 2V_D - 10V}{R_1} = \frac{1}{240} \cdot \frac{1}{C} \cdot \frac{V_{inpk} - 2V_D - 10V}{R_1}$$

Method 2: $i_C(t)$ w Thevenin equivalent



From datasheet Z_D at $5mA = 20\Omega$



$$Z_{th} = R_1 + (Z_D || R_L)$$

$$Z_{th} = 302.95\Omega$$

$$\Delta Q = \int_0^{\Delta t} \frac{V_{inpk} - 2V_D - 10V}{R_1} e^{-\frac{t}{R_{th}C}} dt \quad \tau = R_{th} \cdot C$$

$$\Delta Q = \frac{V_{inpk} - 2V_D - 10V}{R_1} \int_0^{\Delta t} e^{-\frac{t}{\tau}} dt = \frac{V_{inpk} - 2V_D - 10V}{R_1} \cdot \tau \left[1 - e^{-\frac{\Delta t}{\tau}} \right]$$

$$2\Delta V_{in} = \frac{1}{C} \Delta Q \Rightarrow 2\Delta V_{in} = \frac{1}{C} \cdot \frac{V_{inpk} - 2V_D - 10V}{R_1} \cdot \tau \left[1 - e^{-\frac{1}{120}\tau} \right]$$

$$\Delta V_{in} = \frac{1}{2C} \cdot \frac{V_{inpk} - 2V_D - 10V}{R_1} \cdot R_{th} \cdot C \left[1 - e^{-\frac{1}{120}\tau} \right]$$

$$\Delta V_{in} = \frac{1}{2} \cdot \frac{V_{inpk} - 2V_D - 10V}{R_1} \cdot R_{th} \left[1 - e^{-\frac{1}{120}R_{th}C} \right]$$

- 6) (10 pts) Complete the power supply design by choosing a value for C and R_1 . Use standard 5% resistors, and use a standard capacitor value of 1, 2.2, 3.3, or 4.7 times some power of 10 in Farads. There are many possible choices for the component values, but your aim is to get the best performance out of your design in the last simulation step.

Insert your chosen C and R_1 values here. You must explain the rationale for your choices.

R_1 was calculated from the expression obtained from section 2 where we defined R_1 in terms of V_{in_mid} given by the expression: $R_1 = (V_{in_mid} - V_Z) / I_{1DC}$, where V_{in_mid} could be either the higher or lower value calculated from the expression obtained in section 4 $V_{in_mid} + \Delta V_{in} = V_{in_pk}$.

- 1) $V_{in_mid} = V_{in_pk} - \Delta V_{in}$ where $\Delta V_{in} = 1.136$ V calculated from section 4.
- 2) $V_{in_pk} = 17$ V $- 2 * V_D$ where $V_D = 0.8$ V (two voltage drops across diodes in rectifier circuit)
- 3) $V_{in_mid} = 16.536$ V; or $V_{in_mid} = 14.264$ V
- 4) $R_1 = (16.536$ V $- 10$ V) / 15 mA = 435.73 Ohms; $R_1 = (14.264$ V $- 10$ V) / 15 mA = 284.27 Ohms

Then, the equations from section 5 that relate ΔV as a function of C were used to obtain a value for C . I used the equations both from method 1 that assumes a linear voltage drop across the capacitor and method 2 that expresses the voltage across the capacitor as an exponential decay equation.

Essentially, I made two main assumptions here: 1) At the peak input voltage the filter capacitor is charged to the peak value; and 2) Between the peaks the rectifier is not conducting. Some further assumptions also accompanied by these two primary assumptions are that the diodes have no dynamic resistance, and the Zener diode either has no resistance, or has a constant resistance of 20 Ohms (as provided by the data sheet for the ideal operating current of 5 mA).

In general, a larger C value would result in a smaller ripple and allows for R_1 to have a higher value. If a value for the capacitor were chosen that results in a voltage across it that is close to $V_Z = 10$ V, then R_1 would have to be smaller to maintain the required current across both the Zener diode and the load resistor. Additionally, if R_1 was too small, then when the input voltage is at its maximum, the current through the Zener diode might exceed the power rating of 250 mW.

Ultimately, C was chosen to be 100 μ F and R_1 was chosen to be 470 Ohms (rounded up to the next standard value from the previous calculation of 435.73 Ohms).

I then created the circuit in LTspice, ran the simulation, and verified the outputs for accuracy and correctness.

(30 pts) **LTspice Simulation:**

After you have completed your analysis and design, simulate your power supply using your C and R_1 values. Fig. 2, shows the example schematic that may be used as a starting point. Fig. 2 also shows the waveforms to record for the circuit and the "error log" file in which measured values are reported.

Use the op codes shown in Fig. 2a for the simulation. The .meas op codes measure the following quantities:

- average output voltage (AVG)
- peak-to-peak variation of the output voltage (PP)
- average power for the Zener diode (AVG of computed power = $-i*v$)
- peak power for the Zener diode (MAX of computer power = $-i*v$)

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[15]

Date: March 3rd, 2024

Note: The Zener diode current measured for the forward direction of a normal diode, but the Zener diode is used in reverse. As a result, the power computed by $p = iv$ will have the wrong sign. To compensate, we multiply by -1 in the power calculation.

See LTspice Tips for more information on the simulation.

Insert your simulation results here. Include the schematic (10 pts), measured waveforms (10 pts), and measured values (10 pts), as in Fig. 2.

```
.meas v_out AVG V(regulator_output)
.meas v_out_pk2pk PP V(regulator_output)
.meas pwr_avg_zener AVG V(regulator_output)*I(D)*(-1)
.meas pwr_max_zener MAX V(regulator_output)*I(D)*(-1)

.include diode.txt
.tran 0.1m 200m 120m
```

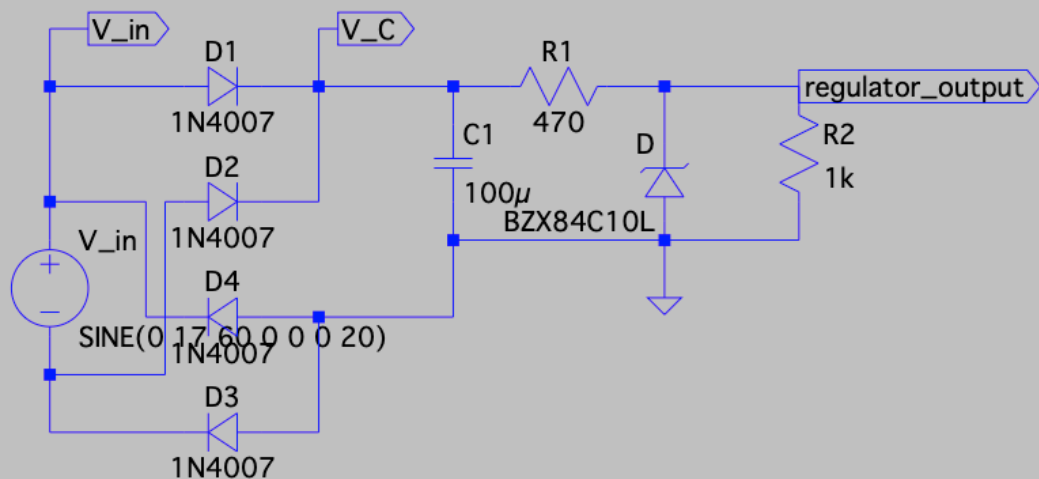


Figure 10: Full Wave Bridge Rectifier Circuit with Filter Capacitor and Zener Diode Voltage Regulator and Load Resistor Connected

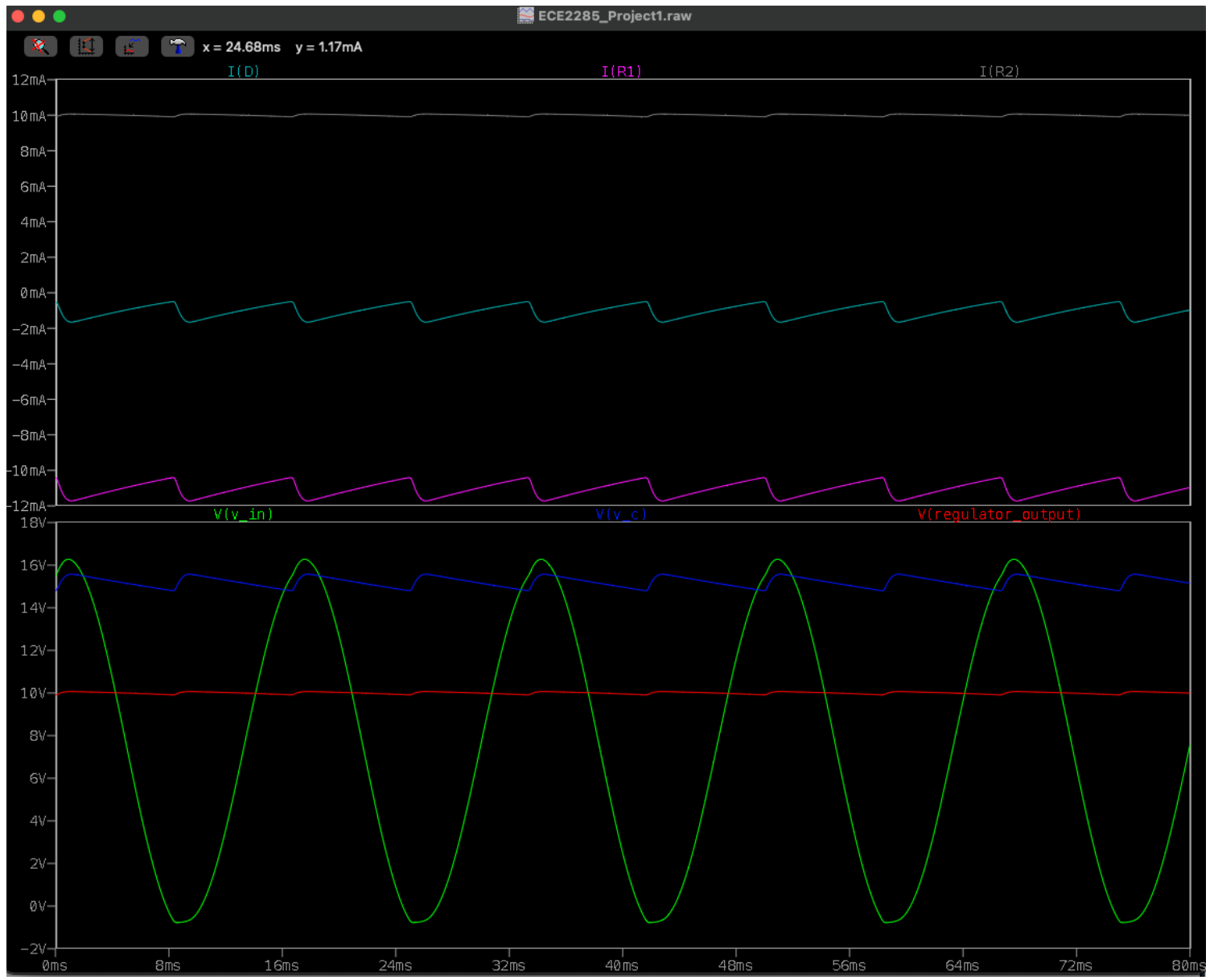


Figure 11: Measured Values with Load Resistor Connected

```
LTspice 17.2.2 for MacOS
Circuit: * /Users/jw/Documents/Computer_Engineering_Courses/Spring_2024/ECE2285/Project1/
ECE2285_Project1.asc
Start Time: Tue Mar 5 09:27:37 2024
Warning: Multiple definitions of model "mur460" Type: Diode
Warning: Multiple definitions of model "mv2201" Type: Diode
solver = Normal
Maximum thread count: 16
tnom = 27
temp = 27
method = modified trap
CompressWinPoints = 1024
.OP point found by inspection.

v_out: AVG(v(regulator_output))=10.0018 FROM 0 TO 0.08
v_out_pk2pk: PP(v(regulator_output))=0.157164 FROM 0 TO 0.08
pwr_avg_zener: AVG(v(regulator_output)*i(d)*(-1))=0.0107589 FROM 0 TO 0.08
pwr_max_zener: MAX(v(regulator_output)*i(d)*(-1))=0.0166981 FROM 0 TO 0.08

Total elapsed time: 0.145 seconds.
```

Figure 12: LTspice Outputs with Load Resistor Connected

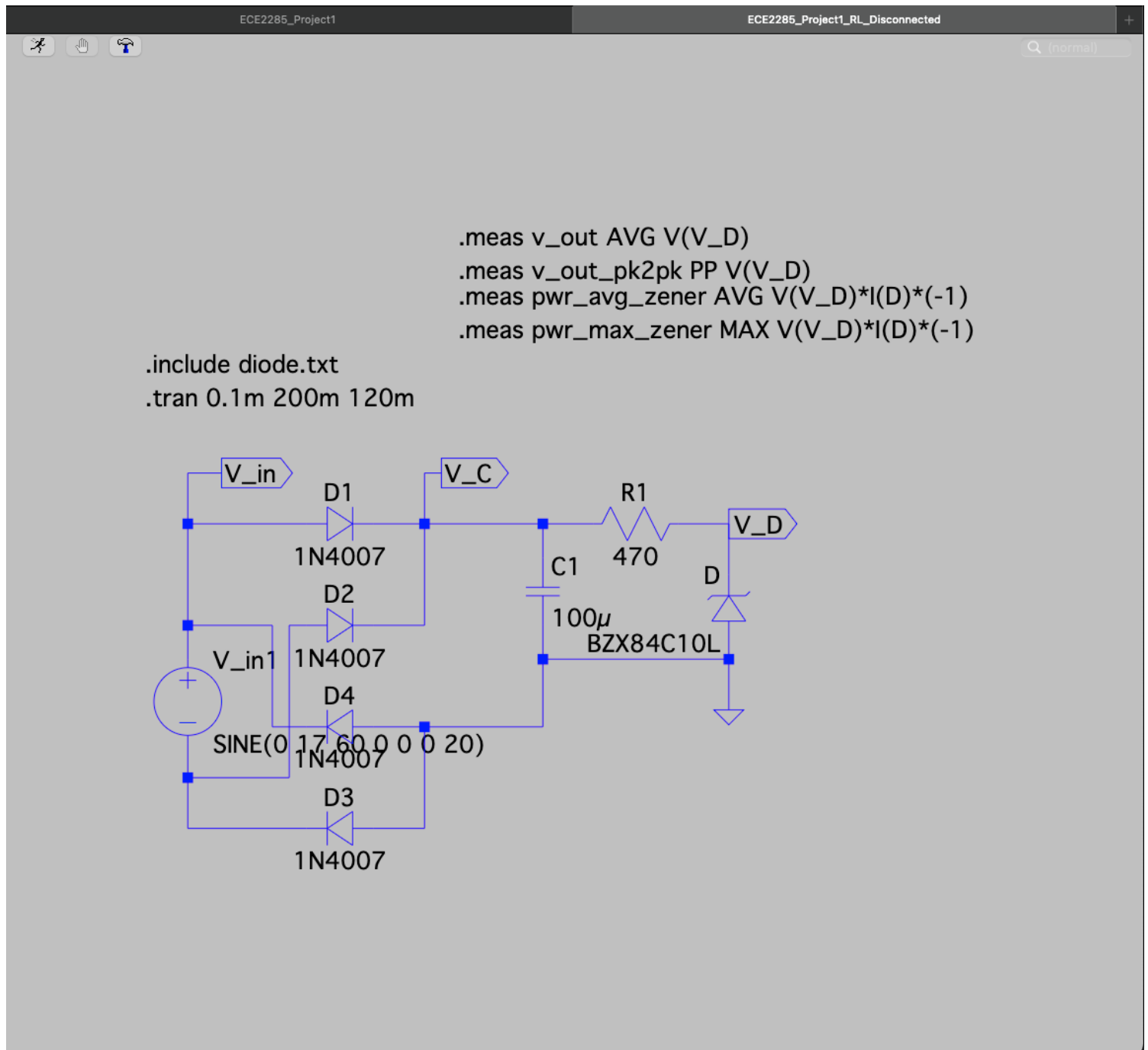


Figure 13: Full Wave Bridge Rectifier Circuit with Filter Capacitor and Zener Diode Voltage Regulator with Load Resistor Disconnected

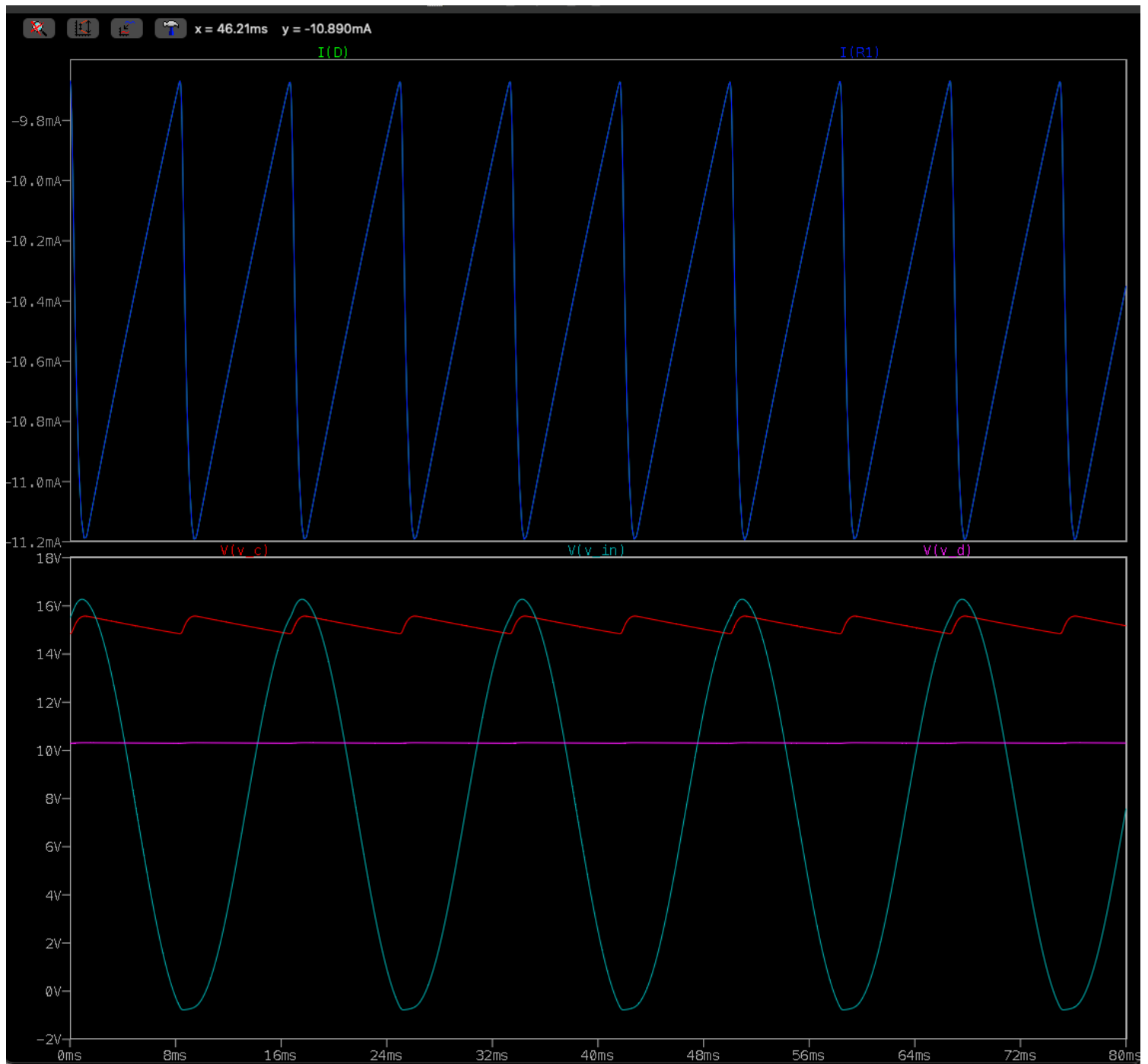
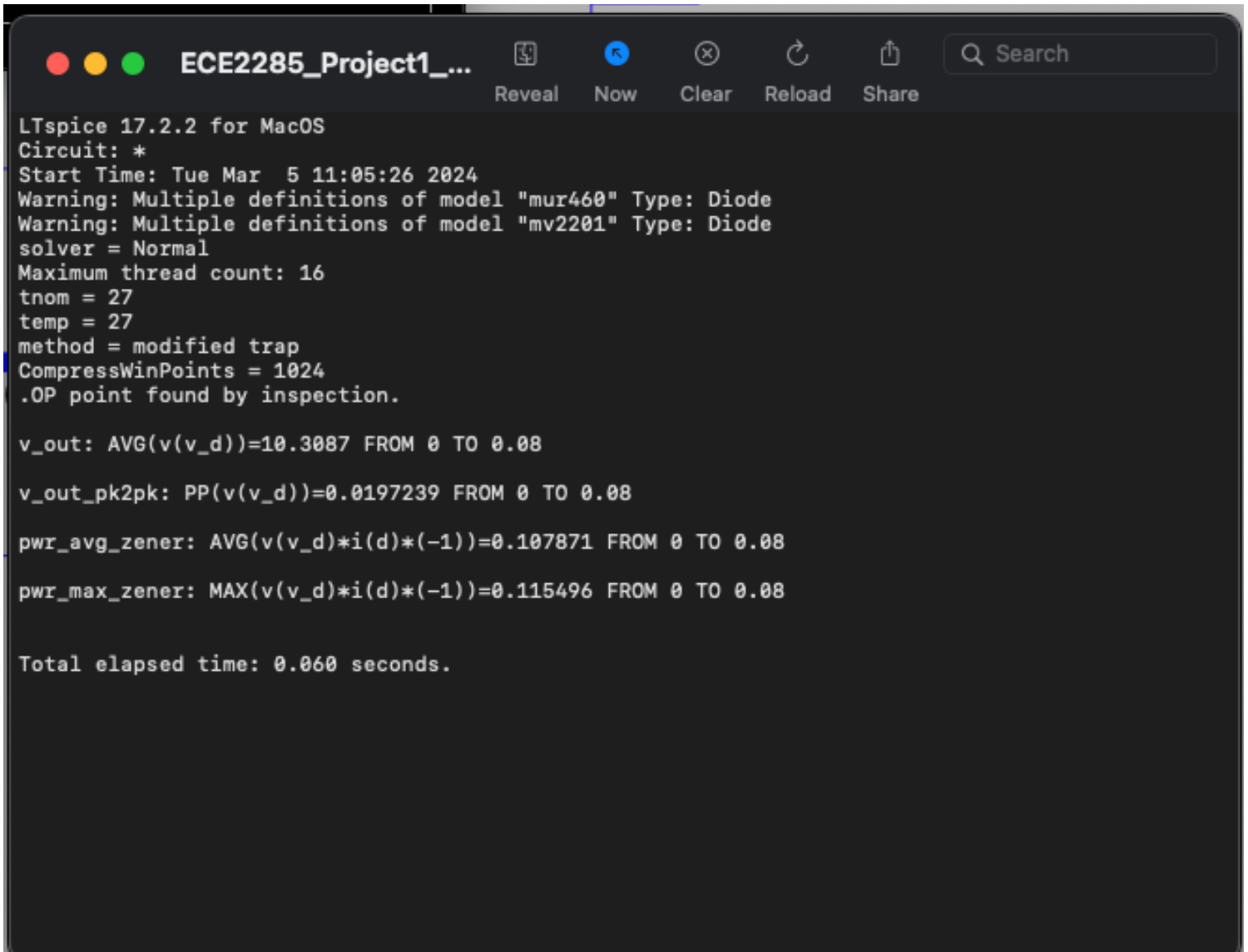


Figure 14: Measured Values with Load Resistor Disconnected



```
LTSpice 17.2.2 for MacOS
Circuit: *
Start Time: Tue Mar 5 11:05:26 2024
Warning: Multiple definitions of model "mur460" Type: Diode
Warning: Multiple definitions of model "mv2201" Type: Diode
solver = Normal
Maximum thread count: 16
tnom = 27
temp = 27
method = modified trap
CompressWinPoints = 1024
.OP point found by inspection.

v_out: AVG(v(v_d))=10.3087 FROM 0 TO 0.08

v_out_pk2pk: PP(v(v_d))=0.0197239 FROM 0 TO 0.08

pwr_avg_zener: AVG(v(v_d)*i(d)*(-1))=0.107871 FROM 0 TO 0.08

pwr_max_zener: MAX(v(v_d)*i(d)*(-1))=0.115496 FROM 0 TO 0.08

Total elapsed time: 0.060 seconds.
```

Figure 15: LTSpice Outputs with Load Resistor Disconnected

Addendum:

A few items to complete the story of the power supply. First, what happens if we remove R_L ? The answer is that, since the Zener diode voltage stays almost constant, the 10 mA that flowed in R_L will now flow through the Zener diode, increasing the current in the Zener diode by 10 mA. Since we designed the circuit for a current variation between $5\text{ mA} - 4\text{ mA} = 1\text{ mA}$ and $5\text{ mA} + 4\text{ mA} = 9\text{ mA}$ (by linearity the deviations above and below the nominal current are the same), the additional current takes the Zener diode to 19 mA, just under the maximum current on the datasheet. Now the maximum current listed on the datasheet makes more sense!

Second, have we exceeded the power rating of the Zener diode? No. Our maximum power dissipation will be close to 10 V times our maximum current of 19 mA which is 190 mW. The power rating on the Zener diode is 250 mW, so we are inside the power limit, but only by a small amount. If we designed for a smaller R_L and then removed it, we might have issues with power in the Zener diode. Conversely, we could reduce the power somewhat by reducing the amount of ripple. With no

ripple at all, an extra current margin of 4 mA is possible. The resistance that gives 14 mA at 10 V is 715 Ω . This value is the absolute minimum possible resistance, if we want to maintain the option of removing the R_L .

Third, where is the Thévenin equivalent model of the Zener diode that is often used? The answer is that the design process is sufficiently accurate and tremendously simplified by treating the Zener diode as a voltage source with no resistance. Now that we have designed the circuit, we could replace the Zener diode with a Thévenin equivalent to determine how the output voltage changes as the input voltage ripples up and down. The solution of that problem is straightforward once the circuit is designed.

(30 pts) **Extra Credit:**

1. (10 pts) Determine the differences between your analyzed values for output voltage and power and those seen in LTspice.

Simulation always reveals details that do not match analysis based on approximations. Specify the differences between the values you predicted for the design as compared to the simulated results. Note that you do not have to modify your design to meet specs if the design predictions meet specs but simulated values do not. (In real life, you would iterate on the design, but that would take more time than we have available for this project).

1) Theoretical Values vs Measured Values

The differences between the theoretical values and measured values for both when the load resistor is connected and when the load resistor is disconnected can be found in Fig.12 and Fig.15, respectively. Perhaps most notably, the average power dissipated by the Zener diode was found to be only 16.70 mW with the load resistor connected. The maximum power dissipated by the Zener diode was still much less than its maximum rating of 250 mW, and the voltage out still remained relatively constant at 10 V plus or minus some deviation as evidenced by the fact that V_{out_pk2pk} was approximately 0.16 V. The percent error between the V_{out} expected of 10 V and the measured average of 10.0018 V, can be calculated by the following:

$$\text{Percent Error} = \left| \frac{\text{Experimental Value} - \text{Theoretical Value}}{\text{Theoretical Value}} \right| * 100\%$$

Substituting measured and theoretical values yields:

$$\% \text{ Error } V_{out} = \left| \frac{10.0018 \text{ V} - 10.0 \text{ V}}{10.0 \text{ V}} \right| * 100\% = 0.018 \%$$

For our purposes, and likely for most practical applications, this is in the realm of acceptable deviations.

When the load resistor was removed, the maximum power dissipated by the Zener diode was measured to be around 115 mW. Again, this is less than the maximum rating of 250 mW. The V_{out_avg} with the load resistor removed was measured to be approximately 10.31 V which aligns with the ranges provided by the data sheet.

Fig. 11 provides the plot of the voltage and current values. As depicted and expected the V_{out} values are around 10 V which further gives credence to the validity of the design. The design here more or less aligns with the expectation and meets the design requirements.

2. (10 pts) State which parts of your analysis you believe caused the differences between your predicted results and the simulated results.

Where did your approximations cause the largest difference between the simulated results and the predicted results? It is vital that sources of error be understood in order for the design process to be efficient. Rather than starting to guess and check different component values in the simulation, an improved design model is needed. Once a deeper understanding of the circuit is gained, a more sophisticated design procedure may be used. Here, you are asked to determine which assumptions in your model(s) are likely responsible for the most significant errors.

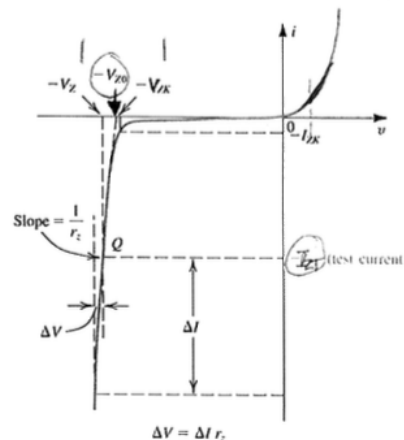
2) Sources for Deviation from Expectation

One initially questionable result was that V_{in} had a maximum at its trough of around 16.4 V (which aligns with the expectation), but the minimum was shown to be slightly less than 0 V, approximately shown as -0.7 V. Given that the input is a sinusoidal waveform, I would initially guess that there would be some amount of symmetry and that the minimum would similarly be approximately -16.4 V. However, there might be some voltage from the rectification diodes that feeds into the branch labeled as V_{in} on the schematic that might account for this. By design the rectifier circuit takes in an AC signal and renders an output of a pulsating DC signal. So, the output from the rectifier will give either a varying voltage that is either entirely positive or entirely negative. The small deviation beyond zero volts of -0.7 V corresponds almost directly to the voltage drop that one of the diodes might give.

Additionally, the plot of the voltages and currents as functions of time in Fig.13 show that the current across the Zener diode vary from around -0.4 mA to -1.7 mA, while the plot of the voltage out remains relatively constant at 10 V. I was under the impression initially that the Zener diode would have a current around its ideal operating current of 5 mA on average. We also measured the current through the Zener diode in the forward direction of a normal diode yet here it is used in reverse. This accounts for the negative value. The actual current would have the same magnitude with positive values.

Moreover, my calculations for selecting a capacitor value used both the approximation method where it is assumes that the current through the capacitor is constant between the relevant time interval of 0 to $t = 1/120$ s, and method 2, where a Thevenin equivalent circuit is used. I think some amount of caution should be taken when using Thevenin equivalent circuits because they somewhat assume linearity. When, in fact, the equation for the current across the capacitor describes exponential decay. There also was an assumption made in the analysis here that the resistance of the Zener diode remains constant at 20 Ohms for all voltages or currents. The resistance of the Zener diode can be dynamic and will vary slightly according to the current through it. The relationship between voltages of the Zener diode and its resistance value can be seen from the handout provided and shown below:

Recall the i-v transfer characteristic of diodes:



Also, the data sheet for the BZX84C10LT1G Zener diode provides that it has a resistance of 20 Ohms when its operating current is the ideal operating current of 5 mA, but is 150 Ohms @ $I_{ZT2} = 1$ mA, and 10 Ohms @ I_{ZT3} of 20 mA.

Furthermore, the resistance of the Zener diode is included in the calculations for R_{TH} expressed as: $R_{TH} = R_1 + (R_Z \parallel R_L)$. While the value of the Zener resistance may not significantly deviate, the deviations do aggregate a bit more when it is also assumed to remain constant when calculating other values. To remedy this, we could model a Thevenin equivalent circuit with some voltage source and non-zero resistor value to replace the Zener diode. We also assumed that when all four rectifier diodes are reverse biased and the capacitor is in its discharge phase, the current across R_1 was at its maximum.

Yet another approximation was that the Zener diode has a constant voltage of V_Z when operating in the reverse breakdown region. While the slope of the i-v curve may be very steep and this isn't an unreasonable approximation, we are implying that the voltage remains V_Z no matter what the current is. If we wanted to spend the time and effort, the i-v chart given from the data could be used to make some calculations and use some kind of interpolation if needed.

More trivial assumptions were made that the diodes possessed a forward voltage drop of 0.7 V or 0.8 V. We also assumed the temperature was in the realm of the specifications provided by the data sheet. The data sheet could be used to obtain specific voltage ranges at currents from which we could make some interpolations or calculations. We could use non linear relationships for the i-v characteristics, account for reverse leakage currents of diodes, account for transient responses using piecewise functions (similar to method 3 specified for obtaining a relationship between ΔV and $I_C(t)$), and so forth.

Lastly, we made small approximations by truncating certain values. For instance, the input sinusoid waveform with an rms value of 12 V is not exactly 17 V. It is 16.9731... V. Programming languages like Python or MATLAB can be used to keep track of floating-point arithmetic for us for slightly better accuracy.

3. (10 pts extra credit) Suggest what better models you would use for a second round of analysis. The level of detail and thought will determine the credit given.