**ECE 2285 Power Supply Simulation**

ECE 2285

Project #2 BJT Amplifier

# Learning Objectives:

* Design, simulate, build, and test an amplifier.

# Requirements:

* Design amplifier with gain = 25
* Use power supply VCC= 5V and load resistor RL=1kΩ.

BJT Amplifier Background and Circuit Overview

Fig. 6 shows a schematic for a typical BJT amplifier. The purpose of the amplifier is to take in a small voltage at *v*IN and produce a scaled-up version of *v*IN at *v*OUT. We could use this circuit to amplify a signal from a sensor that can only produce small voltages, such as an electret microphone.

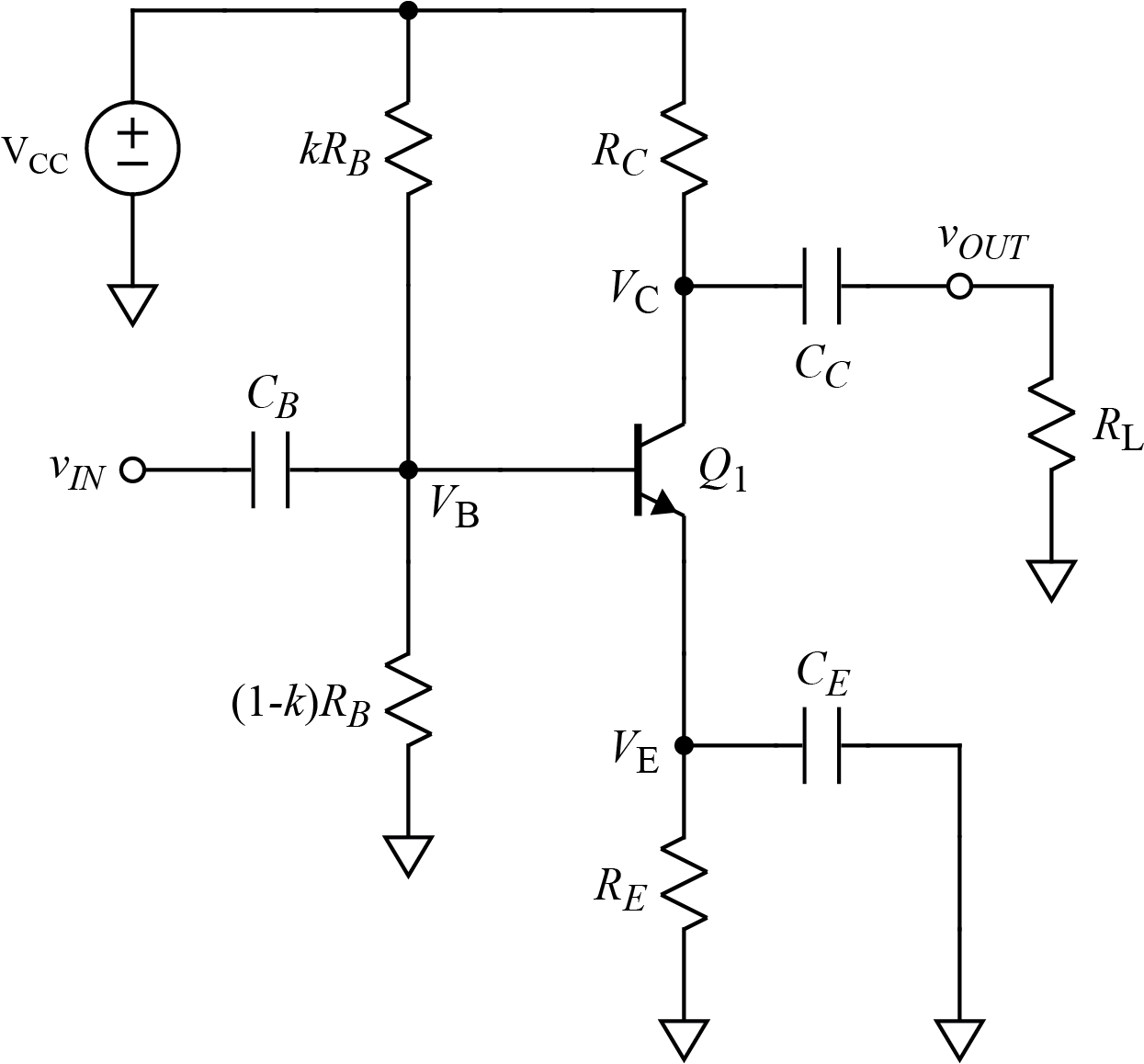


Fig. 6. Common-Emitter (CE) BJT amplifier.

The functions of the components, indicated in Fig. 7, are as follows:

1. Single, positive power supply. (Use 5 V supply from AD2.)
2. Bias resistors to set DC voltage at Base of transistor, which in turns sets the operating point of the transistor and the DC voltage at the collector.
3. Emitter degeneration resistor enabling DC operating point to be independent of transistor gain.
4. Collector resistor creating voltage drop that becomes vOUT.
5. Capacitor to block base DC offset and pass AC signals in from vIN.
6. Capacitor to block collector DC offset from output and pass AC signals to vOUT.
7. Capacitor to short AC signals to ground to make larger AC signals possible at collector without emitter voltage rising and causing transistor saturation.
8. Load resistor (technically not part of amplifier). We will use a 1 kΩ resistor for the load.

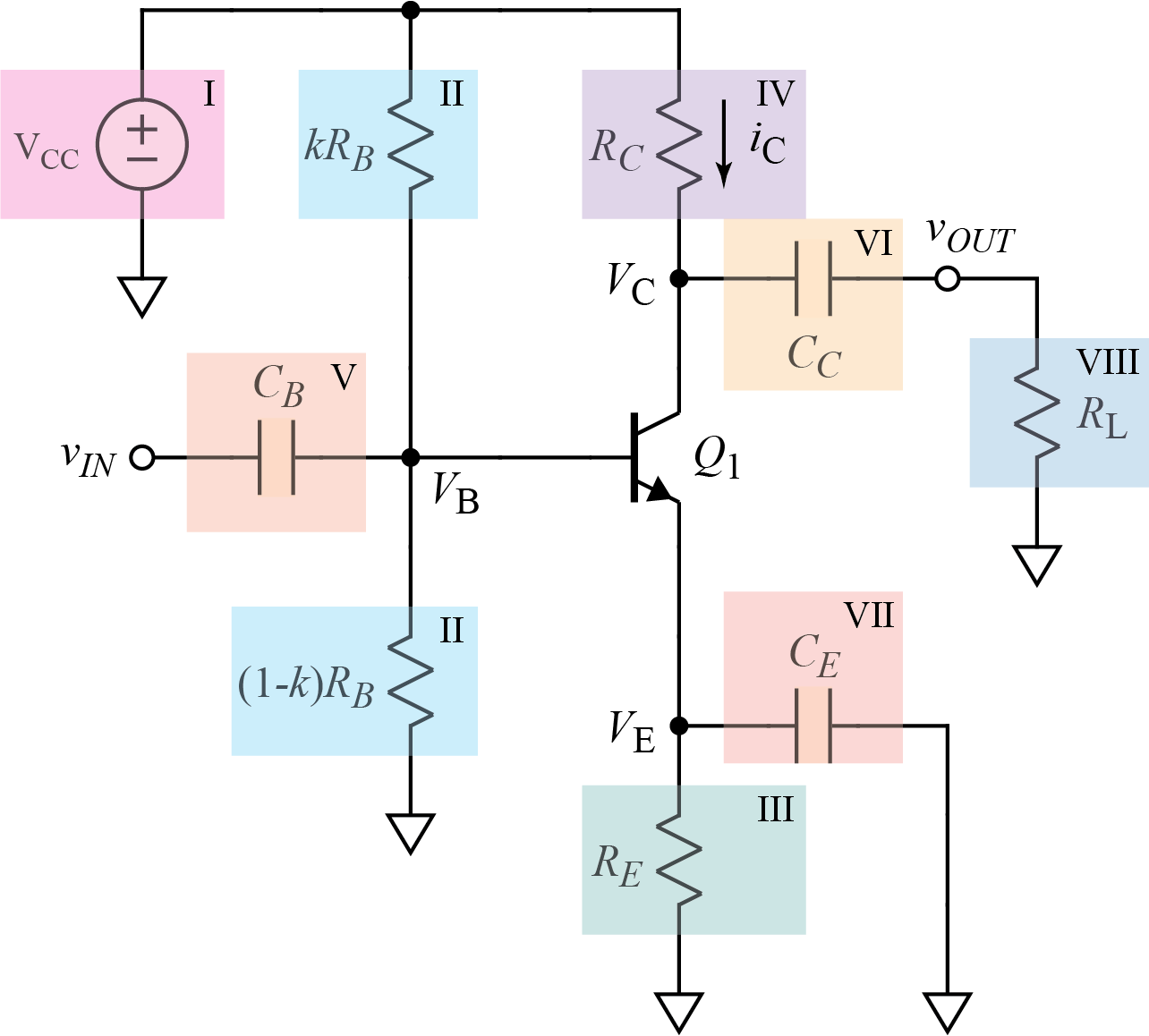


Fig. 7. Components of Common-Emitter (CE) BJT amplifier.

The design of the amplifier is made difficult by competing requirements:

1. To make the DC operating point of the circuit independent of beta, we want the bias resistors (Block II) to be smaller than beta times the emitter resistor (Block III), and to have a larger range for vOUT we want the emitter resistor (Block III) to be smaller than the collector resistor (Block IV), but to have low output impedance we want the collector resistor (Block IV) to be smaller than the load resistor (Block VIII).
2. To have the DC operating point of the circuit be independent of beta, we want the bias resistors (Block II) to be small, but to have high input resistance we want the bias resistors to be large.
3. To have high gain, we want the collector resistor (Block IV) to be large, but to have low output impedance we want the collector resistor to be small.

To satisfy these competing requirements, we have only the gain beta to help us in the step where we want the bias resistors to be smaller than beta times the emitter resistor. Compromises are required in the design process in order to satisfy all the competing needs.

Design Procedure for (CE) BJT Amplifier

**(Use** VCC**= 5V,** RL**=1kΩ. Design for gain = 25)**

DC Biasing

The analysis of the transistor circuit is divided into a DC part and an AC part so we can use superposition to get the complete response. Our first task is to consider the DC bias conditions (with no AC input signal). We want to put the transistor in active mode by setting the base voltage, VB, at a value that gives voltages at VE and VC that can vary with an AC input without causing saturation of the transistor, while at the same time amplifying vin.

For the DC conditions, the capacitors will be open circuits, and we get the circuit shown in Fig 8.

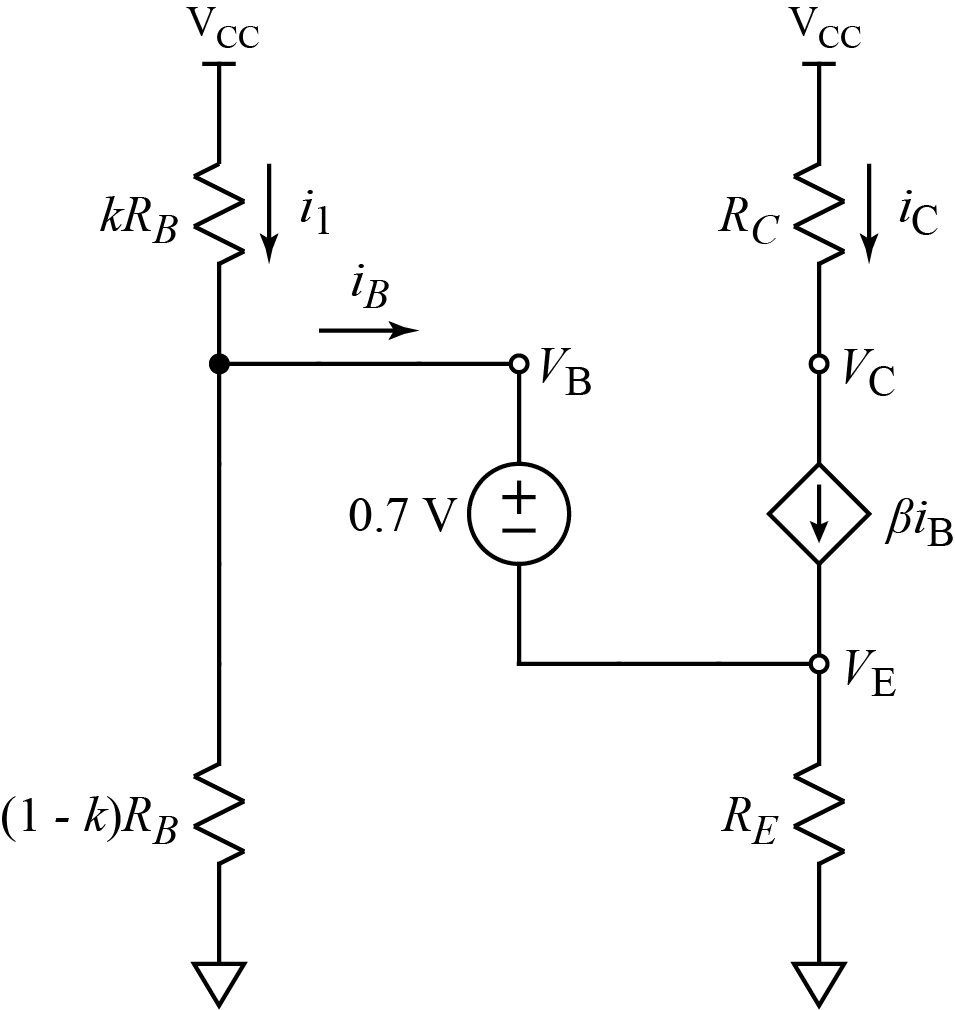


Fig. 8. DC model for Common-Emitter (CE) BJT amplifier.

The key to setting the DC conditions is controlling VB. Fig. 9 shows how VE and VC vary with changes in VB.

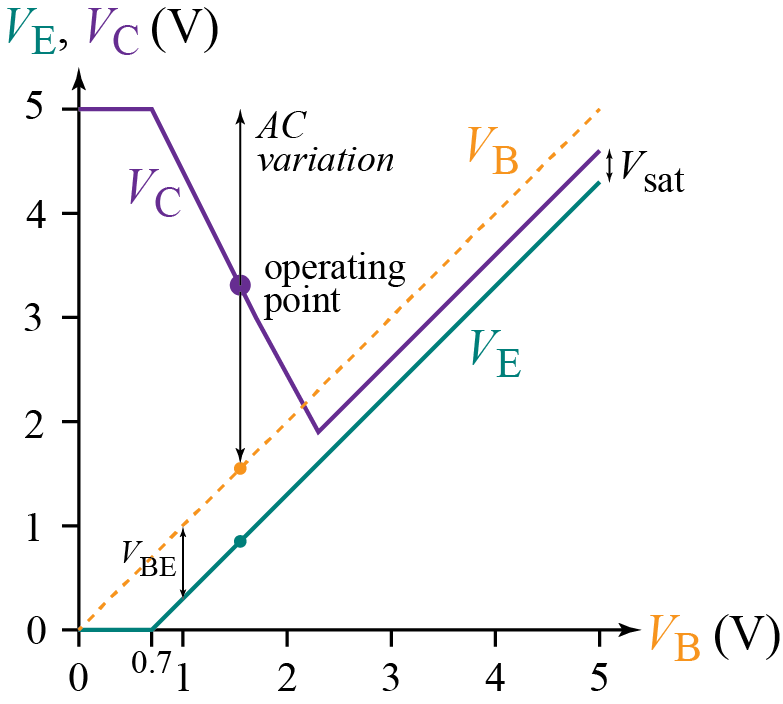


Fig. 9. Operating point for (CE) BJT amplifier.

Starting at the origin in Fig. 9, we consider what happens as VB increases:

Until VB reaches the diode turn-on voltage of 0.7 V, no current flows in the transistor, and VE will be zero, whereas VC will be VCC since there is no current in RC.

As VB increases above 0.7 V, VE must remain one diode drop, or about 0.7 V, below VB. The current in the emitter will be VE/RE = (VB - 0.7 V)/RE. That is, the base voltage dictates the emitter current. The collector, in turn, has almost the same current as the emitter. If RC is larger than RE, as is usually the case, the voltage drop across RC will increase rapidly, lowering VC.

If the VCE drop gets too low, as it does around VB = 2.3 V in Fig. 9, the transistor saturates, and the gain drops so as to maintain the saturation voltage from the emitter to the collector as VB and VE continue to increase. The emitter voltage must keep increasing since the VE voltage must remain one diode drop of 0.7 V below VB.

We want to avoid saturation when we add an AC signal to VB, and we want a DC operating point for VC that allows the VC to increase or decrease the same amount before hitting the power supply voltage on top or saturation on the bottom. The operating point indicated in Fig. 9 indicates the approximate location of a possible operating point. At the operating point, VB is about 1.6V and VE is about 0.9 V. Using a VE around 1 V is a practical choice: VE = 1 V allows for a large VC swing, but it also allows for VE to vary slightly with AC inputs that we approximate as being totally eliminated by the emitter capacitor, CE, but which, in reality, do cause some variation in VE at lower frequencies.

For DC bias, all capacitors will be open-circuits, and we use the DC transistor model in Fig. 8. To calculate base current IB, we use reflected resistance to create a simpler circuit model. Fig 10 shows the reflected-resistance DC model we are working with. The bias resistors are turned into a Thévenin equivalent, and the dependent current source is shown split into two equal current sources to emphasize that the solution of the collector circuitry is a separate problem from the setting of the base current (assuming we avoid saturation of the transistor).

The following ideas are involved in choosing values of resistors for the DC model:

1. We maximize gain by choosing a DC value of VC such that the change in current in VC when an AC input is present takes VC up to a voltage no more than VCC and down to a voltage that is VE plus saturation voltage (Vsat ≈ 0.2 V or 0.3 V).
2. The voltage at the base with an AC input present should never drop below 0.7 V so as to ensure that the transistor is always fully turned on.
3. The current in RC and RE is about the same, and we theoretically get the largest possible swing of VC if we minimize RE. The problem, however, is that gain is unknown. It is impractical to adjust circuit values to accommodate variations in beta. Using a nonzero RE allows us to effectively control the gain of the transistor by fixing the DC value of VE, which in turn determines the value of IE, which in turn fixes the DC value of VC, since IE and IC are about the same. This is why we use this "emitter degeneration" configuration.
4. Controlling the value of VE is accomplished by choosing biasing resistors, (1 - k)RB and kRB, that form a "stiff" voltage divider that essentially fixes the value of VB. This is accomplished by making I1 much larger than IB. "Much larger" is usually taken to be a factor of 10. (A factor of 20 would be more consistent with the 5% accuracy of resistors, but the tradeoffs in the circuit design are such that a factor 10 is often what we can afford to do given other considerations, such as input impedance of the circuit, as discussed below.
5. We know IB is IC /β. Thus, if we know IC, then we want I1 > 10IC /β. We also have that I1 ≈ VCC/[kRB + (1 - k)RB] = VCC /RB. Thus, our condition is

.

1. Solving for RB, we have a rough estimate of the base resistance:

.

1. To calculate the value of IB more precisely, we may use the reflected resistance concept, as shown in Fig. 10. The voltage divider formed by (1 - k)RB and kRB. has been converted to a Thévenin equivalent with VTh = VCC(1 - k)RB / RB, and RTh = (1 - k)RB || kRB. This model shows that the effect of the dependent source in the transistor is equivalent to multiplying RE by β + 1. Thus, the (β + 1)RE acts like a resistive load on the voltage divider formed by (1 - k)RB and kRB. If (β + 1)RE is much less than RThB, current IB is much less than I1, and the voltage at the base of the transistor will be approximately VThB. Thus, a more accurate specification for RB is the following equation:

or, using a factor of 10 as the definition of "much less than", we have

. (2)

The factor of kis found from the biasing voltage divider that gives VB:

.

For a BJT, the current in the emitter is approximately the same as the current in the collector, so by Ohm's law the change in voltages at the emitter and collector will be proportional to RC and RE. We want of gain of 25 from the change in voltage at the collector. If we want a large voltage swing at VC, we will want a smaller voltage swing at VE to avoid saturating the transistor. Note that, as *V*E goes up, VC goes down, so they act together to reduce the voltage, VCE, across the transistor. If VCE gets too small, the transistor goes into saturation.

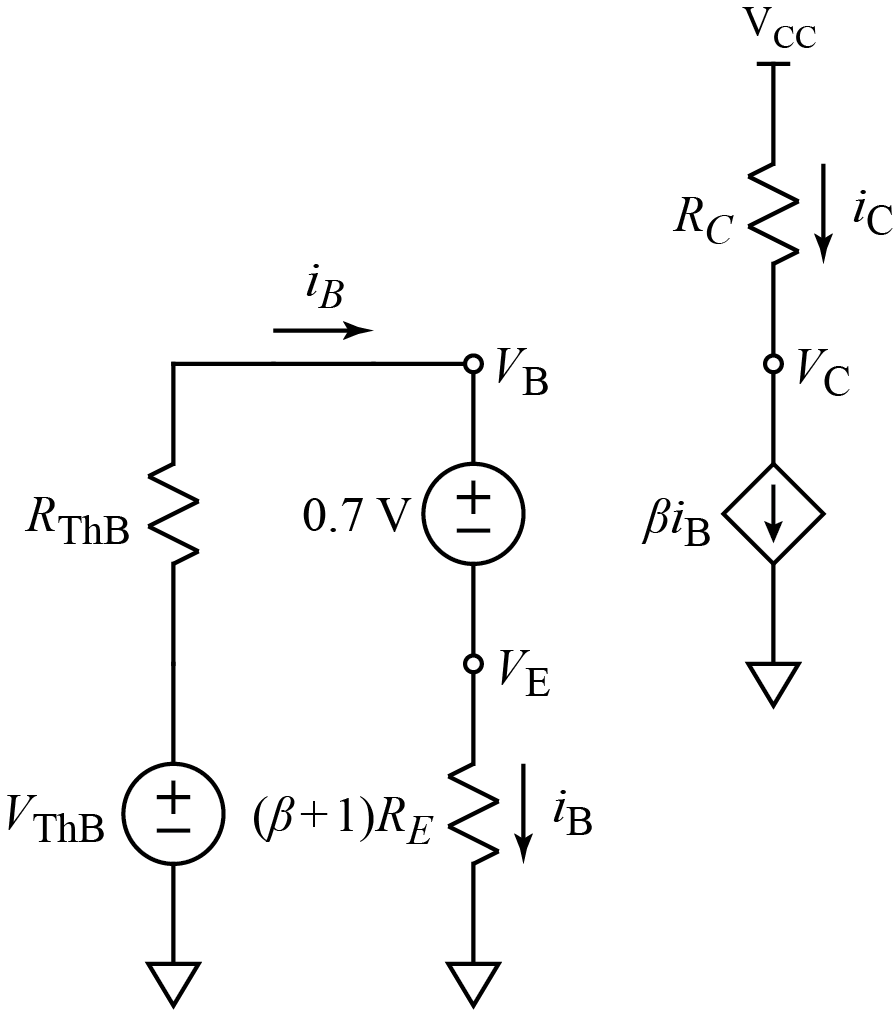


Fig. 10. Reflected impedance model of (CE) BJT amplifier.

Thus, a small value for VE is useful so that the transistor stays in the active mode (VE < VB < VC) where VB= VE + VBE. So the smaller value for VE lets there be a large range until VB gets close in value to VC. Therefore, something around 1V is usually used for VE. Here, since we have a relatively low VCC of +5 V, we will use 0.5 V.

With *I*B negligible compared to *IC*, we have and

and

. (3)

where, again, if IC is known, *R*E can be solved for.

AC Biasing

Once we solve for the DC conditions in the circuit, we can find the AC model of the circuit. For the hybrid- small-signal AC model shown in Figure 11, we have

(4)

and

. (5)

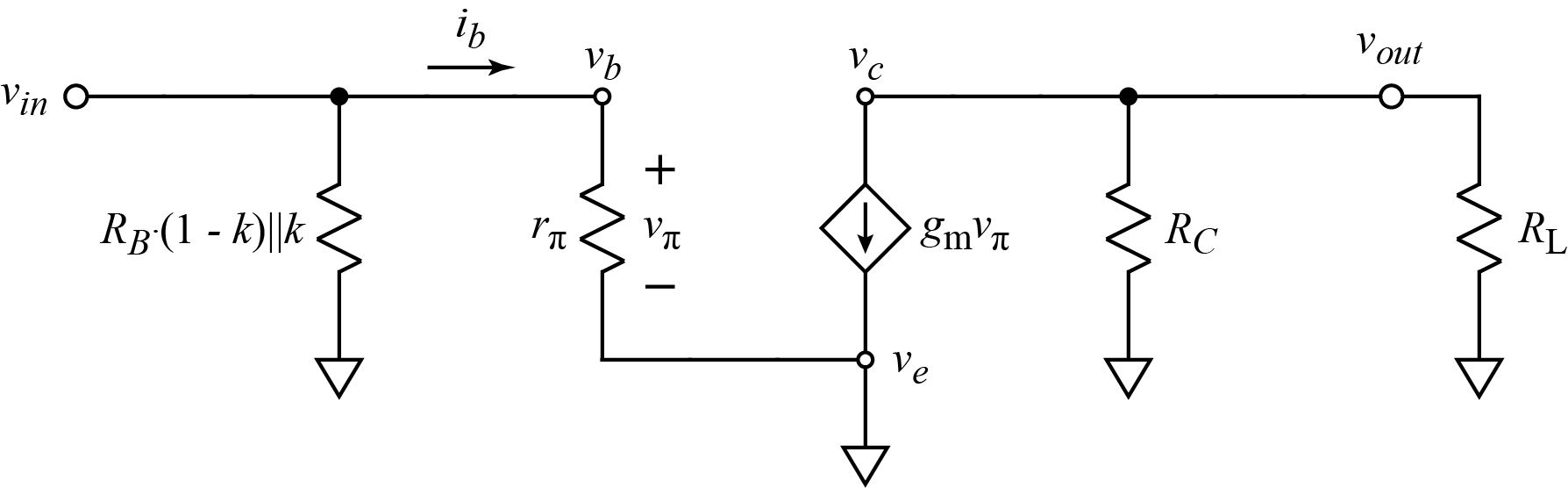


Fig. 11. hybrid- small-signal AC model

The AC gain of the circuit may be found by Ohm's law:

(6)

with

.

Combining these equations gives the relationship between vin and vout: and expresses the gain in terms of the DC collector current, IC.

or

. (7)

**Example:**

Say that we want to design this amplifier to have a gain = 20:

(8)

A value for RC or IC is needed, and we are given RL. = 1 kΩ. The DC operating point, where RL is disconnected owing to blocking capacitor CC, gives us the extra equation we need.

We want to make sure that VC is a higher value than VB so that the transistor stays out of saturation (VB < VC). Since vC will vary up and down, it makes sense to have a DC value of VC halfway between VCC and the maximum of VE plus VBE = 0.7 V to avoid saturation. We chose a VE of 0.5 V earlier, so our VB and our minimum total vC would be

.

A convenient operating point of VC= 3 V is close to halfway between VCC and the minimum vC.

This value of VC = 3 V is 2 V below VCC, and we know that this DC voltage is created by IC times RC (without RL because of the blocking capacitor CC).

or

(9)

Now we can substitute for IC in (8) and solve for RC.

We do some algebra to isolate RC.

or

or

(10)

Using values of VT = 25 mV and RL = 1 kΩ, we find RC:

.

From (9) we can now compute the value of IC:

Using this value of IC and the expected value of β = 100, (you can use the actual β from Table 1 in your design), (3) gives

,

and (2) gives

.

The characteristics of the transistor for the small-signal model are

and

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Now it is possible to find the value of (1 - k)RB and kRB that gives vB = VE + 0.7V = 1.2 V. Calculate the value of k for use in your design.

**Capacitor Estimate Values**

An estimate for the capacitors is to use:

(11)

Where fC is a critical frequency, which you want to be less than 10 Hz if possible for voice signals. Resistance R will be the Thévenin resistance seen by the capacitor in the AC model, (i.e., the input resistance or output resistance of the circuit). Therefore, for CB we have

.

Suppose we had used k = 1/2 for our (1 - k)RB and kRB resistors. This is *not* the value of k you found, but it turns out to be the value of k that causes the voltage divider formed by (1 - k)RB and kRB to be most sensitive to IB as discussed below. (Also, k = 1/2 gives simpler results!)

If we use k = 1.2/5, RB= 41.5 kΩ, RE= 750 Ω, RC = 3 kΩ, RL= 1 kΩ, β = 100, and IC = 0.67 mA then

or

or

or

.

Solving (11) for C, we have

.

We also want the RC value for the output to be large enough. For this calculation, we use the output impedance, RC, plus RL since both are in series with CC at vout:

Finally, we want the time constant looking into CE from reference to be sufficiently large:

Design Your Own CE Amplifier With a Gain of 25 (50 pts)

Redo the above design for a gain of 25 (or as close to 25 as possible). You also might want to utilize MATLAB for the design.

After you derive design values, draw the circuit in LTSpice and simulate it. To achieve the gain, modify the resistors until you reach the same current for as you had for your design. Recheck that VE < VB < VC, and VE, VB, and VC are close to the expected values.

Verify that amplification (Vout/Vin) is around 25 for 100 Hz, 1 kHz, and 10 kHz. If the signal is distorted for the transient, make sure to reduce the input voltage.

You can use the following to change the value of Beta in the simulation:

.MODEL MyBJT AKO: 2N3904 (Bf=100)

Where you can replace the NPN name with MyBJT and the Bf value with the value that you measured in Table 1 of Lab 3. See Figure 12 for an example schematic. In the schematic, you will need to change the V1 voltage source value to be "AC 1" and remove the asterisk from the spice directive at the bottom of the schematic to do the AC sweep.

**(10 pts) Add a page at the end of this report with your hand calculations/MATLAB for the CE amplifier with Gain = 25.**

**(10 pts) Add a page at the end of this report with the LTSpice schematic of your design for Gain = 25.**

**(10 pts) Add a page at the end of this report with the AC sweep simulation showing the design produces a gain of 25 V/V and operates at a minimum at 100Hz or lower. (Start simulation at 10 Hz.) This will be the Bode Magnitude Plot.**

**(10 pts) Add a page at the end of this report with a transient simulation showing the design produces a gain of 25 V/V for 1 kHz with no distortion. Note the input magnitude for no distortion. Make sure to only show a maximum of 4 cycles (4ms).**

**(10 pts) Add a page at the end of this report with the spice logs for the transient simulations for 100 Hz, 1 kHz, and 10 kHz respectively.**

A close up of text on a white background

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Fig. 12. Using “AKO” for simulation.

A screenshot of a computer

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Fig. 13. Example of transient simulation showing no distortion (for larger gain ≈ 40)

Build Your CE Amplifier and Test it (50 points)

Build your designed CE amplifier and test it. Note that larger capacitors are more expensive and so use the 100μF and/or other capacitors in the kit for your built circuit. Also, use potentiometers where appropriate so that you can adjust them to achieve the designed IC current. Recheck that the transistor is in active mode, VE < VB < VC, and VE, VB, and VC are close to the expected values.

Verify that amplification or gain (Vout/Vin) is around 25 for 100Hz, 1kHz, and 10kHz. If the signal is distorted for the transient, make sure to reduce the input voltage.

Note: Be sure you use non-polarized (also called bipolar) capacitors if the capacitor voltage is ever negative.

**(10 pts) Add a page at the end of this report with a photo of your amplifier circuit on a breadboard.**

**(30 pts) Add a page at the end of this report with a screen capture from your equipment that shows the circuit amplification gain of 25 at 100 Hz, 1k Hz, 10 kHz from your built prototype that is working. Use a screen capture of a dual-trace oscilloscope of vIN and vOUT at each frequency. Make sure to annotate or clearly show the values used for calculating the gain values.**

**(10 pts) Add a graph at the end of this report with a plot of the gain on a dB scale versus frequency (on a log scale) like a Bode plot. Show your measured values of gain at 100 Hz, 1k Hz, and 10 kHz on the plot. Add more points as needed for a representative picture of the gain versus frequency.**