ECGR 3183 - Final Project Report

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Memory Elements

Instruction Memory ,Register File, Data Memory & Stage Registers

Instruction Memory:

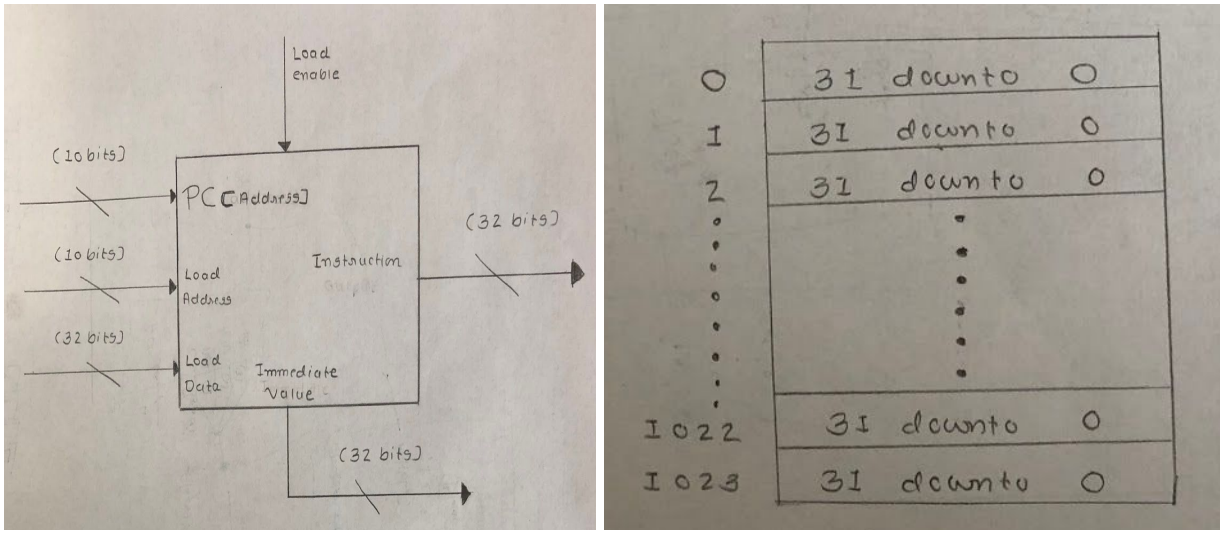

Figure 1: Black Box Diagram of Instruction Memory

Above image 1, shows the diagram of the instruction memory. Instruction memory is designed to have a capacity of storing 1024 words maximum at once (4096 bytes). As shown in figure, it has four input ports and two output ports. For the Program Counter and load address ports 10 bits signal ports are used to index the particular word of data from 1024 different word(1 word = 32 bits) values. Load Data port is used to transfer the data to instruction memory when load enable signal is high (once while loading the program). For output, two ports of 32 bits are assigned. Instruction output signal is used to omit out the pointed instruction data by PC. While the Immediate value signal carry outs the immediate value stored on instruction memory.

For the stimulation of the instruction memory, 1024 arrays each of 32 bits were created using the VHDL code. Instruction memory is programmed to omit out one word of instruction data and reading new PC value on every rising edge of clock. For loading the new data to instruction memory, load data port is used to transfer the new data and load address is used for pointing the load location for new data. While load enable port is used to activate the load data and load address ports. Finally, the immediate values according to ISA uses 32 bits (entire block of word) so, the instruction consisting of immediate values omits out the entire block of word data followed by the one indexed by PC (PC+1) indexed value of particular instruction.

Register File:

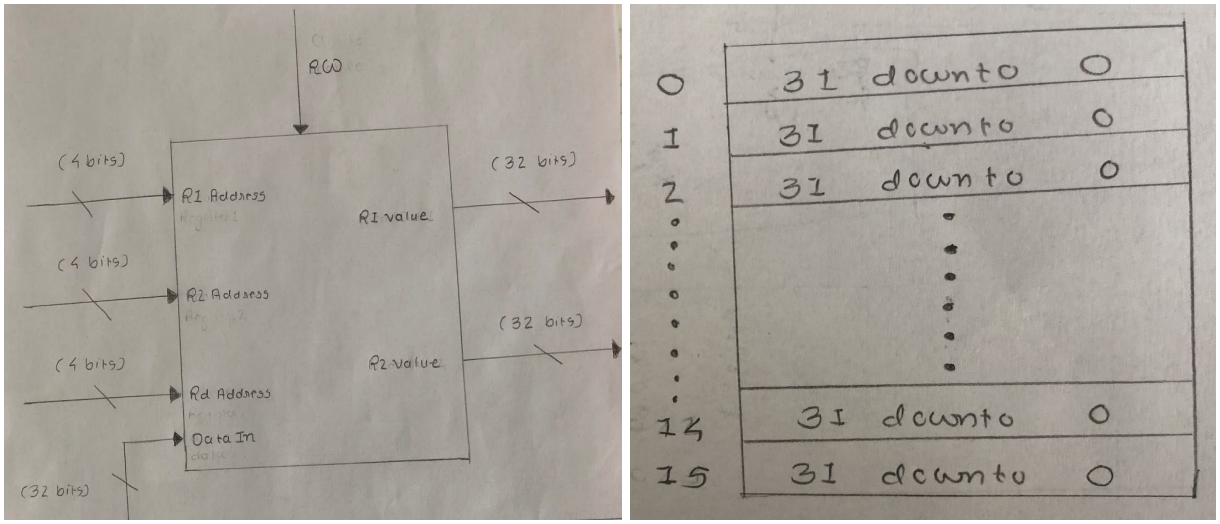

Figure 2: Black Box Diagram of Register File

Above image 2, shows the diagram of the register file. Register file designed for the processor consist of the sixteen different registers each of 32 bits. As demonstrated in diagram, it has five input ports and two output ports. ‘R1 Address’ and ‘R2 Address’ ports each with four bit bus signal are used to point the two source registers from the register file similarly, ‘Rd Address’ port is used to point the destination register for the particular instruction.’Data In’ port with 32 bit bus signal is used for transferring(writing) the data to the destination register, when ‘RW’ signal is high. For output ‘R1 value’ and ‘R2 value’ ports each assigned with 32 bits bus signal for passing the source register data to ALU for execution stage.

For stimulating the register file,16 arrays each of 32 bits were created using the vhdl code. Register memory is programmed to omit out data at output ports on every rising edge of the clock cycle and read new input values pointing the other new two source registers. For writing the data to destination register on the register file, ‘RW’ signal is activated then, ‘Rd Address’’ port is used to point the destination register on the file and data is written through the ‘Data In’ port.

Data Memory:

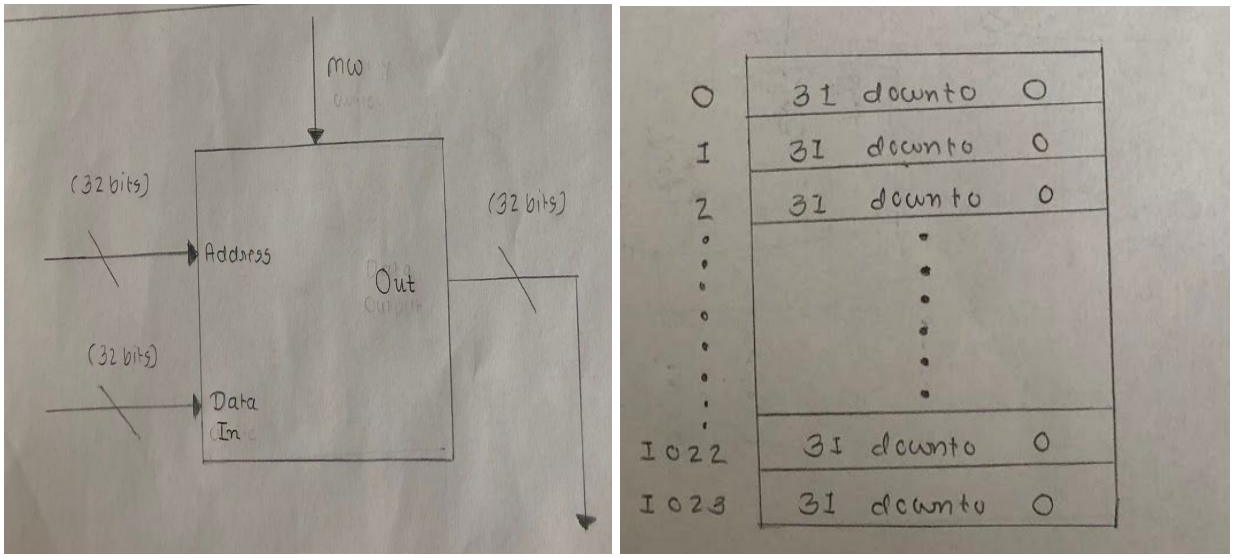

Figure 3: Black Box Diagram of Data Memory

Above image 3, shows the diagram of the data memory. Data memory is designed to have capacity of storing 1024 words maximum at once (4096 bytes). As shown in diagram, it has three input and one output ports. ‘Address’ port is assigned the signal of 32 bits bus for indexing the particular word in data memory. ‘Data In’’ port is used to transfer/write the data in the data memory when ‘MW’ signal is high. For the output ‘Out’ port is used, it also has 32 bit bus signal assigned to it. Output data then is written to destination register.

For stimulation of the data memory, 1024 arrays each of 32 bits were created using the vhdl coding. Data memory is programmed to omit out one word(1 word = 32 bits) of data and read new ‘Address’ on every rising edge of clock cycle. For storing the new data in data memory ‘Data In’ port is used for writing the new data and ‘Address’ port is used to point location in memory. ‘MW’ signal is used to activate the both of the other input ports. At last, data omitted by ‘Out’ port is send to the ‘Data In’ port of the the register file. The only issue faced while stimulating the data memory was that the ‘Address’ value calculated by the ALU was in format of floating point numbers, so it became hurdle for indexing the location in memory. To fix that problem, function that converts the floating point number to integer format was utilized.

Stage Registers:

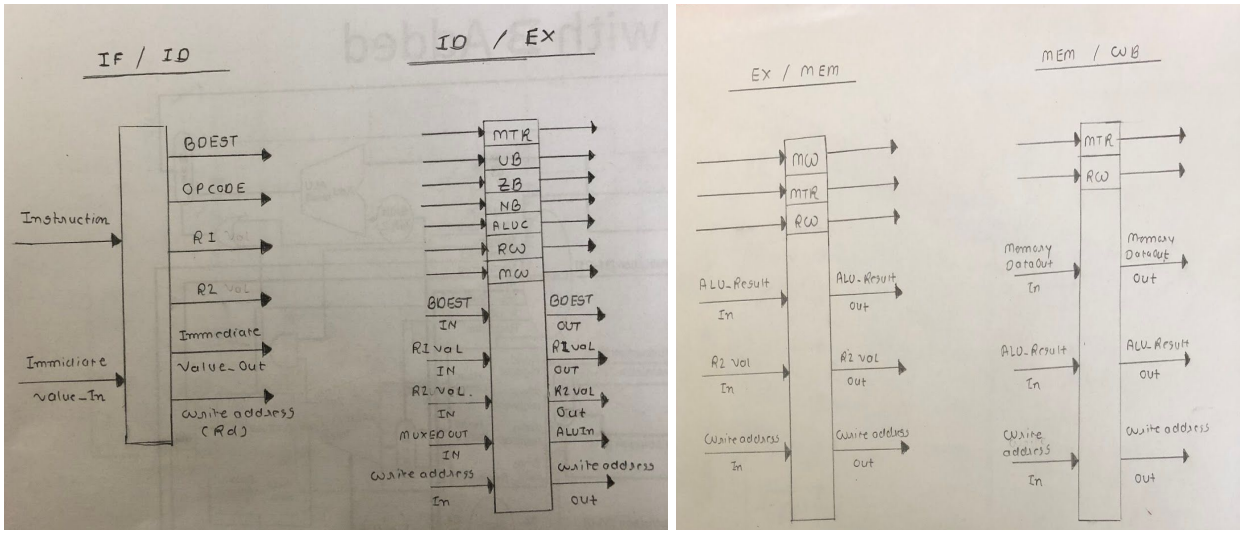

Figure 4: Black Box Diagram of four Stage Registers

As shown in figure 4, four stage registers are used while applying the pipeline on the processor. Each stage in processor pass its output signals along with the control signals to this stage registers and then stage registers pass those signal to next stage as per needed (by detecting hazards). For stimulation of these registers VHDL code was used. Basically registers were designed to take the input in form of signal on rising edge of clock of clock, and omitted the signals for the rest.. Below is the the description of each stage register in brief:

IF/ID: This stage register receives the inputs from fetch stage components like instruction memory and passess output to decode stage component such as register file.

ID/EX: This stage register receives the inputs from decode stage components like register file and passess output to execution stage component such as ALU.

EX/MEM: This stage register receives the inputs from execution stage components like ALU and passess output to memory stage component such as data memory.

MEM/WB: This stage register receives the inputs from memory stage components like data memory and passess output back to destination register in register file.