SPB2 CT Trigger Board Memory Map
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NOTES:

1. All time periods (length, counter value, prescale value, etc…) are specified in units of ticks of the 100 MHz local clock.
2. Registers shown in red exist, so they can be read/written, but they are not yet connected to any logic.

Overview

Memory Block	*Ethernet Space*	*Starting Address*
System Registers	0	0x0000
Trigger Registers	0	0x1000
Counter Registers	0	0x2000
Block Memory Control Registers	0	0x3000
Block Memory Access Registers	0	0x8000

System Registers

To be completed.
This includes the Info registers from Mesa Electronics and the SPB2 CT version/date registers, etc…

Trigger Registers

Trigger Control and Status Registers

ID: Name	*Address*	*Functionality*	*Access*
0: Discriminator Stretching Enable-0	0x1000	D0-D31: Turns on(1)/off(0) stretching logic for discriminators 0:31	R/W
1: Discriminator Stretching Enable-1	0x1004	D0-D31: Turns on(1)/off(0) stretching logic for discriminators 32:63	R/W
2: Discriminator Stretching Length	0x1008	D0-D6: Length of stretched discriminator signals	R/W
3: Discriminator Stretching Restart	0x100c	D0: Turns on(1)/off(0) logic to restart stretching if a discriminator re-fires while stretching is already in progress	RW
4: Discriminator Test Trigger prescale	0x1010	D0-D15: Pre-scale value for Test trigger (at least 1 discriminator fired)	RW
5: Internal Trigger prescale	0x1014	D0-D31: Pre-scale value for internal Trigger	R/W
6: Internal Trigger Mode	0x1018	D0: Sets Internal Trigger in standalone (0) or LED (1) mode	R/W
7: External Trigger Mode	0x101c	D0: Sets External Trigger in standalone (0) or LED (1) mode	R/W
8: GPS Trigger Mode	0x1020	D0: Sets GPS Trigger in standalone (0) or LED (1) mode	R/W
9: LED Delay	0x1024	D0-D7: Delay between LED strobe and Event Trigger for LED triggers	R/W
10: Transit Busy Length	0x1028	D0-D15: Length of the Transit Busy	R/W
11: Enable Busy	0x102c	D0: Enables (1) or Disables (0) use of the CoBo Busy input D1: Enables (1) or Disables (0) use of the local Buffer Busy input	R/W
12: Clear Busy	0x1030	D0: Clear the Transit Busy D1: Clear the CoBo Busy D2: Clear the local Buffer Busy	W
13: Save Busy	0x1034	D0: Save the current status of all Busy bits to a static register	W
14: Read Busy Status	0x1038	D0: Saved Transit Busy Status (1 = Busy, 0 = Live) D1: Saved CoBo Busy Status (1 = Busy, 0 = Live) D2: Saved Buffer Busy Status (1 = Busy, 0 = Live)	R

		D3: Saved Block Memory Full Status (1 = Busy, 0 = Live) D4: Saved Trigger Board Busy Status (1 = Busy, 0 = Live)	
15: Enable Trigger Types	0x103c	D0: Enable (1) or disable (0) the bifocal coincidence trigger D1: Enable (1) or disable (0) the discriminator test trigger D2: Enable (1) or disable (0) the internal trigger D3: Enable (1) or disable (0) the external trigger D4: Enable (1) or disable (0) the GPS trigger NOTE: The LED trigger is automatically enabled if any of the Internal, External or GPS triggers is set to LED mode.	R/W
16: Enable Triggering	0x1040	D0: Enable (1) or disable (0) trigger generation	R/W
	0x1044 – 0x107c	Reserved for future Control and Status Registers	N/A

Local Event Data Buffer

ID: Name	*Address*	*Functionality*	*Access*
0: Event Number	0x1080	D0-D23: Current event number	R
1: Time-0	0x1084	D0-D31: Clock Counter value when trigger was issued 32 LSB	R
2: Time-1	0x1088	D0-D7: Clock Counter value when trigger was issued 8 MSB	R
3: Trigger List	0x108c	D0: Bi-focal trigger was enabled and fired D1: Discriminator test trigger was enabled and fired D2: Internal trigger was enabled and fired D3: External trigger was enabled and fired D4: GPS trigger was enabled and fired D5: LED trigger was enabled and fired	R
4: Disc-Str-1	0x1090	D0-D31: Stretched discriminator bits for discriminators 0:31	R
5: Disc-Str-2	0x1094	D0-D31: Stretched discriminator bits for discriminators 32:63	R

Counter Registers

Counter Control and Status Registers

ID: Name	*Address*	*Functionality*	*Access*
0: Clear Counters	0x2000	D0: Clear all counter values and overflow bits	W
1: Save Counters	0x2004	D0: Save all counter values to static registers	W
2: Rate Counter Period	0x2008	D0-D15: Rate Counter integration time (0)	R/W
3: Overflow-0	0x200c	D0-D31: Overflow bits 0:31	R
4: Overflow-1	0x2010	D0-D31: Overflow bits 32:63	R
5: Overflow-2	0x2014	D0-D20: Overflow bits 64:84	R
	0x2018 – 0x201c	Reserved for future control and status registers	N/A

Counter Value Registers

ID: Name	*Address*	*Functionality*	*Access*
0: Clock Counter-0	0x2020	D0-D31: Clock ticks while triggers are enabled - 32 LSB	R
1: Clock Counter-1	0x2024	D0-D7: Clock ticks while triggers are enabled - 8 MSB	R
2: Event Counter	0x2028	D0-D23: Number of triggers issued	R
Trigger Component Counters			
3: Bi-Focal	0x202c		
4: Discriminator	0x2030		
5: Internal	0x2034		
6: External	0x2038		
7: GPS	0x203c		

8: LED	0x2040		
Trigger Component Live Counters (only count when TB is LIVE, not BUSY)			
9: Bi-Focal	0x2044		
10: Discriminator	0x2048		
11: Internal	0x204c		
12: External	0x2050		
13: GPS	0x2054		
14: LED	0x2058		
Busy Logic Counters			
15: TB Busy Counter-0	0x205c	D0-D31: Clock ticks while TB is BUSY - 32 LSB	R
16: TB Busy Counter-1	0x2060	D0-D7: Clock ticks while TB is BUSY - 8 MSB	R
17: CoBo Busy Counter-0	0x2064	D0-D31: Clock ticks while CoBo is BUSY - 32 LSB	R
18: CoBo Busy Counter-1	0x2068	D0-D7: Clock ticks while CoBo is BUSY - 8 MSB	R
19: Transit Busy Counter-0	0x206c	D0-D31: Clock ticks while TB is BUSY - 32 LSB	R
20: Transit Busy Counter-1	0x2070	D0-D7: Clock ticks while TB is BUSY - 8 MSB	R
21: Buffer Busy Counter-0	0x2074	D0-D31: Clock ticks while Buffer is BUSY - 32 LSB	R
22: Buffer Busy Counter-1	0x2078	D0-D7: Clock ticks while Buffer is BUSY - 8 MSB	R
23: Mem Full Counter-0	0x207c	D0-D31: Clock ticks while Mem is FULL - 32 LSB	R
24: Mem Full Counter-1	0x2080	D0-D7: Clock ticks while Mem is FULL - 8 MSB	R
25: Mem Reading Counter-0	0x2084	D0-D31: Clock ticks while Mem is BUSY - 32 LSB	R
26: Mem Reading Counter-1	0x2088	D0-D7: Clock ticks while Mem is BUSY - 8 MSB	R
27: Mem Writing Counter-0	0x208c	D0-D31: Clock ticks while Mem is BUSY - 32 LSB	R
28: Mem Writing Counter-1	0x2090	D0-D7: Clock ticks while Mem is BUSY - 8 MSB	R
Discriminator Rate Counters			
29: IO#0 Rate	0x2094		
30: IO#1 Rate	0x2098		
31: IO#2 Rate	0x209c		
32: IO#3 Rate	0x20a0		
33: IO#4 Rate	0x20a4		
34: IO#5 Rate	0x20a8		
35: IO#6 Rate	0x20ac		
36: IO#7 Rate	0x20b0		
37: IO#8 Rate	0x20b4		
38: IO#9 Rate	0x20b8		
39: IO#10 Rate	0x20bc		
40: IO#11 Rate	0x20c0		
41: IO#12 Rate	0x20c4		
42: IO#13 Rate	0x20c8		
43: IO#14 Rate	0x20cc		
44: IO#15 Rate	0x20d0		
45: IO#16 Rate	0x20d4		
46: IO#17 Rate	0x20d8		
47: IO#18 Rate	0x20dc		
48: IO#19 Rate	0x20e0		
49: IO#20 Rate	0x20e4		
50: IO#21 Rate	0x20e8		
51: IO#22 Rate	0x20ec		
52: IO#23 Rate	0x20f0		
53: IO#24 Rate	0x20f4		
54: IO#25 Rate	0x20f8		
55: IO#26 Rate	0x20fc		
56: IO#27 Rate	0x2100		
57: IO#28 Rate	0x2104		
58: IO#29 Rate	0x2108		

59: IO#30 Rate	0x210c		
60: IO#31 Rate	0x2110		
61: IO#32 Rate	0x2114		
62: IO#33 Rate	0x2118		
63: IO#34 Rate	0x211c		
64: IO#35 Rate	0x2120		
65: IO#36 Rate	0x2124		
66: IO#37 Rate	0x2128		
67: IO#38 Rate	0x212c		
68: IO#39 Rate	0x2130		
69: IO#40 Rate	0x2134		
70: IO#41 Rate	0x2138		
71: IO#42 Rate	0x213c		
72: IO#43 Rate	0x2140		
73: IO#44 Rate	0x2144		
74: IO#45 Rate	0x2148		
75: IO#46 Rate	0x214c		
76: IO#47 Rate	0x2150		
77: IO#48 Rate	0x2154		
78: IO#49 Rate	0x2158		
79: IO#50 Rate	0x215c		
80: IO#51 Rate	0x2160		
81: IO#52 Rate	0x2164		
82: IO#53 Rate	0x2168		
83: IO#54 Rate	0x216c		
84: IO#55 Rate	0x2170		
85: IO#56 Rate	0x2174		
86: IO#57 Rate	0x2178		
87: IO#58 Rate	0x217c		
88: IO#59 Rate	0x2180		
89: IO#60 Rate	0x2184		
90: IO#61 Rate	0x2188		
91: IO#62 Rate	0x218c		
92: IO#63 Rate	0x2190		

Data Storage Registers

Block Memory Control and Status Registers

ID: Name	*Address*	*Functionality*	*Access*
0: Block Memory Enable	0x3000	D0: Enables (1) or Disables (0) use of the Block Memory	R/W
1: Memory Start Address	0x3004	D0-D14: Block Memory address to start writing	R/W
2: Events Written	0x3008	D0-D12: Number of events written to the Block Memory	R
3: Readout Start	0x300c	D0: Prepare for read access to Block Memory	W
4: Memory Block Select	0x3010	D0-D1: Two MSB of Block Memory address	R/W
5: Readout Done	0x3014	D0: Read access to Block Memory is complete	W

Block Memory Access Registers

5 words are written to the block memory for every event. The 1st event is written starting at the "Memory Start Address". The 2nd event is written starting at "Memory Start Address + 5", etc…. The block memory has space for 20000 words, so 3999 events can be stored in the block memory before the "Memory Full" logic is triggered. 20000 is a 15-bit number, so the block memory has 15-bit address buses.
The Ethernet interface protocol uses 16-bit addresses. The MSB (the "8" in 0x8000) is used to select the block memory. The

2 LSB are never accessible so only 13 bits are actually available to the user. The user therefore uses the Memory Block Select register to specify the 2 MSB of the 15-bit address

The following table assumes that Memory Start Address is set to zero.

Name	*Block Select*	*Address*	*Functionality*	*Access*
1st Event Word-1	0	0x8000	D0-D23: Event number	R
1st Event Word-2	0	0x8004	D0-D31: Clock Counter value 32 LSB	R
1st Event Word-3	0	0x8008	D0-D7: Clock Counter value 8 MSB D8-D25: Unused - set to zero D26: Bi-focal trigger was enabled and fired D27: Discriminator test trigger was enabled and fired D28: Internal trigger was enabled and fired D29: External trigger was enabled and fired D30: GPS trigger was enabled and fired D31: LED trigger was enabled and fired	R
1st Event Word-4	0	0x800C	D0-D31: Stretched discriminator bits 0:31	R
1st Event Word-5	0	0x8010	D0-D31: Stretched discriminator bits 32:63	R
2nd Event Words 1-5	0	0x8014-0x8024	Same format as 1st event	R
1639th Event Words 1&2	0	0xFFF8 – 0xFFFC	Same format as 1st event	R
1639th Event Words 3-5	1	0x8000 – 0x8008	Same format as 1st event	R
1640th Event Words 1-5	1	0x800C – 0x801C	Same format as 1st event	R
Etc…				