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# Static Timing Analysis

|  |  |
| --- | --- |
| **Project :** | Rover\_holonomic\_Motors0308 |
| **Build Time :** | 03/08/19 14:11:05 |
| **Device :** | CY8C5888LTI-LP097 |
| **Temperature :** | -40C - 85/125C |
| **VDDA :** | 5.00 |
| **VDDABUF :** | 5.00 |
| **VDDD :** | 5.00 |
| **VDDIO0 :** | 5.00 |
| **VDDIO1 :** | 5.00 |
| **VDDIO2 :** | 5.00 |
| **VDDIO3 :** | 5.00 |
| **VUSB :** | 5.00 |
| **Voltage :** | 5.0 |

[Expand All](#gjdgxs) | [Collapse All](#gjdgxs) | [Show All Paths](#gjdgxs) | [Hide All Paths](#gjdgxs)

[**+ Timing Violation Section**](#gjdgxs)

No Timing Violations

[**+ Clock Summary Section**](#gjdgxs)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Clock | Domain | Nominal Frequency | Required Frequency | Maximum Frequency | Violation |
| CyILO | CyILO | 1.000 kHz | 1.000 kHz | N/A |  |
| CyIMO | CyIMO | 3.000 MHz | 3.000 MHz | N/A |  |
| CyMASTER\_CLK | CyMASTER\_CLK | 24.000 MHz | 24.000 MHz | N/A |  |
| CyBUS\_CLK | CyMASTER\_CLK | 24.000 MHz | 24.000 MHz | 63.902 MHz |  |
| Clock\_1 | CyMASTER\_CLK | 1.000 MHz | 1.000 MHz | 62.716 MHz |  |
| UART\_IntClock | CyMASTER\_CLK | 923.077 kHz | 923.077 kHz | 49.251 MHz |  |
| CyPLL\_OUT | CyPLL\_OUT | 24.000 MHz | 24.000 MHz | N/A |  |

[**+ Register to Register Section**](#gjdgxs)

[**+ Setup Subsection**](#gjdgxs)

[**+ Source Clock : Clock\_1 : Positive edge(Required Frequency 1 MHz)**](#gjdgxs)

[**+ Destination Clock : Clock\_1 : Positive edge(Required Frequency 1 MHz)**](#gjdgxs)

Path Delay Requirement : 1000ns(1 MHz)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Source | Destination | FMax | Delay (ns) | Slack (ns) | Violation |
| \PWM1:PWMUDB:sP16:pwmdp:u0\/z0 | \PWM1:PWMUDB:sP16:pwmdp:u1\/ci | 62.716 MHz | 15.945 | 984.055 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell1 | U(1,4) | 1 | \PWM1:PWMUDB:sP16:pwmdp:u0\ | \PWM1:PWMUDB:sP16:pwmdp:u0\/clock | \PWM1:PWMUDB:sP16:pwmdp:u0\/z0 | 0.760 | | Route |  | 1 | \PWM1:PWMUDB:sP16:pwmdp:u0.z0\_\_sig\ | \PWM1:PWMUDB:sP16:pwmdp:u0\/z0 | \PWM1:PWMUDB:sP16:pwmdp:u1\/z0i | 0.000 | | datapathcell2 | U(0,4) | 1 | \PWM1:PWMUDB:sP16:pwmdp:u1\ | \PWM1:PWMUDB:sP16:pwmdp:u1\/z0i | \PWM1:PWMUDB:sP16:pwmdp:u1\/z0\_comb | 2.740 | | Route |  | 1 | \PWM1:PWMUDB:tc\_i\ | \PWM1:PWMUDB:sP16:pwmdp:u1\/z0\_comb | \PWM1:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | 3.085 | | datapathcell1 | U(1,4) | 1 | \PWM1:PWMUDB:sP16:pwmdp:u0\ | \PWM1:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | \PWM1:PWMUDB:sP16:pwmdp:u0\/co\_msb | 5.130 | | Route |  | 1 | \PWM1:PWMUDB:sP16:pwmdp:u0.co\_msb\_\_sig\ | \PWM1:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM1:PWMUDB:sP16:pwmdp:u1\/ci | 0.000 | | datapathcell2 | U(0,4) | 1 | \PWM1:PWMUDB:sP16:pwmdp:u1\ |  | SETUP | 4.230 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \PWM4:PWMUDB:sP16:pwmdp:u0\/z0 | \PWM4:PWMUDB:sP16:pwmdp:u1\/ci | 62.716 MHz | 15.945 | 984.055 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell11 | U(3,4) | 1 | \PWM4:PWMUDB:sP16:pwmdp:u0\ | \PWM4:PWMUDB:sP16:pwmdp:u0\/clock | \PWM4:PWMUDB:sP16:pwmdp:u0\/z0 | 0.760 | | Route |  | 1 | \PWM4:PWMUDB:sP16:pwmdp:u0.z0\_\_sig\ | \PWM4:PWMUDB:sP16:pwmdp:u0\/z0 | \PWM4:PWMUDB:sP16:pwmdp:u1\/z0i | 0.000 | | datapathcell12 | U(2,4) | 1 | \PWM4:PWMUDB:sP16:pwmdp:u1\ | \PWM4:PWMUDB:sP16:pwmdp:u1\/z0i | \PWM4:PWMUDB:sP16:pwmdp:u1\/z0\_comb | 2.740 | | Route |  | 1 | \PWM4:PWMUDB:tc\_i\ | \PWM4:PWMUDB:sP16:pwmdp:u1\/z0\_comb | \PWM4:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | 3.085 | | datapathcell11 | U(3,4) | 1 | \PWM4:PWMUDB:sP16:pwmdp:u0\ | \PWM4:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | \PWM4:PWMUDB:sP16:pwmdp:u0\/co\_msb | 5.130 | | Route |  | 1 | \PWM4:PWMUDB:sP16:pwmdp:u0.co\_msb\_\_sig\ | \PWM4:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM4:PWMUDB:sP16:pwmdp:u1\/ci | 0.000 | | datapathcell12 | U(2,4) | 1 | \PWM4:PWMUDB:sP16:pwmdp:u1\ |  | SETUP | 4.230 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \PWM5:PWMUDB:sP16:pwmdp:u0\/z0 | \PWM5:PWMUDB:sP16:pwmdp:u1\/ci | 63.391 MHz | 15.775 | 984.225 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell5 | U(2,3) | 1 | \PWM5:PWMUDB:sP16:pwmdp:u0\ | \PWM5:PWMUDB:sP16:pwmdp:u0\/clock | \PWM5:PWMUDB:sP16:pwmdp:u0\/z0 | 0.760 | | Route |  | 1 | \PWM5:PWMUDB:sP16:pwmdp:u0.z0\_\_sig\ | \PWM5:PWMUDB:sP16:pwmdp:u0\/z0 | \PWM5:PWMUDB:sP16:pwmdp:u1\/z0i | 0.000 | | datapathcell6 | U(3,3) | 1 | \PWM5:PWMUDB:sP16:pwmdp:u1\ | \PWM5:PWMUDB:sP16:pwmdp:u1\/z0i | \PWM5:PWMUDB:sP16:pwmdp:u1\/z0\_comb | 2.740 | | Route |  | 1 | \PWM5:PWMUDB:tc\_i\ | \PWM5:PWMUDB:sP16:pwmdp:u1\/z0\_comb | \PWM5:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | 2.915 | | datapathcell5 | U(2,3) | 1 | \PWM5:PWMUDB:sP16:pwmdp:u0\ | \PWM5:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | \PWM5:PWMUDB:sP16:pwmdp:u0\/co\_msb | 5.130 | | Route |  | 1 | \PWM5:PWMUDB:sP16:pwmdp:u0.co\_msb\_\_sig\ | \PWM5:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM5:PWMUDB:sP16:pwmdp:u1\/ci | 0.000 | | datapathcell6 | U(3,3) | 1 | \PWM5:PWMUDB:sP16:pwmdp:u1\ |  | SETUP | 4.230 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \PWM3:PWMUDB:sP16:pwmdp:u0\/z0 | \PWM3:PWMUDB:sP16:pwmdp:u1\/ci | 63.391 MHz | 15.775 | 984.225 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell7 | U(0,5) | 1 | \PWM3:PWMUDB:sP16:pwmdp:u0\ | \PWM3:PWMUDB:sP16:pwmdp:u0\/clock | \PWM3:PWMUDB:sP16:pwmdp:u0\/z0 | 0.760 | | Route |  | 1 | \PWM3:PWMUDB:sP16:pwmdp:u0.z0\_\_sig\ | \PWM3:PWMUDB:sP16:pwmdp:u0\/z0 | \PWM3:PWMUDB:sP16:pwmdp:u1\/z0i | 0.000 | | datapathcell8 | U(1,5) | 1 | \PWM3:PWMUDB:sP16:pwmdp:u1\ | \PWM3:PWMUDB:sP16:pwmdp:u1\/z0i | \PWM3:PWMUDB:sP16:pwmdp:u1\/z0\_comb | 2.740 | | Route |  | 1 | \PWM3:PWMUDB:tc\_i\ | \PWM3:PWMUDB:sP16:pwmdp:u1\/z0\_comb | \PWM3:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | 2.915 | | datapathcell7 | U(0,5) | 1 | \PWM3:PWMUDB:sP16:pwmdp:u0\ | \PWM3:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | \PWM3:PWMUDB:sP16:pwmdp:u0\/co\_msb | 5.130 | | Route |  | 1 | \PWM3:PWMUDB:sP16:pwmdp:u0.co\_msb\_\_sig\ | \PWM3:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM3:PWMUDB:sP16:pwmdp:u1\/ci | 0.000 | | datapathcell8 | U(1,5) | 1 | \PWM3:PWMUDB:sP16:pwmdp:u1\ |  | SETUP | 4.230 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \PWM2:PWMUDB:sP16:pwmdp:u0\/z0 | \PWM2:PWMUDB:sP16:pwmdp:u1\/ci | 63.391 MHz | 15.775 | 984.225 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell9 | U(0,3) | 1 | \PWM2:PWMUDB:sP16:pwmdp:u0\ | \PWM2:PWMUDB:sP16:pwmdp:u0\/clock | \PWM2:PWMUDB:sP16:pwmdp:u0\/z0 | 0.760 | | Route |  | 1 | \PWM2:PWMUDB:sP16:pwmdp:u0.z0\_\_sig\ | \PWM2:PWMUDB:sP16:pwmdp:u0\/z0 | \PWM2:PWMUDB:sP16:pwmdp:u1\/z0i | 0.000 | | datapathcell10 | U(1,3) | 1 | \PWM2:PWMUDB:sP16:pwmdp:u1\ | \PWM2:PWMUDB:sP16:pwmdp:u1\/z0i | \PWM2:PWMUDB:sP16:pwmdp:u1\/z0\_comb | 2.740 | | Route |  | 1 | \PWM2:PWMUDB:tc\_i\ | \PWM2:PWMUDB:sP16:pwmdp:u1\/z0\_comb | \PWM2:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | 2.915 | | datapathcell9 | U(0,3) | 1 | \PWM2:PWMUDB:sP16:pwmdp:u0\ | \PWM2:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | \PWM2:PWMUDB:sP16:pwmdp:u0\/co\_msb | 5.130 | | Route |  | 1 | \PWM2:PWMUDB:sP16:pwmdp:u0.co\_msb\_\_sig\ | \PWM2:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM2:PWMUDB:sP16:pwmdp:u1\/ci | 0.000 | | datapathcell10 | U(1,3) | 1 | \PWM2:PWMUDB:sP16:pwmdp:u1\ |  | SETUP | 4.230 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \PWM6:PWMUDB:sP16:pwmdp:u0\/z0 | \PWM6:PWMUDB:sP16:pwmdp:u1\/ci | 64.675 MHz | 15.462 | 984.538 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell3 | U(1,2) | 1 | \PWM6:PWMUDB:sP16:pwmdp:u0\ | \PWM6:PWMUDB:sP16:pwmdp:u0\/clock | \PWM6:PWMUDB:sP16:pwmdp:u0\/z0 | 0.760 | | Route |  | 1 | \PWM6:PWMUDB:sP16:pwmdp:u0.z0\_\_sig\ | \PWM6:PWMUDB:sP16:pwmdp:u0\/z0 | \PWM6:PWMUDB:sP16:pwmdp:u1\/z0i | 0.000 | | datapathcell4 | U(0,2) | 1 | \PWM6:PWMUDB:sP16:pwmdp:u1\ | \PWM6:PWMUDB:sP16:pwmdp:u1\/z0i | \PWM6:PWMUDB:sP16:pwmdp:u1\/z0\_comb | 2.740 | | Route |  | 1 | \PWM6:PWMUDB:tc\_i\ | \PWM6:PWMUDB:sP16:pwmdp:u1\/z0\_comb | \PWM6:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | 2.602 | | datapathcell3 | U(1,2) | 1 | \PWM6:PWMUDB:sP16:pwmdp:u0\ | \PWM6:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | \PWM6:PWMUDB:sP16:pwmdp:u0\/co\_msb | 5.130 | | Route |  | 1 | \PWM6:PWMUDB:sP16:pwmdp:u0.co\_msb\_\_sig\ | \PWM6:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM6:PWMUDB:sP16:pwmdp:u1\/ci | 0.000 | | datapathcell4 | U(0,2) | 1 | \PWM6:PWMUDB:sP16:pwmdp:u1\ |  | SETUP | 4.230 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \PWM1:PWMUDB:sP16:pwmdp:u1\/z0\_comb | \PWM1:PWMUDB:sP16:pwmdp:u1\/ci | 67.866 MHz | 14.735 | 985.265 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell2 | U(0,4) | 1 | \PWM1:PWMUDB:sP16:pwmdp:u1\ | \PWM1:PWMUDB:sP16:pwmdp:u1\/clock | \PWM1:PWMUDB:sP16:pwmdp:u1\/z0\_comb | 2.290 | | Route |  | 1 | \PWM1:PWMUDB:tc\_i\ | \PWM1:PWMUDB:sP16:pwmdp:u1\/z0\_comb | \PWM1:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | 3.085 | | datapathcell1 | U(1,4) | 1 | \PWM1:PWMUDB:sP16:pwmdp:u0\ | \PWM1:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | \PWM1:PWMUDB:sP16:pwmdp:u0\/co\_msb | 5.130 | | Route |  | 1 | \PWM1:PWMUDB:sP16:pwmdp:u0.co\_msb\_\_sig\ | \PWM1:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM1:PWMUDB:sP16:pwmdp:u1\/ci | 0.000 | | datapathcell2 | U(0,4) | 1 | \PWM1:PWMUDB:sP16:pwmdp:u1\ |  | SETUP | 4.230 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \PWM4:PWMUDB:sP16:pwmdp:u1\/z0\_comb | \PWM4:PWMUDB:sP16:pwmdp:u1\/ci | 67.866 MHz | 14.735 | 985.265 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell12 | U(2,4) | 1 | \PWM4:PWMUDB:sP16:pwmdp:u1\ | \PWM4:PWMUDB:sP16:pwmdp:u1\/clock | \PWM4:PWMUDB:sP16:pwmdp:u1\/z0\_comb | 2.290 | | Route |  | 1 | \PWM4:PWMUDB:tc\_i\ | \PWM4:PWMUDB:sP16:pwmdp:u1\/z0\_comb | \PWM4:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | 3.085 | | datapathcell11 | U(3,4) | 1 | \PWM4:PWMUDB:sP16:pwmdp:u0\ | \PWM4:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | \PWM4:PWMUDB:sP16:pwmdp:u0\/co\_msb | 5.130 | | Route |  | 1 | \PWM4:PWMUDB:sP16:pwmdp:u0.co\_msb\_\_sig\ | \PWM4:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM4:PWMUDB:sP16:pwmdp:u1\/ci | 0.000 | | datapathcell12 | U(2,4) | 1 | \PWM4:PWMUDB:sP16:pwmdp:u1\ |  | SETUP | 4.230 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \PWM5:PWMUDB:sP16:pwmdp:u1\/z0\_comb | \PWM5:PWMUDB:sP16:pwmdp:u1\/ci | 68.658 MHz | 14.565 | 985.435 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell6 | U(3,3) | 1 | \PWM5:PWMUDB:sP16:pwmdp:u1\ | \PWM5:PWMUDB:sP16:pwmdp:u1\/clock | \PWM5:PWMUDB:sP16:pwmdp:u1\/z0\_comb | 2.290 | | Route |  | 1 | \PWM5:PWMUDB:tc\_i\ | \PWM5:PWMUDB:sP16:pwmdp:u1\/z0\_comb | \PWM5:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | 2.915 | | datapathcell5 | U(2,3) | 1 | \PWM5:PWMUDB:sP16:pwmdp:u0\ | \PWM5:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | \PWM5:PWMUDB:sP16:pwmdp:u0\/co\_msb | 5.130 | | Route |  | 1 | \PWM5:PWMUDB:sP16:pwmdp:u0.co\_msb\_\_sig\ | \PWM5:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM5:PWMUDB:sP16:pwmdp:u1\/ci | 0.000 | | datapathcell6 | U(3,3) | 1 | \PWM5:PWMUDB:sP16:pwmdp:u1\ |  | SETUP | 4.230 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \PWM3:PWMUDB:sP16:pwmdp:u1\/z0\_comb | \PWM3:PWMUDB:sP16:pwmdp:u1\/ci | 68.658 MHz | 14.565 | 985.435 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell8 | U(1,5) | 1 | \PWM3:PWMUDB:sP16:pwmdp:u1\ | \PWM3:PWMUDB:sP16:pwmdp:u1\/clock | \PWM3:PWMUDB:sP16:pwmdp:u1\/z0\_comb | 2.290 | | Route |  | 1 | \PWM3:PWMUDB:tc\_i\ | \PWM3:PWMUDB:sP16:pwmdp:u1\/z0\_comb | \PWM3:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | 2.915 | | datapathcell7 | U(0,5) | 1 | \PWM3:PWMUDB:sP16:pwmdp:u0\ | \PWM3:PWMUDB:sP16:pwmdp:u0\/cs\_addr\_2 | \PWM3:PWMUDB:sP16:pwmdp:u0\/co\_msb | 5.130 | | Route |  | 1 | \PWM3:PWMUDB:sP16:pwmdp:u0.co\_msb\_\_sig\ | \PWM3:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM3:PWMUDB:sP16:pwmdp:u1\/ci | 0.000 | | datapathcell8 | U(1,5) | 1 | \PWM3:PWMUDB:sP16:pwmdp:u1\ |  | SETUP | 4.230 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |

[**+ Source Clock : CyBUS\_CLK : Positive edge(Required Frequency 24 MHz)**](#gjdgxs)

[**+ Destination Clock : UART\_IntClock : Positive edge(Required Frequency 923.077 kHz)**](#gjdgxs)

Path Delay Requirement : 41.6667ns(24 MHz)

Affects clock : CyMASTER\_CLK

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Source | Destination | FMax | Delay (ns) | Slack (ns) | Violation |
| Rx\_1(0)/fb | \UART:BUART:sRX:RxShifter:u0\/route\_si | 63.902 MHz | 15.649 | 26.018 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell8 | P12[6] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.009 | | Route |  | 1 | Net\_6168 | Rx\_1(0)/fb | \UART:BUART:rx\_postpoll\/main\_1 | 4.594 | | macrocell12 | U(1,0) | 1 | \UART:BUART:rx\_postpoll\ | \UART:BUART:rx\_postpoll\/main\_1 | \UART:BUART:rx\_postpoll\/q | 3.350 | | Route |  | 1 | \UART:BUART:rx\_postpoll\ | \UART:BUART:rx\_postpoll\/q | \UART:BUART:sRX:RxShifter:u0\/route\_si | 2.226 | | datapathcell15 | U(1,0) | 1 | \UART:BUART:sRX:RxShifter:u0\ |  | SETUP | 3.470 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| Rx\_1(0)/fb | \UART:BUART:rx\_state\_2\/main\_8 | 84.048 MHz | 11.898 | 29.769 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell8 | P12[6] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.009 | | Route |  | 1 | Net\_6168 | Rx\_1(0)/fb | \UART:BUART:rx\_state\_2\/main\_8 | 6.379 | | macrocell48 | U(1,2) | 1 | \UART:BUART:rx\_state\_2\ |  | SETUP | 3.510 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| Rx\_1(0)/fb | \UART:BUART:rx\_state\_0\/main\_9 | 90.942 MHz | 10.996 | 30.671 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell8 | P12[6] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.009 | | Route |  | 1 | Net\_6168 | Rx\_1(0)/fb | \UART:BUART:rx\_state\_0\/main\_9 | 5.477 | | macrocell45 | U(1,1) | 1 | \UART:BUART:rx\_state\_0\ |  | SETUP | 3.510 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| Rx\_1(0)/fb | \UART:BUART:rx\_status\_3\/main\_6 | 90.942 MHz | 10.996 | 30.671 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell8 | P12[6] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.009 | | Route |  | 1 | Net\_6168 | Rx\_1(0)/fb | \UART:BUART:rx\_status\_3\/main\_6 | 5.477 | | macrocell53 | U(1,1) | 1 | \UART:BUART:rx\_status\_3\ |  | SETUP | 3.510 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| Rx\_1(0)/fb | \UART:BUART:pollcount\_1\/main\_3 | 98.883 MHz | 10.113 | 31.554 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell8 | P12[6] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.009 | | Route |  | 1 | Net\_6168 | Rx\_1(0)/fb | \UART:BUART:pollcount\_1\/main\_3 | 4.594 | | macrocell51 | U(1,0) | 1 | \UART:BUART:pollcount\_1\ |  | SETUP | 3.510 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| Rx\_1(0)/fb | \UART:BUART:pollcount\_0\/main\_2 | 98.883 MHz | 10.113 | 31.554 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell8 | P12[6] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.009 | | Route |  | 1 | Net\_6168 | Rx\_1(0)/fb | \UART:BUART:pollcount\_0\/main\_2 | 4.594 | | macrocell52 | U(1,0) | 1 | \UART:BUART:pollcount\_0\ |  | SETUP | 3.510 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| Rx\_1(0)/fb | \UART:BUART:rx\_last\/main\_0 | 98.883 MHz | 10.113 | 31.554 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell8 | P12[6] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.009 | | Route |  | 1 | Net\_6168 | Rx\_1(0)/fb | \UART:BUART:rx\_last\/main\_0 | 4.594 | | macrocell54 | U(1,0) | 1 | \UART:BUART:rx\_last\ |  | SETUP | 3.510 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |

[**+ Source Clock : UART\_IntClock : Positive edge(Required Frequency 923.077 kHz)**](#gjdgxs)

[**+ Destination Clock : UART\_IntClock : Positive edge(Required Frequency 923.077 kHz)**](#gjdgxs)

Path Delay Requirement : 1083.33ns(923.077 kHz)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Source | Destination | FMax | Delay (ns) | Slack (ns) | Violation |
| \UART:BUART:rx\_state\_2\/q | \UART:BUART:sRX:RxBitCounter\/load | 49.251 MHz | 20.304 | 1063.029 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell48 | U(1,2) | 1 | \UART:BUART:rx\_state\_2\ | \UART:BUART:rx\_state\_2\/clock\_0 | \UART:BUART:rx\_state\_2\/q | 1.250 | | Route |  | 1 | \UART:BUART:rx\_state\_2\ | \UART:BUART:rx\_state\_2\/q | \UART:BUART:rx\_counter\_load\/main\_3 | 8.045 | | macrocell11 | U(1,1) | 1 | \UART:BUART:rx\_counter\_load\ | \UART:BUART:rx\_counter\_load\/main\_3 | \UART:BUART:rx\_counter\_load\/q | 3.350 | | Route |  | 1 | \UART:BUART:rx\_counter\_load\ | \UART:BUART:rx\_counter\_load\/q | \UART:BUART:sRX:RxBitCounter\/load | 2.299 | | count7cell | U(1,1) | 1 | \UART:BUART:sRX:RxBitCounter\ |  | SETUP | 5.360 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART:BUART:tx\_state\_0\/q | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 55.782 MHz | 17.927 | 1065.406 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell41 | U(0,2) | 1 | \UART:BUART:tx\_state\_0\ | \UART:BUART:tx\_state\_0\/clock\_0 | \UART:BUART:tx\_state\_0\/q | 1.250 | | Route |  | 1 | \UART:BUART:tx\_state\_0\ | \UART:BUART:tx\_state\_0\/q | \UART:BUART:counter\_load\_not\/main\_1 | 4.898 | | macrocell8 | U(0,0) | 1 | \UART:BUART:counter\_load\_not\ | \UART:BUART:counter\_load\_not\/main\_1 | \UART:BUART:counter\_load\_not\/q | 3.350 | | Route |  | 1 | \UART:BUART:counter\_load\_not\ | \UART:BUART:counter\_load\_not\/q | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 2.239 | | datapathcell14 | U(0,0) | 1 | \UART:BUART:sTX:sCLOCK:TxBitClkGen\ |  | SETUP | 6.190 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART:BUART:tx\_state\_1\/q | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 58.319 MHz | 17.147 | 1066.186 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell40 | U(0,1) | 1 | \UART:BUART:tx\_state\_1\ | \UART:BUART:tx\_state\_1\/clock\_0 | \UART:BUART:tx\_state\_1\/q | 1.250 | | Route |  | 1 | \UART:BUART:tx\_state\_1\ | \UART:BUART:tx\_state\_1\/q | \UART:BUART:counter\_load\_not\/main\_0 | 4.118 | | macrocell8 | U(0,0) | 1 | \UART:BUART:counter\_load\_not\ | \UART:BUART:counter\_load\_not\/main\_0 | \UART:BUART:counter\_load\_not\/q | 3.350 | | Route |  | 1 | \UART:BUART:counter\_load\_not\ | \UART:BUART:counter\_load\_not\/q | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 2.239 | | datapathcell14 | U(0,0) | 1 | \UART:BUART:sTX:sCLOCK:TxBitClkGen\ |  | SETUP | 6.190 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART:BUART:tx\_state\_2\/q | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 63.646 MHz | 15.712 | 1067.621 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell42 | U(0,0) | 1 | \UART:BUART:tx\_state\_2\ | \UART:BUART:tx\_state\_2\/clock\_0 | \UART:BUART:tx\_state\_2\/q | 1.250 | | Route |  | 1 | \UART:BUART:tx\_state\_2\ | \UART:BUART:tx\_state\_2\/q | \UART:BUART:counter\_load\_not\/main\_3 | 2.683 | | macrocell8 | U(0,0) | 1 | \UART:BUART:counter\_load\_not\ | \UART:BUART:counter\_load\_not\/main\_3 | \UART:BUART:counter\_load\_not\/q | 3.350 | | Route |  | 1 | \UART:BUART:counter\_load\_not\ | \UART:BUART:counter\_load\_not\/q | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 2.239 | | datapathcell14 | U(0,0) | 1 | \UART:BUART:sTX:sCLOCK:TxBitClkGen\ |  | SETUP | 6.190 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART:BUART:sTX:sCLOCK:TxBitClkGen\/ce0\_reg | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 64.809 MHz | 15.430 | 1067.903 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell14 | U(0,0) | 1 | \UART:BUART:sTX:sCLOCK:TxBitClkGen\ | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/clock | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/ce0\_reg | 0.190 | | Route |  | 1 | \UART:BUART:tx\_bitclk\_enable\_pre\ | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/ce0\_reg | \UART:BUART:counter\_load\_not\/main\_2 | 3.461 | | macrocell8 | U(0,0) | 1 | \UART:BUART:counter\_load\_not\ | \UART:BUART:counter\_load\_not\/main\_2 | \UART:BUART:counter\_load\_not\/q | 3.350 | | Route |  | 1 | \UART:BUART:counter\_load\_not\ | \UART:BUART:counter\_load\_not\/q | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 2.239 | | datapathcell14 | U(0,0) | 1 | \UART:BUART:sTX:sCLOCK:TxBitClkGen\ |  | SETUP | 6.190 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART:BUART:rx\_state\_0\/q | \UART:BUART:sRX:RxBitCounter\/load | 65.096 MHz | 15.362 | 1067.971 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell45 | U(1,1) | 1 | \UART:BUART:rx\_state\_0\ | \UART:BUART:rx\_state\_0\/clock\_0 | \UART:BUART:rx\_state\_0\/q | 1.250 | | Route |  | 1 | \UART:BUART:rx\_state\_0\ | \UART:BUART:rx\_state\_0\/q | \UART:BUART:rx\_counter\_load\/main\_1 | 3.103 | | macrocell11 | U(1,1) | 1 | \UART:BUART:rx\_counter\_load\ | \UART:BUART:rx\_counter\_load\/main\_1 | \UART:BUART:rx\_counter\_load\/q | 3.350 | | Route |  | 1 | \UART:BUART:rx\_counter\_load\ | \UART:BUART:rx\_counter\_load\/q | \UART:BUART:sRX:RxBitCounter\/load | 2.299 | | count7cell | U(1,1) | 1 | \UART:BUART:sRX:RxBitCounter\ |  | SETUP | 5.360 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART:BUART:tx\_ctrl\_mark\_last\/q | \UART:BUART:sRX:RxBitCounter\/load | 66.551 MHz | 15.026 | 1068.307 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell44 | U(1,1) | 1 | \UART:BUART:tx\_ctrl\_mark\_last\ | \UART:BUART:tx\_ctrl\_mark\_last\/clock\_0 | \UART:BUART:tx\_ctrl\_mark\_last\/q | 1.250 | | Route |  | 1 | \UART:BUART:tx\_ctrl\_mark\_last\ | \UART:BUART:tx\_ctrl\_mark\_last\/q | \UART:BUART:rx\_counter\_load\/main\_0 | 2.767 | | macrocell11 | U(1,1) | 1 | \UART:BUART:rx\_counter\_load\ | \UART:BUART:rx\_counter\_load\/main\_0 | \UART:BUART:rx\_counter\_load\/q | 3.350 | | Route |  | 1 | \UART:BUART:rx\_counter\_load\ | \UART:BUART:rx\_counter\_load\/q | \UART:BUART:sRX:RxBitCounter\/load | 2.299 | | count7cell | U(1,1) | 1 | \UART:BUART:sRX:RxBitCounter\ |  | SETUP | 5.360 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART:BUART:rx\_state\_3\/q | \UART:BUART:sRX:RxBitCounter\/load | 67.308 MHz | 14.857 | 1068.476 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell47 | U(1,1) | 1 | \UART:BUART:rx\_state\_3\ | \UART:BUART:rx\_state\_3\/clock\_0 | \UART:BUART:rx\_state\_3\/q | 1.250 | | Route |  | 1 | \UART:BUART:rx\_state\_3\ | \UART:BUART:rx\_state\_3\/q | \UART:BUART:rx\_counter\_load\/main\_2 | 2.598 | | macrocell11 | U(1,1) | 1 | \UART:BUART:rx\_counter\_load\ | \UART:BUART:rx\_counter\_load\/main\_2 | \UART:BUART:rx\_counter\_load\/q | 3.350 | | Route |  | 1 | \UART:BUART:rx\_counter\_load\ | \UART:BUART:rx\_counter\_load\/q | \UART:BUART:sRX:RxBitCounter\/load | 2.299 | | count7cell | U(1,1) | 1 | \UART:BUART:sRX:RxBitCounter\ |  | SETUP | 5.360 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART:BUART:sTX:TxShifter:u0\/f0\_blk\_stat\_comb | \UART:BUART:sTX:TxSts\/status\_0 | 69.300 MHz | 14.430 | 1068.903 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell13 | U(0,1) | 1 | \UART:BUART:sTX:TxShifter:u0\ | \UART:BUART:sTX:TxShifter:u0\/clock | \UART:BUART:sTX:TxShifter:u0\/f0\_blk\_stat\_comb | 3.580 | | Route |  | 1 | \UART:BUART:tx\_fifo\_empty\ | \UART:BUART:sTX:TxShifter:u0\/f0\_blk\_stat\_comb | \UART:BUART:tx\_status\_0\/main\_3 | 4.673 | | macrocell9 | U(0,2) | 1 | \UART:BUART:tx\_status\_0\ | \UART:BUART:tx\_status\_0\/main\_3 | \UART:BUART:tx\_status\_0\/q | 3.350 | | Route |  | 1 | \UART:BUART:tx\_status\_0\ | \UART:BUART:tx\_status\_0\/q | \UART:BUART:sTX:TxSts\/status\_0 | 2.327 | | statusicell7 | U(0,2) | 1 | \UART:BUART:sTX:TxSts\ |  | SETUP | 0.500 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART:BUART:rx\_state\_2\/q | \UART:BUART:rx\_state\_stop1\_reg\/main\_3 | 74.722 MHz | 13.383 | 1069.950 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell48 | U(1,2) | 1 | \UART:BUART:rx\_state\_2\ | \UART:BUART:rx\_state\_2\/clock\_0 | \UART:BUART:rx\_state\_2\/q | 1.250 | | Route |  | 1 | \UART:BUART:rx\_state\_2\ | \UART:BUART:rx\_state\_2\/q | \UART:BUART:rx\_state\_stop1\_reg\/main\_3 | 8.623 | | macrocell50 | U(1,1) | 1 | \UART:BUART:rx\_state\_stop1\_reg\ |  | SETUP | 3.510 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |

[**+ Hold Subsection**](#gjdgxs)

[**+ Source Clock : Clock\_1 : Positive edge**](#gjdgxs)

[**+ Destination Clock : Clock\_1 : Positive edge**](#gjdgxs)

|  |  |  |  |
| --- | --- | --- | --- |
| Source | Destination | Slack (ns) | Violation |
| \PWM5:PWMUDB:status\_0\/q | \PWM5:PWMUDB:genblk8:stsreg\/status\_0 | 1.557 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell25 | U(3,3) | 1 | \PWM5:PWMUDB:status\_0\ | \PWM5:PWMUDB:status\_0\/clock\_0 | \PWM5:PWMUDB:status\_0\/q | 1.250 | | Route |  | 1 | \PWM5:PWMUDB:status\_0\ | \PWM5:PWMUDB:status\_0\/q | \PWM5:PWMUDB:genblk8:stsreg\/status\_0 | 2.307 | | statusicell3 | U(3,3) | 1 | \PWM5:PWMUDB:genblk8:stsreg\ |  | HOLD | -2.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \PWM3:PWMUDB:status\_0\/q | \PWM3:PWMUDB:genblk8:stsreg\/status\_0 | 1.557 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell29 | U(1,5) | 1 | \PWM3:PWMUDB:status\_0\ | \PWM3:PWMUDB:status\_0\/clock\_0 | \PWM3:PWMUDB:status\_0\/q | 1.250 | | Route |  | 1 | \PWM3:PWMUDB:status\_0\ | \PWM3:PWMUDB:status\_0\/q | \PWM3:PWMUDB:genblk8:stsreg\/status\_0 | 2.307 | | statusicell4 | U(1,5) | 1 | \PWM3:PWMUDB:genblk8:stsreg\ |  | HOLD | -2.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \PWM2:PWMUDB:status\_0\/q | \PWM2:PWMUDB:genblk8:stsreg\/status\_0 | 1.557 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell33 | U(1,3) | 1 | \PWM2:PWMUDB:status\_0\ | \PWM2:PWMUDB:status\_0\/clock\_0 | \PWM2:PWMUDB:status\_0\/q | 1.250 | | Route |  | 1 | \PWM2:PWMUDB:status\_0\ | \PWM2:PWMUDB:status\_0\/q | \PWM2:PWMUDB:genblk8:stsreg\/status\_0 | 2.307 | | statusicell5 | U(1,3) | 1 | \PWM2:PWMUDB:genblk8:stsreg\ |  | HOLD | -2.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \PWM1:PWMUDB:status\_0\/q | \PWM1:PWMUDB:genblk8:stsreg\/status\_0 | 1.573 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell17 | U(0,4) | 1 | \PWM1:PWMUDB:status\_0\ | \PWM1:PWMUDB:status\_0\/clock\_0 | \PWM1:PWMUDB:status\_0\/q | 1.250 | | Route |  | 1 | \PWM1:PWMUDB:status\_0\ | \PWM1:PWMUDB:status\_0\/q | \PWM1:PWMUDB:genblk8:stsreg\/status\_0 | 2.323 | | statusicell1 | U(0,4) | 1 | \PWM1:PWMUDB:genblk8:stsreg\ |  | HOLD | -2.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \PWM6:PWMUDB:status\_0\/q | \PWM6:PWMUDB:genblk8:stsreg\/status\_0 | 1.573 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell21 | U(0,3) | 1 | \PWM6:PWMUDB:status\_0\ | \PWM6:PWMUDB:status\_0\/clock\_0 | \PWM6:PWMUDB:status\_0\/q | 1.250 | | Route |  | 1 | \PWM6:PWMUDB:status\_0\ | \PWM6:PWMUDB:status\_0\/q | \PWM6:PWMUDB:genblk8:stsreg\/status\_0 | 2.323 | | statusicell2 | U(0,3) | 1 | \PWM6:PWMUDB:genblk8:stsreg\ |  | HOLD | -2.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \PWM4:PWMUDB:status\_0\/q | \PWM4:PWMUDB:genblk8:stsreg\/status\_0 | 1.580 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell37 | U(2,4) | 1 | \PWM4:PWMUDB:status\_0\ | \PWM4:PWMUDB:status\_0\/clock\_0 | \PWM4:PWMUDB:status\_0\/q | 1.250 | | Route |  | 1 | \PWM4:PWMUDB:status\_0\ | \PWM4:PWMUDB:status\_0\/q | \PWM4:PWMUDB:genblk8:stsreg\/status\_0 | 2.330 | | statusicell6 | U(2,4) | 1 | \PWM4:PWMUDB:genblk8:stsreg\ |  | HOLD | -2.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \PWM1:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM1:PWMUDB:sP16:pwmdp:u1\/ci | 2.140 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell1 | U(1,4) | 1 | \PWM1:PWMUDB:sP16:pwmdp:u0\ | \PWM1:PWMUDB:sP16:pwmdp:u0\/clock | \PWM1:PWMUDB:sP16:pwmdp:u0\/co\_msb | 2.140 | | Route |  | 1 | \PWM1:PWMUDB:sP16:pwmdp:u0.co\_msb\_\_sig\ | \PWM1:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM1:PWMUDB:sP16:pwmdp:u1\/ci | 0.000 | | datapathcell2 | U(0,4) | 1 | \PWM1:PWMUDB:sP16:pwmdp:u1\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \PWM6:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM6:PWMUDB:sP16:pwmdp:u1\/ci | 2.140 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell3 | U(1,2) | 1 | \PWM6:PWMUDB:sP16:pwmdp:u0\ | \PWM6:PWMUDB:sP16:pwmdp:u0\/clock | \PWM6:PWMUDB:sP16:pwmdp:u0\/co\_msb | 2.140 | | Route |  | 1 | \PWM6:PWMUDB:sP16:pwmdp:u0.co\_msb\_\_sig\ | \PWM6:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM6:PWMUDB:sP16:pwmdp:u1\/ci | 0.000 | | datapathcell4 | U(0,2) | 1 | \PWM6:PWMUDB:sP16:pwmdp:u1\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \PWM5:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM5:PWMUDB:sP16:pwmdp:u1\/ci | 2.140 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell5 | U(2,3) | 1 | \PWM5:PWMUDB:sP16:pwmdp:u0\ | \PWM5:PWMUDB:sP16:pwmdp:u0\/clock | \PWM5:PWMUDB:sP16:pwmdp:u0\/co\_msb | 2.140 | | Route |  | 1 | \PWM5:PWMUDB:sP16:pwmdp:u0.co\_msb\_\_sig\ | \PWM5:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM5:PWMUDB:sP16:pwmdp:u1\/ci | 0.000 | | datapathcell6 | U(3,3) | 1 | \PWM5:PWMUDB:sP16:pwmdp:u1\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \PWM3:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM3:PWMUDB:sP16:pwmdp:u1\/ci | 2.140 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell7 | U(0,5) | 1 | \PWM3:PWMUDB:sP16:pwmdp:u0\ | \PWM3:PWMUDB:sP16:pwmdp:u0\/clock | \PWM3:PWMUDB:sP16:pwmdp:u0\/co\_msb | 2.140 | | Route |  | 1 | \PWM3:PWMUDB:sP16:pwmdp:u0.co\_msb\_\_sig\ | \PWM3:PWMUDB:sP16:pwmdp:u0\/co\_msb | \PWM3:PWMUDB:sP16:pwmdp:u1\/ci | 0.000 | | datapathcell8 | U(1,5) | 1 | \PWM3:PWMUDB:sP16:pwmdp:u1\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |

[**+ Source Clock : CyBUS\_CLK : Positive edge**](#gjdgxs)

[**+ Destination Clock : UART\_IntClock : Positive edge**](#gjdgxs)

|  |  |  |  |
| --- | --- | --- | --- |
| Source | Destination | Slack (ns) | Violation |
| Rx\_1(0)/fb | \UART:BUART:pollcount\_1\/main\_3 | 6.603 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell8 | P12[6] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.009 | | Route |  | 1 | Net\_6168 | Rx\_1(0)/fb | \UART:BUART:pollcount\_1\/main\_3 | 4.594 | | macrocell51 | U(1,0) | 1 | \UART:BUART:pollcount\_1\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| Rx\_1(0)/fb | \UART:BUART:pollcount\_0\/main\_2 | 6.603 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell8 | P12[6] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.009 | | Route |  | 1 | Net\_6168 | Rx\_1(0)/fb | \UART:BUART:pollcount\_0\/main\_2 | 4.594 | | macrocell52 | U(1,0) | 1 | \UART:BUART:pollcount\_0\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| Rx\_1(0)/fb | \UART:BUART:rx\_last\/main\_0 | 6.603 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell8 | P12[6] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.009 | | Route |  | 1 | Net\_6168 | Rx\_1(0)/fb | \UART:BUART:rx\_last\/main\_0 | 4.594 | | macrocell54 | U(1,0) | 1 | \UART:BUART:rx\_last\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| Rx\_1(0)/fb | \UART:BUART:rx\_state\_0\/main\_9 | 7.486 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell8 | P12[6] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.009 | | Route |  | 1 | Net\_6168 | Rx\_1(0)/fb | \UART:BUART:rx\_state\_0\/main\_9 | 5.477 | | macrocell45 | U(1,1) | 1 | \UART:BUART:rx\_state\_0\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| Rx\_1(0)/fb | \UART:BUART:rx\_status\_3\/main\_6 | 7.486 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell8 | P12[6] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.009 | | Route |  | 1 | Net\_6168 | Rx\_1(0)/fb | \UART:BUART:rx\_status\_3\/main\_6 | 5.477 | | macrocell53 | U(1,1) | 1 | \UART:BUART:rx\_status\_3\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| Rx\_1(0)/fb | \UART:BUART:rx\_state\_2\/main\_8 | 8.388 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell8 | P12[6] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.009 | | Route |  | 1 | Net\_6168 | Rx\_1(0)/fb | \UART:BUART:rx\_state\_2\/main\_8 | 6.379 | | macrocell48 | U(1,2) | 1 | \UART:BUART:rx\_state\_2\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| Rx\_1(0)/fb | \UART:BUART:sRX:RxShifter:u0\/route\_si | 12.179 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell8 | P12[6] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.009 | | Route |  | 1 | Net\_6168 | Rx\_1(0)/fb | \UART:BUART:rx\_postpoll\/main\_1 | 4.594 | | macrocell12 | U(1,0) | 1 | \UART:BUART:rx\_postpoll\ | \UART:BUART:rx\_postpoll\/main\_1 | \UART:BUART:rx\_postpoll\/q | 3.350 | | Route |  | 1 | \UART:BUART:rx\_postpoll\ | \UART:BUART:rx\_postpoll\/q | \UART:BUART:sRX:RxShifter:u0\/route\_si | 2.226 | | datapathcell15 | U(1,0) | 1 | \UART:BUART:sRX:RxShifter:u0\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |

[**+ Source Clock : UART\_IntClock : Positive edge**](#gjdgxs)

[**+ Destination Clock : UART\_IntClock : Positive edge**](#gjdgxs)

|  |  |  |  |
| --- | --- | --- | --- |
| Source | Destination | Slack (ns) | Violation |
| \UART:BUART:rx\_status\_3\/q | \UART:BUART:sRX:RxSts\/status\_3 | 2.107 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell53 | U(1,1) | 1 | \UART:BUART:rx\_status\_3\ | \UART:BUART:rx\_status\_3\/clock\_0 | \UART:BUART:rx\_status\_3\/q | 1.250 | | Route |  | 1 | \UART:BUART:rx\_status\_3\ | \UART:BUART:rx\_status\_3\/q | \UART:BUART:sRX:RxSts\/status\_3 | 2.857 | | statusicell8 | U(1,0) | 1 | \UART:BUART:sRX:RxSts\ |  | HOLD | -2.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART:BUART:sTX:sCLOCK:TxBitClkGen\/ce1\_reg | \UART:BUART:txn\/main\_5 | 2.723 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell14 | U(0,0) | 1 | \UART:BUART:sTX:sCLOCK:TxBitClkGen\ | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/clock | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/ce1\_reg | 0.190 | | Route |  | 1 | \UART:BUART:tx\_counter\_dp\ | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/ce1\_reg | \UART:BUART:txn\/main\_5 | 2.533 | | macrocell39 | U(0,0) | 1 | \UART:BUART:txn\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART:BUART:sTX:sCLOCK:TxBitClkGen\/ce1\_reg | \UART:BUART:tx\_state\_2\/main\_4 | 2.731 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell14 | U(0,0) | 1 | \UART:BUART:sTX:sCLOCK:TxBitClkGen\ | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/clock | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/ce1\_reg | 0.190 | | Route |  | 1 | \UART:BUART:tx\_counter\_dp\ | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/ce1\_reg | \UART:BUART:tx\_state\_2\/main\_4 | 2.541 | | macrocell42 | U(0,0) | 1 | \UART:BUART:tx\_state\_2\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART:BUART:sRX:RxBitCounter\/count\_5 | \UART:BUART:rx\_state\_0\/main\_6 | 2.933 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | count7cell | U(1,1) | 1 | \UART:BUART:sRX:RxBitCounter\ | \UART:BUART:sRX:RxBitCounter\/clock | \UART:BUART:sRX:RxBitCounter\/count\_5 | 0.620 | | Route |  | 1 | \UART:BUART:rx\_count\_5\ | \UART:BUART:sRX:RxBitCounter\/count\_5 | \UART:BUART:rx\_state\_0\/main\_6 | 2.313 | | macrocell45 | U(1,1) | 1 | \UART:BUART:rx\_state\_0\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART:BUART:sRX:RxBitCounter\/count\_5 | \UART:BUART:rx\_state\_3\/main\_6 | 2.933 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | count7cell | U(1,1) | 1 | \UART:BUART:sRX:RxBitCounter\ | \UART:BUART:sRX:RxBitCounter\/clock | \UART:BUART:sRX:RxBitCounter\/count\_5 | 0.620 | | Route |  | 1 | \UART:BUART:rx\_count\_5\ | \UART:BUART:sRX:RxBitCounter\/count\_5 | \UART:BUART:rx\_state\_3\/main\_6 | 2.313 | | macrocell47 | U(1,1) | 1 | \UART:BUART:rx\_state\_3\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART:BUART:sRX:RxBitCounter\/count\_0 | \UART:BUART:rx\_bitclk\_enable\/main\_2 | 2.965 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | count7cell | U(1,1) | 1 | \UART:BUART:sRX:RxBitCounter\ | \UART:BUART:sRX:RxBitCounter\/clock | \UART:BUART:sRX:RxBitCounter\/count\_0 | 0.620 | | Route |  | 1 | \UART:BUART:rx\_count\_0\ | \UART:BUART:sRX:RxBitCounter\/count\_0 | \UART:BUART:rx\_bitclk\_enable\/main\_2 | 2.345 | | macrocell49 | U(1,1) | 1 | \UART:BUART:rx\_bitclk\_enable\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART:BUART:sTX:sCLOCK:TxBitClkGen\/ce0\_reg | \UART:BUART:tx\_state\_2\/main\_2 | 3.164 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell14 | U(0,0) | 1 | \UART:BUART:sTX:sCLOCK:TxBitClkGen\ | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/clock | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/ce0\_reg | 0.190 | | Route |  | 1 | \UART:BUART:tx\_bitclk\_enable\_pre\ | \UART:BUART:sTX:sCLOCK:TxBitClkGen\/ce0\_reg | \UART:BUART:tx\_state\_2\/main\_2 | 2.974 | | macrocell42 | U(0,0) | 1 | \UART:BUART:tx\_state\_2\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART:BUART:sRX:RxBitCounter\/count\_2 | \UART:BUART:rx\_bitclk\_enable\/main\_0 | 3.253 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | count7cell | U(1,1) | 1 | \UART:BUART:sRX:RxBitCounter\ | \UART:BUART:sRX:RxBitCounter\/clock | \UART:BUART:sRX:RxBitCounter\/count\_2 | 0.620 | | Route |  | 1 | \UART:BUART:rx\_count\_2\ | \UART:BUART:sRX:RxBitCounter\/count\_2 | \UART:BUART:rx\_bitclk\_enable\/main\_0 | 2.633 | | macrocell49 | U(1,1) | 1 | \UART:BUART:rx\_bitclk\_enable\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART:BUART:sRX:RxBitCounter\/count\_1 | \UART:BUART:rx\_bitclk\_enable\/main\_1 | 3.256 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | count7cell | U(1,1) | 1 | \UART:BUART:sRX:RxBitCounter\ | \UART:BUART:sRX:RxBitCounter\/clock | \UART:BUART:sRX:RxBitCounter\/count\_1 | 0.620 | | Route |  | 1 | \UART:BUART:rx\_count\_1\ | \UART:BUART:sRX:RxBitCounter\/count\_1 | \UART:BUART:rx\_bitclk\_enable\/main\_1 | 2.636 | | macrocell49 | U(1,1) | 1 | \UART:BUART:rx\_bitclk\_enable\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART:BUART:sRX:RxBitCounter\/count\_6 | \UART:BUART:rx\_state\_0\/main\_5 | 3.258 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | count7cell | U(1,1) | 1 | \UART:BUART:sRX:RxBitCounter\ | \UART:BUART:sRX:RxBitCounter\/clock | \UART:BUART:sRX:RxBitCounter\/count\_6 | 0.620 | | Route |  | 1 | \UART:BUART:rx\_count\_6\ | \UART:BUART:sRX:RxBitCounter\/count\_6 | \UART:BUART:rx\_state\_0\/main\_5 | 2.638 | | macrocell45 | U(1,1) | 1 | \UART:BUART:rx\_state\_0\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |

[**+ Clock To Output Section**](#gjdgxs)

[**+ Clock\_1**](#gjdgxs)

|  |  |  |
| --- | --- | --- |
| Source | Destination | Delay (ns) |
| Net\_1932/q | servo5(0)\_PAD | 24.351 |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell26 | U(2,3) | 1 | Net\_1932 | Net\_1932/clock\_0 | Net\_1932/q | 1.250 | | Route |  | 1 | Net\_1932 | Net\_1932/q | servo5(0)/pin\_input | 7.176 | | iocell4 | P15[5] | 1 | servo5(0) | servo5(0)/pin\_input | servo5(0)/pad\_out | 15.925 | | Route |  | 1 | servo5(0)\_PAD | servo5(0)/pad\_out | servo5(0)\_PAD | 0.000 | | Clock |  |  |  |  | Clock path delay | 0.000 | | | |
| Net\_1879/q | servo4(0)\_PAD | 24.271 |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell38 | U(2,4) | 1 | Net\_1879 | Net\_1879/clock\_0 | Net\_1879/q | 1.250 | | Route |  | 1 | Net\_1879 | Net\_1879/q | servo4(0)/pin\_input | 7.234 | | iocell7 | P2[2] | 1 | servo4(0) | servo4(0)/pin\_input | servo4(0)/pad\_out | 15.787 | | Route |  | 1 | servo4(0)\_PAD | servo4(0)/pad\_out | servo4(0)\_PAD | 0.000 | | Clock |  |  |  |  | Clock path delay | 0.000 | | | |
| Net\_1733/q | servo2(0)\_PAD | 23.424 |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell34 | U(0,3) | 1 | Net\_1733 | Net\_1733/clock\_0 | Net\_1733/q | 1.250 | | Route |  | 1 | Net\_1733 | Net\_1733/q | servo2(0)/pin\_input | 6.326 | | iocell6 | P15[4] | 1 | servo2(0) | servo2(0)/pin\_input | servo2(0)/pad\_out | 15.848 | | Route |  | 1 | servo2(0)\_PAD | servo2(0)/pad\_out | servo2(0)\_PAD | 0.000 | | Clock |  |  |  |  | Clock path delay | 0.000 | | | |
| Net\_78/q | servo1(0)\_PAD | 23.288 |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell18 | U(0,4) | 1 | Net\_78 | Net\_78/clock\_0 | Net\_78/q | 1.250 | | Route |  | 1 | Net\_78 | Net\_78/q | servo1(0)/pin\_input | 6.371 | | iocell1 | P2[0] | 1 | servo1(0) | servo1(0)/pin\_input | servo1(0)/pad\_out | 15.667 | | Route |  | 1 | servo1(0)\_PAD | servo1(0)/pad\_out | servo1(0)\_PAD | 0.000 | | Clock |  |  |  |  | Clock path delay | 0.000 | | | |
| Net\_7176/q | servo6(0)\_PAD | 23.124 |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell22 | U(0,2) | 1 | Net\_7176 | Net\_7176/clock\_0 | Net\_7176/q | 1.250 | | Route |  | 1 | Net\_7176 | Net\_7176/q | servo6(0)/pin\_input | 6.493 | | iocell10 | P1[7] | 1 | servo6(0) | servo6(0)/pin\_input | servo6(0)/pad\_out | 15.381 | | Route |  | 1 | servo6(0)\_PAD | servo6(0)/pad\_out | servo6(0)\_PAD | 0.000 | | Clock |  |  |  |  | Clock path delay | 0.000 | | | |
| Net\_1760/q | servo3(0)\_PAD | 22.874 |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell30 | U(0,5) | 1 | Net\_1760 | Net\_1760/clock\_0 | Net\_1760/q | 1.250 | | Route |  | 1 | Net\_1760 | Net\_1760/q | servo3(0)/pin\_input | 5.733 | | iocell5 | P2[1] | 1 | servo3(0) | servo3(0)/pin\_input | servo3(0)/pad\_out | 15.891 | | Route |  | 1 | servo3(0)\_PAD | servo3(0)/pad\_out | servo3(0)\_PAD | 0.000 | | Clock |  |  |  |  | Clock path delay | 0.000 | | | |

[**+ UART\_IntClock**](#gjdgxs)

|  |  |  |
| --- | --- | --- |
| Source | Destination | Delay (ns) |
| \UART:BUART:txn\/q | Tx\_1(0)\_PAD | 30.513 |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell39 | U(0,0) | 1 | \UART:BUART:txn\ | \UART:BUART:txn\/clock\_0 | \UART:BUART:txn\/q | 1.250 | | Route |  | 1 | \UART:BUART:txn\ | \UART:BUART:txn\/q | Net\_6163/main\_0 | 2.690 | | macrocell7 | U(0,0) | 1 | Net\_6163 | Net\_6163/main\_0 | Net\_6163/q | 3.350 | | Route |  | 1 | Net\_6163 | Net\_6163/q | Tx\_1(0)/pin\_input | 6.256 | | iocell9 | P12[7] | 1 | Tx\_1(0) | Tx\_1(0)/pin\_input | Tx\_1(0)/pad\_out | 16.967 | | Route |  | 1 | Tx\_1(0)\_PAD | Tx\_1(0)/pad\_out | Tx\_1(0)\_PAD | 0.000 | | Clock |  |  |  |  | Clock path delay | 0.000 | | | |