JORDAN TAPIA

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SUMMARY

As a hardware engineer, I have nearly three years of experience working within a multidisciplinary team to develop LAN ethernet switches from design to production.

HARDWARE

- Responsible for hardware development of LAN ethernet switches for enterprise.
- Experience identifying electrical test coverage areas, effectively engaging team members for review, and executing these plans to meet required deadlines.
- Practiced in board bringup and hardware verification of networking systems.
- Heavy usage of high speed oscilloscopes, spectrum analyzers, function generators, frequency counters, signal source analyzer, logic analyzers, soldering, TDR modules
- Familiar with SI modeling (LT Spice, Hyperlynx, IBIS models), transmission line concepts
- Debugging and characterizing I2C, SPI, eMMC, MDIO, DDR4, JTAG
- Allegro PCB Editor for high speed digital design, Cadence Schematic Capture, BOM Integrity, Agile project management

SOFTWARE

- Interest in embedded design with C and ARM-based MCUs
- Usage of Eclipse IDEs, GNU toolchain, Make, CMSIS header files
- Git, JIRA used for version control of HW design files and issue tracking
- Python familiarity for low level hardware testing
- Verilog and Quartus familiarity for FPGA verification on Intel Cyclone V, Max10

EXPERIENCE

Hardware Design Engineer: ***Aruba, a HPE Company,*** June 2018 - Present

- Responsible for schematic entry, layout/routing, and BOM integrity of 12 port 100GBE switch for enterprise.
- Lead test development/execution for assigned coverages areas.
- Used expertise in Cadence and Allegro to efficiently leverage common areas of the design from a previously proven design SKU.
- Assisted with power module design, layout of DC-DC converters.
- Contributed to developing board-level test plans for assessing signal integrity and reliability of critical components.
- Experience guiding layout houses for additions/modifications of high speed networking serdes, management interfaces, and power planes.
- Lead designer for ancillary boards: hot swap controller, U2U, and LED modules.

EDUCATION

B.S. Electrical Engineering, ***University of California at Santa Cruz,*** Sept. 2015 – June 2018

- Senior Design Project sponsored by Kateeva®: successfully developed PID controller for y-axis control of pneumatic piston.
- Coursework in RF Design, High Speed Digital Design, and Verilog