Lab 1 Fall 2021

Goal: To create a logic design implementing a counter and a register.

Materials: DE10-Lite board

Due: Lab 1 is due by midnight on the day of lab in week 2.

Basic Assignment (90%)

Create a counter that will count up from 0 to C, then repeat. Display the count value on the 7-segment display HEX0. Use a GENERIC to build in flexibility – add a parameter, M, which will specify the number of seconds between each increment of the counter.

Create a register to hold a 4-bit value. Load the current count value of the counter into the register when KEY(1) is pressed. The value in the register should be continuously displayed on the LEDs, LEDR(3:0).

Create VHDL designs for the counter (with the GENERIC) and for a hex-to-7-segment converter, and use them as components in your high level design, where you will specify the value to use for the GENERIC parameter.

Advanced Assignment (100%)

Add a new feature to allow selection of the count direction. If SW(0) is ‘0’, count down, if it is ‘1’, count up, and repeat in both cases.

Add another GENERIC parameter, N, to specify the maximum count value (in the range 1 to 255). Note: with the expanded count range, you will need to expand your displays. Use HEX0 and HEX1, as well as LEDR(7:0).

Report

Follow standard report format. Required attachments are your commented VHDL code, for the top level design, and the components.