TÉCNICO LISBOA

T4 - Audio Amplifier

Integrated Master in Physics Engineering

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1 Introduction

In this laboratory assignment we seek to build an audio amplifier circuit , with the goal of maximizing the merit figure, M, given by:

$$M = \frac{voltageGain * bandwidth}{cost * lowerCutoffFreq}$$

being that the voltage gain is given by the quotient between the output voltage and the input voltage; the bandwidth is the magnitude of the interval of frequencies for which the circuit functions; and the lower cut off frequency is given by the lowest frequency for which the circuit functions. The cost equals the sum of the cost of each individual component.

The circuit consists only of resistors, voltage sources (AC as well as DC), capacitors and bipolar junction transistors (more specifically one PNP transistor and one NPN transistor)

The circuit used was the following:

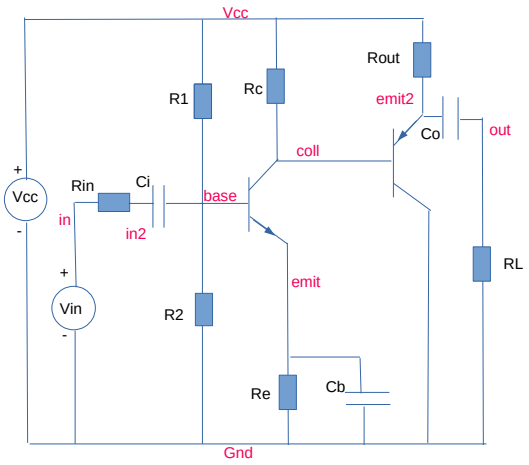

Figure 1: Circuito utilizado

In Section 2, a theoretical analysis is presented. In Section 3, the circuit is analysed by simulation, and the results are compared to the theoretical results obtained in Section 2. The conclusions of this study are outlined in Section 4.

2 Theoretical Analysis

2.1 First part

The theoretical analysis is split into three parts. In the first part we compute the operating point using the Ebers-Moll model for the transistor. Taking into account the fact that capacitors act as an open circuit on the operating point, and using Thevenin's theorem to simplify the circuit, we get the following equations:

$$R_{th} = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}}$$

$$V_{th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$I_{B1} = \frac{V_{th} - V_{BEON}}{R_{th} + (1 + \beta_{FN}) R_e}$$

$$I_{C1} = \beta_{FN} I_{B1}$$

$$I_{E1} = (1 + \beta_{FN}) I_{B1}$$

$$V_{E1} = R_e * I_{E1}$$

$$V_{O1} = V_{CC} - R_1 I_{C1}$$

$$V_{CE} = V_{O1} - V_{E1}$$

being that I_{B1} is the current going **into** the base of the first transitor; I_{E1} is the current going **out** of the emitter of the first transistor; V_{O1} is the voltage at the 'coll' node; $V_C E$ is the potential difference between the collector and emitter of the first transistor.

Using the following values:

RE1	100.000000
RC1	73.000000
RB1	72400.000000
RB2	14400.000000
VCC	12.000000
RS	100.000000

Table 1: Values used as parameters for the circuit studied.

We get:

IB1	0.000008
IC1	0.001370
IE1	0.001378
VE1	1.198692
VO1	11.899980
VCE	10.701288
gm1	0.054806
rpi1	3260.617904
ro1	50870.748278
ZI1	2564.451494
ZO1	72.895394
AV1	3.845133
VI2	11.899980
IE2	-0.006000
IC2	-0.005974
VO2	12.599980
gm2	-0.238941
go2	-0.000161
gpi2	-0.001051
ge2	0.010000
AV2	1.038184
ZI2	24912.920045
ZO2	-4.344945
a	0.962469
b	0.997083
c	2.188749

Table 2: Operating point theoretically

2.2 Second part

In this part we compute the gain, input and output impedances separately for the 2 stages. The model used for the transistors here is the same.

$$g_{m1} = I_{C1}/V_T$$

$$r_{pi1} = \beta FN/g_{m1}$$

$$r_{o1} = V_{AFN}/I_{C1}$$

Using this, we can calculate the voltage gain

$$A_{V1} = \frac{g_{m1} Z_{O1} Z_{I1}}{Z_{I1} + R_S}$$

$$R_{E1} = 100$$

For calculating the entrance impendance of transistor 1, we've come to the following equations

$$Z_{I1} = r_{pi}||R_2||R_1$$

$$Z_{I1} = \frac{R_{B1}R_{B2}r_{pi1}}{R_{B1}R_{B2} + R_{B1}r_{pi1} + R_{B2}r_{pi1}}$$

For calculating the exit impedance

$$Z_{O1} = r_{01}||R_{C1}$$

Repeating the same calculations, but for transistor 2, we get that

$$g_{m2} = I_{C2}/V_T$$

$$g_{o2} = I_{C2}/V_{AFP}$$

$$g_{pi2} = g_{m2}/\beta_{FP}$$

$$g_{e2} = 1/R_{E2}$$

For calculating the entrance impendance of transistor 2, we've come to the following equation

$$A_{V2} = \frac{g_{m2}}{g_{m2} + g_{pi2} + g_{o2} + g_{e2}}$$

for calculating the exit impendance of transistor 2, we get

$$Z_{O2} = 1/(g_{m2} + g_{pi2} + g_{o2} + g_{e2})$$

The following ratio should be equal to one. if that's the case, then we've confirmed there's a small loss of signal between the transistors

$$b = ZI2/(ZI2 + ZO1)$$

Similarly, the following ratio should be one if there's a small loss of signal between Vin and the first transistor

$$a = Z_{I1}/(Z_{I1} + R_S)$$

Finally, to ensure that there's no signal loss between the speaker and the second transistor, the following ratio should be approximately one

$$c = R_L/(R_L + Z_{O2})$$

3 Simulation Analysis

The Operating point analysis is the following:

Name	Value
base	1.365942e+00
coll	4.821057e+00
emit	6.570592e-01
emit2	5.649825e+00
in	0.000000e+00
in2	0.000000e+00
out	0.000000e+00
vcc	1.200000e+01

Table 3: Operating point.

The impedances measured are the following:

Name	Value
zi	-5.63461e-01
z0	-4.79476e+01

Table 4: Impedances

The graphs are the following:

Time analysis:

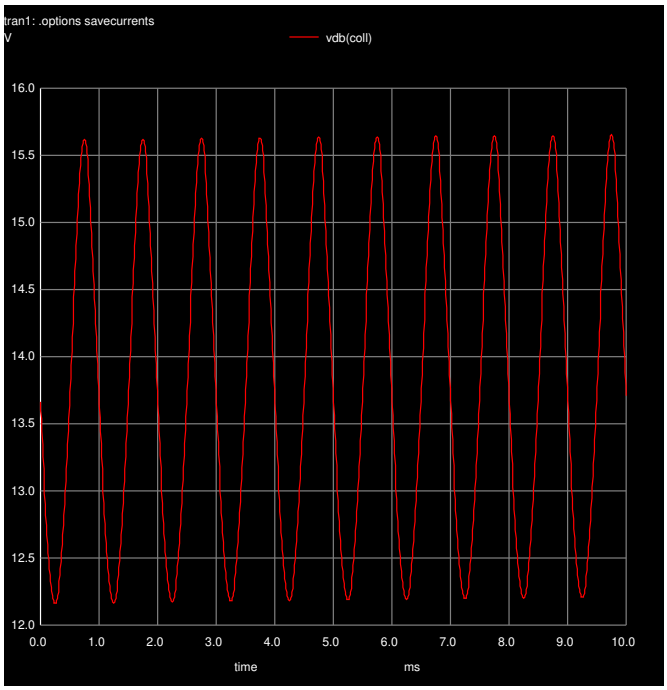

Figure 2: Time analysis

Frequency analysis:

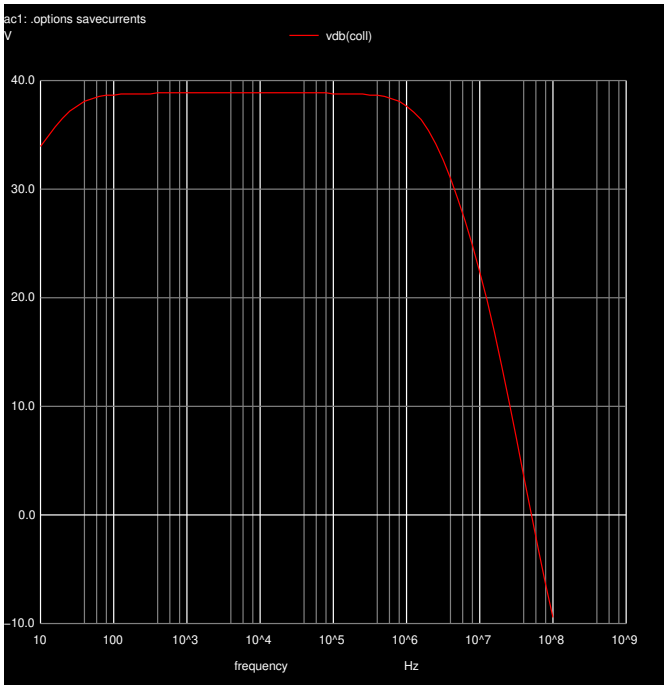

Figure 3: Frequency analysis

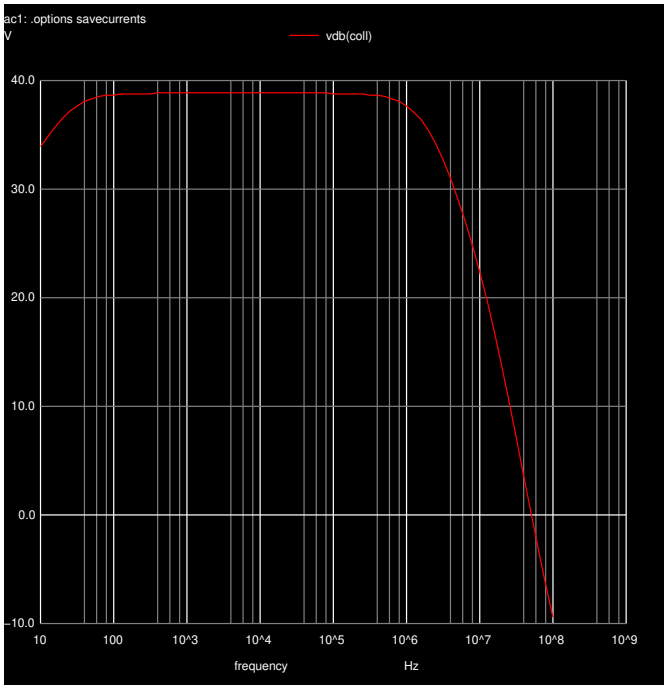

Figure 4: Frequency analysis

4 Conclusion

As we can see in the operating point analysis there are some differences between the theoretical values and simulation values. This is due to the aproximations used in the theoretical analysis, ngspice uses a much more sofisticated model.