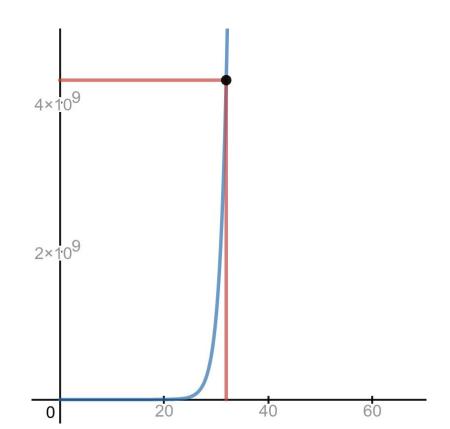
Paginación nivel 5

Sanabria Betancourt Erik

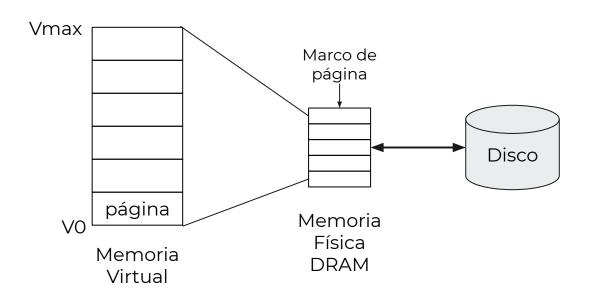
Arquitectura x86_64

Direccionamiento de:

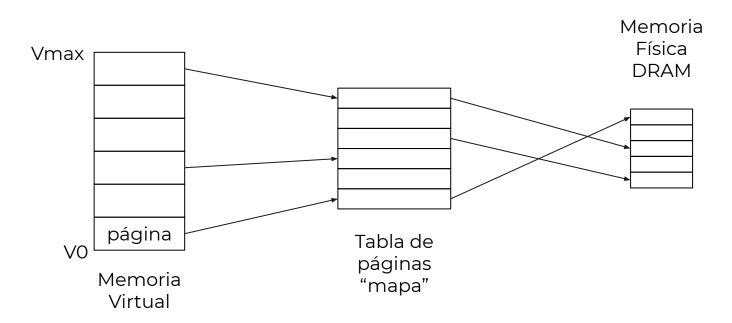
- 16 bits → 64 KB
- 32 bits \rightarrow 4 GB
- 64 bits → 16M TB = 16 EB
- 39 bits → 512 GB
- 46 bits → 64 TB
- 48 bits → 256 TB



Memoria Virtual



Paginación



Página

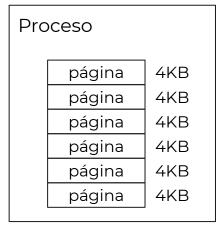
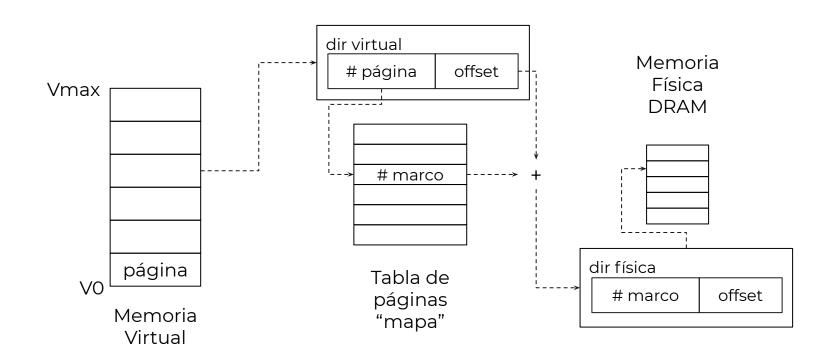
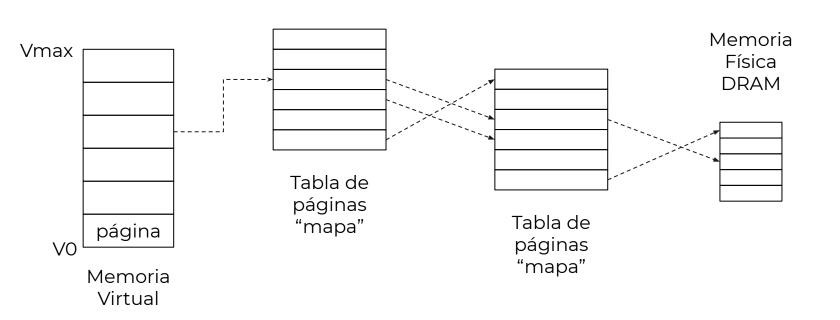


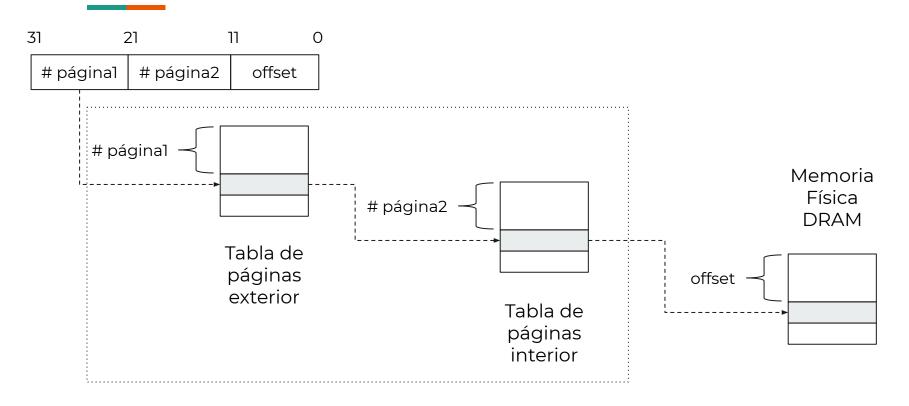
Tabla de Páginas



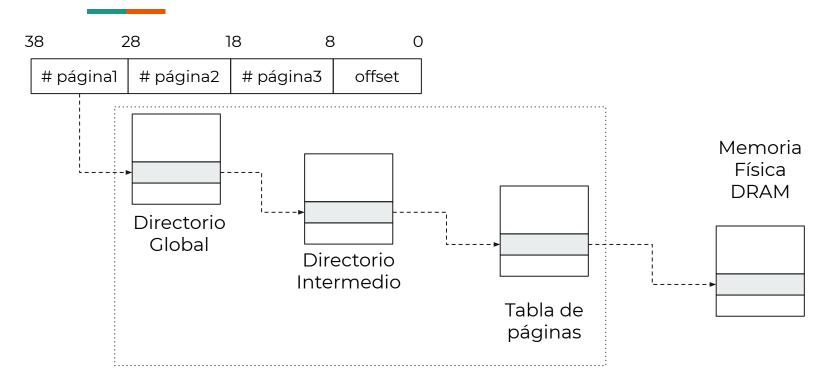
Paginación de múltiples niveles



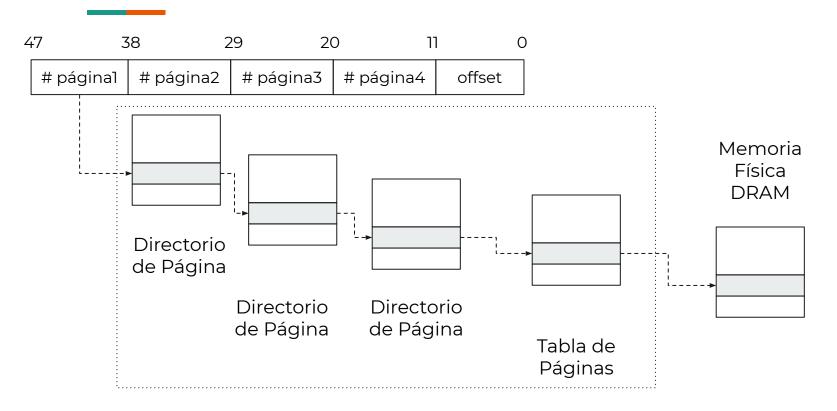
Paginación en el Pentium de 32-bits



X86_64 con 39-bits



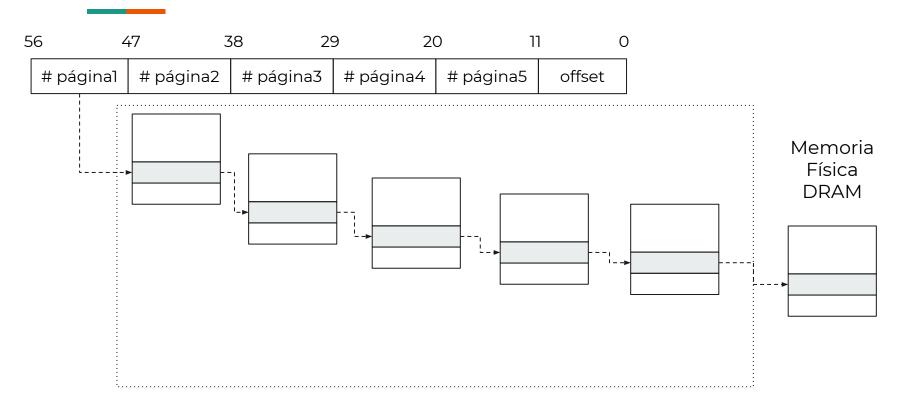
X86_64 con 48-bits



Paginación nivel 5

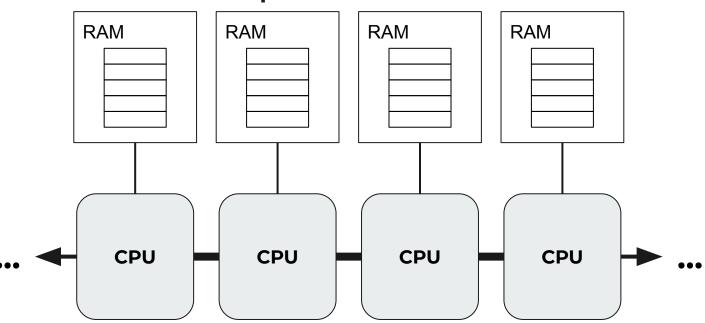
- Memoria física: 46-bits \rightarrow 52-bits, 64 TB \rightarrow 4 PB
- Memoria virtual: 48-bits \rightarrow 57-bits, 256 TB \rightarrow 128 PB
- Compilar con: CONFIG_X86_5LEVEL=y

X86_64 con 57-bits



¿Cómo se Logra?

NUMA —> Scale-Up



¿Para Qué Tanta Memoria?

- In-Memory Computing
- Bases de Datos
- Business Intelligence
- OLTP
- OLAP
- Virtualización





Referencias

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