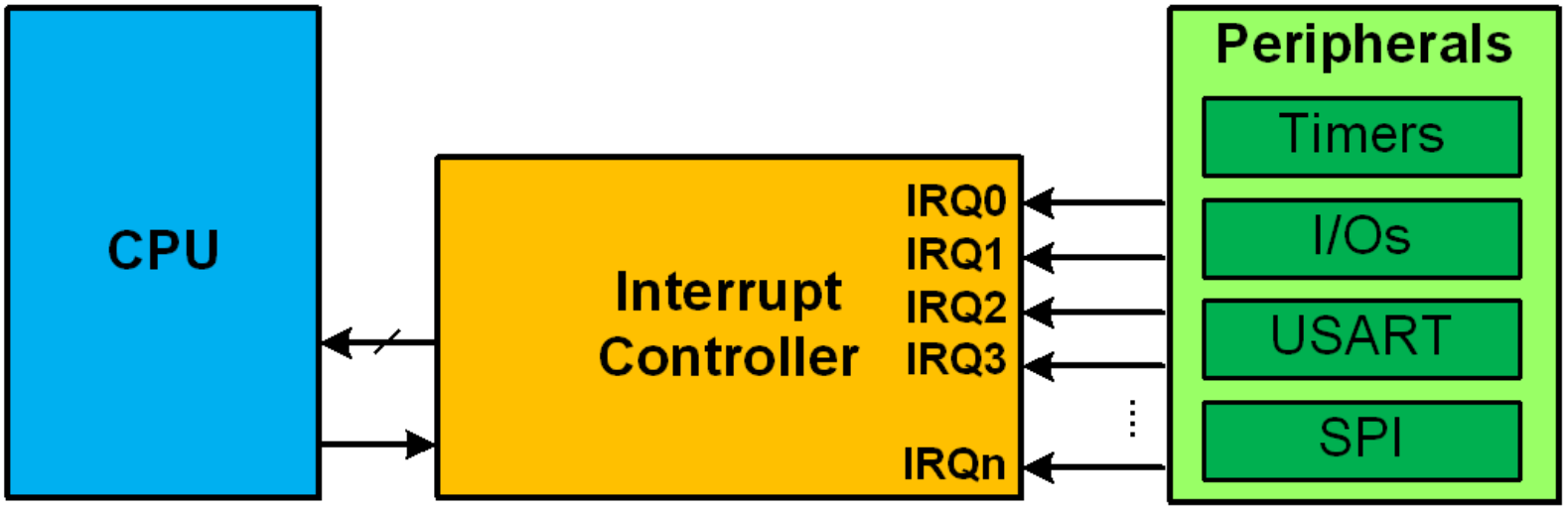
Interrupts

Interrupts vs polling

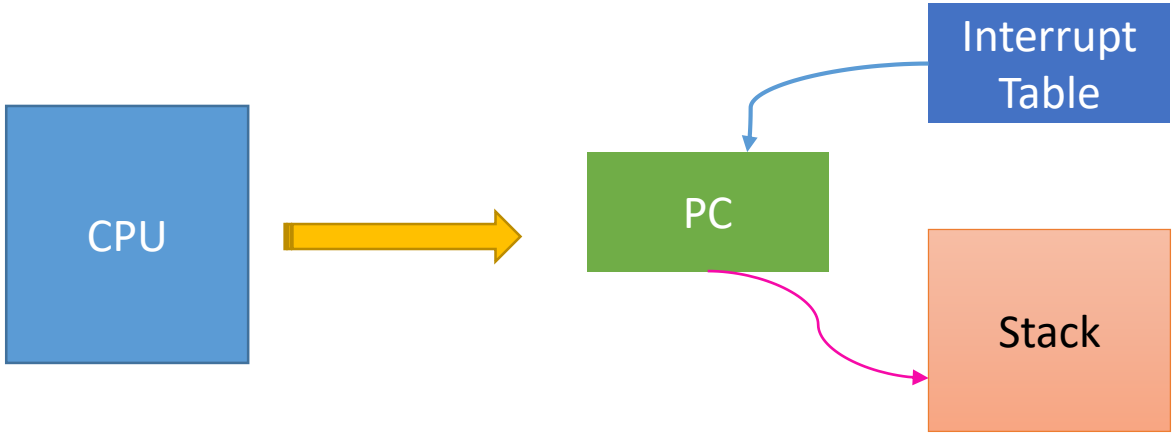
- MCU serves to several devices:
  - Polling → MCU monitors the status of every device, when a condition is met it performs a service
  - Interrupts → the device notifies to MCU sending a request, then MCU stops and serves to the device.

- MCU wastes time by polling device when they do not need service.

Interrupts



Source: "The AVR microcontroller and embedded system". M.Ali Mazidi, S.Naimi



Interrupts

- Interrupts → stop the main program to perform **I**nterrupt **S**ervice **R**outine
- Each interrupt have a program vector in the memory

Interrupt vector table

Priority

VectorNo.	Program Address(2)	Source	Interrupt Definition
1	0x0000(1)	RESET	External Pin, Power-on Reset, Brown-out Reset and Watchdog System Reset
2	0x0002	INT0	External Interrupt Request 0
3	0x0004	INT1	External Interrupt Request 1
4	0x0006	PCINT0	Pin Change Interrupt Request 0
5	0x0008	PCINT1	Pin Change Interrupt Request 1
6	0x000A	PCINT2	Pin Change Interrupt Request 2
7	0x000C	WDT	Watchdog Time-out Interrupt
8	0x000E	TIMER2 COMPA	Timer/Counter2 Compare Match A
9	0x0010	TIMER2 COMPB	Timer/Counter2 Compare Match B
10	0x0012	TIMER2 OVF	Timer/Counter2 Overflow
11	0x0014	TIMER1 CAPT	Timer/Counter1 Capture Event
12	0x0016	TIMER1 COMPA	Timer/Counter1 Compare Match A
13	0x0018	TIMER1 COMPB	Timer/Coutner1 Compare Match B
14	0x001A	TIMER1 OVF	Timer/Counter1 Overflow
15	0x001C	TIMER0 COMPA	Timer/Counter0 Compare Match A
16	0x001E	TIMER0 COMPB	Timer/Counter0 Compare Match B
17	0x0020	TIMER0 OVF	Timer/Counter0 Overflow
18	0x0022	SPI, STC	SPI Serial Transfer Complete
19	0x0024	USART, RX	USART Rx Complete
20	0x0026	USART, UDRE	USART, Data Register Empty
21	0x0028	USART, TX	USART, Tx Complete
22	0x002A	ADC	ADC Conversion Complete
23	0x002C	EE READY	EEPROM Ready
24	0x002E	ANALOG COMP	Analog Comparator
25	0x0030	TWI	2-wire Serial Interface
26	0x0032	SPM READY	Store Program Memory Ready

Only a JMP instruction

Interrupts

ATmega328P

Vector Number	Interrupt definition	Vector name
2	External Interrupt Request 0	INT0_vect
3	External Interrupt Request 1	INT1_vect
4	Pin Change Interrupt Request 0	PCINT0_vect
5	Pin Change Interrupt Request 1	PCINT1_vect
6	Pin Change Interrupt Request 2	PCINT2_vect
7	Watchdog Time-out Interrupt	WDT_vect
8	Timer/Counter2 Compare Match A	TIMER2_COMPA_vect
9	Timer/Counter2 Compare Match B	TIMER2_COMPB_vect
10	Timer/Counter2 Overflow	TIMER2_OVF_vect
11	Timer/Counter1 Capture Event	TIMER1_CAPT_vect
12	Timer/Counter1 Compare Match A	TIMER1_COMPA_vect
13	Timer/Counter1 Compare Match B	TIMER1_COMPB_vect
14	Timer/Counter1 Overflow	TIMER1_OVF_vect
15	Timer/Counter0 Compare Match A	TIMER0_COMPA_vect
16	Timer/Counter0 Compare Match B	TIMER0_COMPB_vect
17	Timer/Counter0 Overflow	TIMER0_OVF_vect
18	SPI Serial Transfer Complete	SPI_STC_vect
19	USART Rx Complete	USART_RX_vect
20	USART Data Register Empty	USART_UDRE_vect
21	USART Tx Complete	USART_TX_vect
22	ADC Conversion Complete	ADC_vect
23	EEPROM Ready	EE_READY_vect
24	Analog Comparator	ANALOG_COMP_vect
25	Two-wire Serial Interface	TWI_vect
26	Store Program Memory Read	SPM_READY_vect

Interrupts

Interrupt Process

PC: 0000

Little Endian (Low byte first, then high byte) is used here, following the AVR simulator.

```
                .INCLUDE "M32DEF.INC"
                .ORG 0
0000            JMP     MAIN
                .ORG 0x02
0002            JMP     EXO_ISR
0004    MAIN:   LDI     R20,HIGH(RAMEND)
0005            OUT     SPH,R20
0006            LDI     R20,LOW(RAMEND)
0007            OUT     SPL,R20
0008            SBI     DDRC,3
0009            SBI     PORTD,2
000A            LDI     R20,1<<INT0
000B            OUT     GICR,R20
000C            SEI
000D            LDI     R30,3
000E            LDI     R31,4
000F            ADD     R30,R31
0010    HERE:   JMP     HERE
0012 EX0_ISR:   IN      R21,PORTC
0013            LDI     R22,0X08
0014            EOR     R21,R22
0015            OUT     PORTC,R21
0016            RETI
```

Source: Lecturer Shaidatul Sadiah, University of Malasya
https://www.youtube.com/watch?v=zViw6mMzEoA&list=PLbnXeqW-iDlnWDkh5uNtHVDV4SqlnxRP9&index=17

Interrupts

- An enable bit for each interrupt → '1'
- Global Interrupt Enable bit in the Status Register → '1'
- Priority levels → the lower the address the higher the priority
- When an interrupt occurs:
  - All interrupts are disabled.
  - Program Counter and GPRs to the stack.
  - Program Counter = Interrupt vector to directs to the ISR
  - When ISR is completed → returns to the main program
- Interrupt sources:
  - External
  - Internals Peripherals:
    - Timers
    - USART
    - SPI
    - Etc.

It takes 4 clk cycles

ATMega 328: External Interrupts (INT)

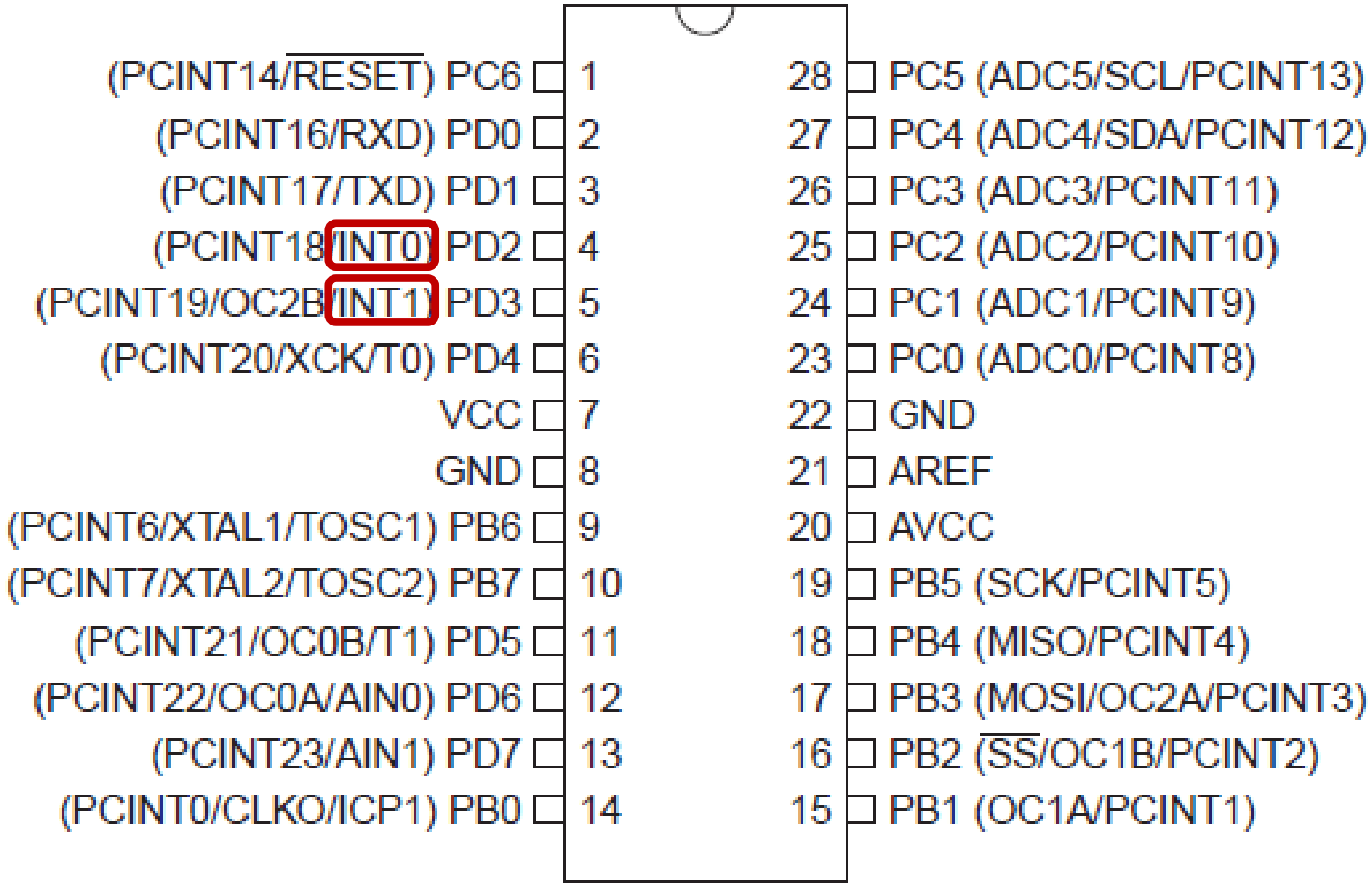
Interrupts: External Interrupts

- Two types:
  - External INT0 and INT1 pins (PD2 and PD3)
    - Triggered by a falling or rising edge or a low level.
  - Pin change (PCINT0-PCINT23) → whatever pin
    - PCINT2 → PCINT[23:16] pin toggles.
    - PCINT1 → PCINT[14:8] pin toggles
    - PCINT0 → PCINT[7:0] pin toggles

VectorNo.	Program Address(2)	Source	Interrupt Definition
2	0x0002	INT0	External Interrupt Request 0
3	0x0004	INT1	External Interrupt Request 1
4	0x0006	PCINT0	Pin Change Interrupt Request 0
5	0x0008	PCINT1	Pin Change Interrupt Request 1
6	0x000A	PCINT2	Pin Change Interrupt Request 2

- Synchronously (a clk is required, event) or asynchronously (level triggered).
- Asynchronously (Pin change) → waking the device from sleep modes

Interrupts: External Interrupts



ATMEGA328p – 28PDIP

Source: Microchip

Interrupts: External Interrupts

➢ Registers

SREG – AVR Status Register

The AVR Status Register – SREG – is defined as:

Bit	7	6	5	4	3	2	1	0	
0x3F (0x5F)	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – I: Global Interrupt Enable**

The Global Interrupt Enable bit must be set for the interrupts to be enabled. The individual interrupt enable control is then performed in separate control registers. If the Global Interrupt Enable Register is cleared, none of the interrupts are enabled independent of the individual interrupt enable settings. The I-bit is cleared by hardware after an interrupt has occurred, and is set by the RETI instruction to enable subsequent interrupts. The I-bit can also be set and cleared by the application with the SEI and CLI instructions, as described in the instruction set reference.

‘1’ → Enable
‘0’ → Disable

Interrupts: External Interrupts

➢ Registers

EICRA – External Interrupt Control Register A

The External Interrupt Control Register A contains control bits for interrupt sense control.

Bit	7	6	5	4	3	2	1	0	
(0x69)	–	–	–	–	ISC11	ISC10	ISC01	ISC00	EICRA
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

INT1

ISC11	ISC10	Description
0	0	The low level of INT1 generates an interrupt request.
0	1	Any logical change on INT1 generates an interrupt request.
1	0	The falling edge of INT1 generates an interrupt request.
1	1	The rising edge of INT1 generates an interrupt request.

INT0

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Any logical change on INT0 generates an interrupt request.
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

Interrupts: External Interrupts

- Registers to setup INT0 and INT1

EIMSK – External Interrupt Mask Register

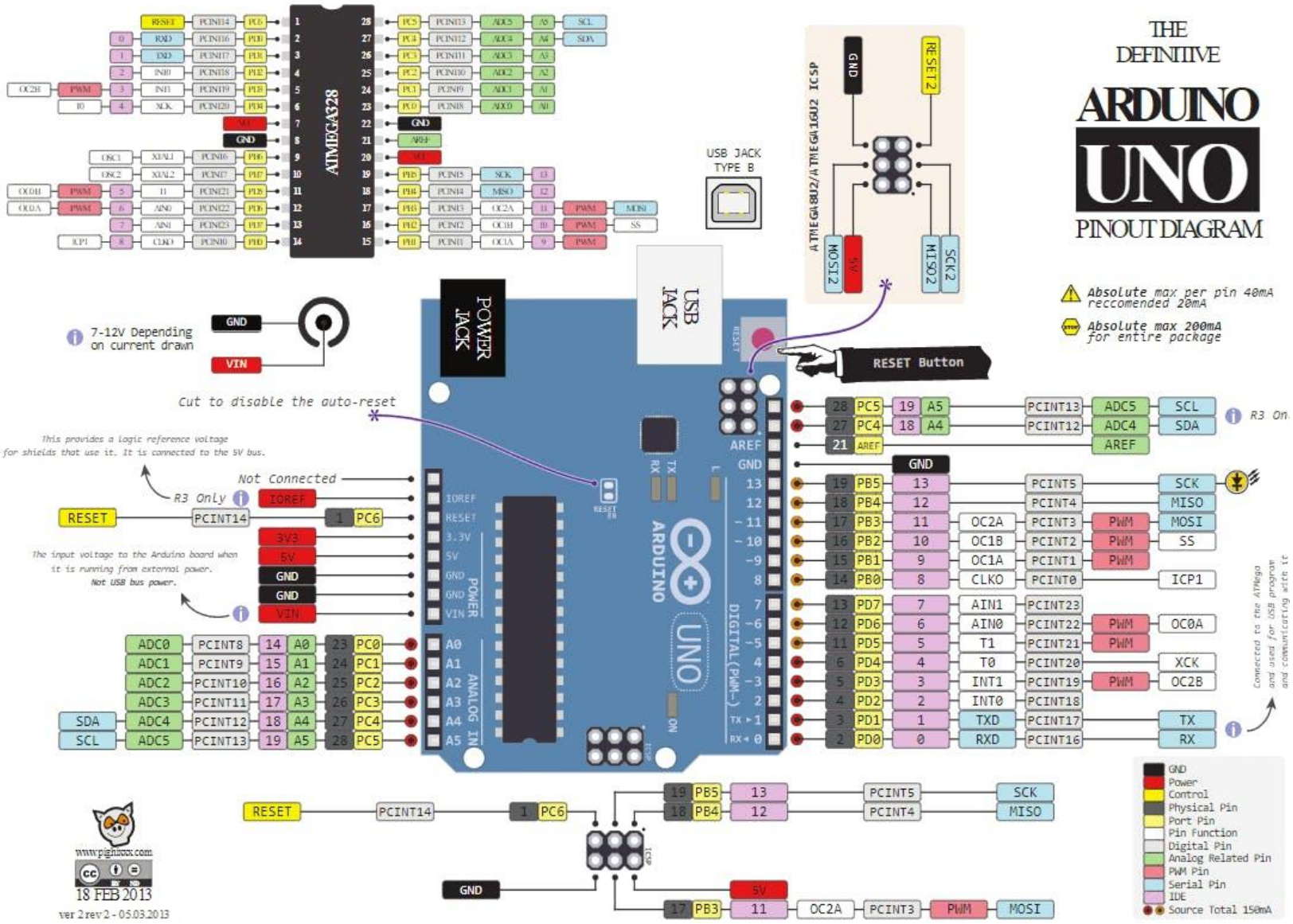
Bit	7	6	5	4	3	2	1	0	
0x1D (0x3D)	–	–	–	–	–	–	INT1	INT0	EIMSK
Read/Write	R	R	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

'1' → Enable
'0' → Disable

EIFR – External Interrupt Flag Register

Bit	7	6	5	4	3	2	1	0	
0x1C (0x3C)	–	–	–	–	–	–	INTF1	INTF0	EIFR
Read/Write	R	R	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

ATMega 328: External Interrupts (PCINT)


THE DEFINITIVE
ARDUINO
UNO
PINOUT DIAGRAM
ATMEGA328
ATMEGA8U2/ATMEGA16U2 ICSP
USB JACK TYPE B
POWER JACK
USB JACK
RESET Button
7-12V Depending on current drawn
GND
VIN
Cut to disable the auto-reset
This provides a logic reference voltage for shields that use it. It is connected to the 5V bus.
Not Connected
R3 Only
IOREF
RESET
PCINT14
1 PC6
3V3
5V
GND
GND
VIN
The input voltage to the Arduino board when it is running from external power.
Not USB bus power.
ADC0 PCINT8 14 A0 23 PC0
ADC1 PCINT9 15 A1 24 PC1
ADC2 PCINT10 16 A2 25 PC2
ADC3 PCINT11 17 A3 26 PC3
SDA ADC4 PCINT12 18 A4 27 PC4
SCL ADC5 PCINT13 19 A5 28 PC5
AREF
GND
13 PB5 PCINT5 SCK
12 PB4 PCINT4 MISO
~11 PB3 OC2A PCINT3 PWM MOSI
10 PB2 OC1B PCINT2 PWM SS
~9 PB1 OC1A PCINT1 PWM
8 PB0 CLKO PCINT0 ICP1
7 PD7 AIN1 PCINT23
~6 PD6 AIN0 PCINT22 PWM OC0A
~5 PD5 T1 PCINT21 PWM
4 PD4 T0 PCINT20 XCK
~3 PD3 INT1 PCINT19 PWM OC2B
2 PD2 INT0 PCINT18
TX →1 PD1 TXD PCINT17 TX
RX ←0 PD0 RXD PCINT16 RX
Absolute max per pin 40mA reccomended 20mA
Absolute max 200mA for entire package
Connected to the ATMega and used for USB program and communication with it
GND
Power
Control
Physical Pin
Port Pin
Pin Function
Digital Pin
Analog Related Pin
PWM Pin
Serial Pin
IDE
Source Total 150mA
www.pighixx.com
18 FEB 2013
ver 2 rev 2 - 05.03.2013

Interrupts: External Interrupts

- Registers to setup PCINT

PCICR – Pin Change Interrupt Control Register

Bit	7	6	5	4	3	2	1	0	
(0x68)	–	–	–	–	–	PCIE2	PCIE1	PCIE0	PCICR
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

'1' → Enable
'0' → Disable

PCIFR – Pin Change Interrupt Flag Register

Bit	7	6	5	4	3	2	1	0	
0x1B (0x3B)	–	–	–	–	–	PCIF2	PCIF1	PCIF0	PCIFR
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Interrupts: External Interrupts

- Registers to setup PCINT

'1' → Enable
'0' → Disable

PCMSK2 – Pin Change Mask Register 2

Bit	7	6	5	4	3	2	1	0	
(0x6D)	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	PCMSK2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7:0 – PCINT[23:16]: Pin Change Enable Mask 23...16**

Each PCINT[23:16]-bit selects whether pin change interrupt is enabled on the corresponding I/O pin. If PCINT[23:16] is set and the PCIE2 bit in PCICR is set, pin change interrupt is enabled on the corresponding I/O pin. If PCINT[23:16] is cleared, pin change interrupt on the corresponding I/O pin is disabled.

PCMSK1 – Pin Change Mask Register 1

Bit	7	6	5	4	3	2	1	0	
(0x6C)	–	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	PCMSK1
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

PCMSK0 – Pin Change Mask Register 0

Bit	7	6	5	4	3	2	1	0	
(0x6B)	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	PCMSK0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	