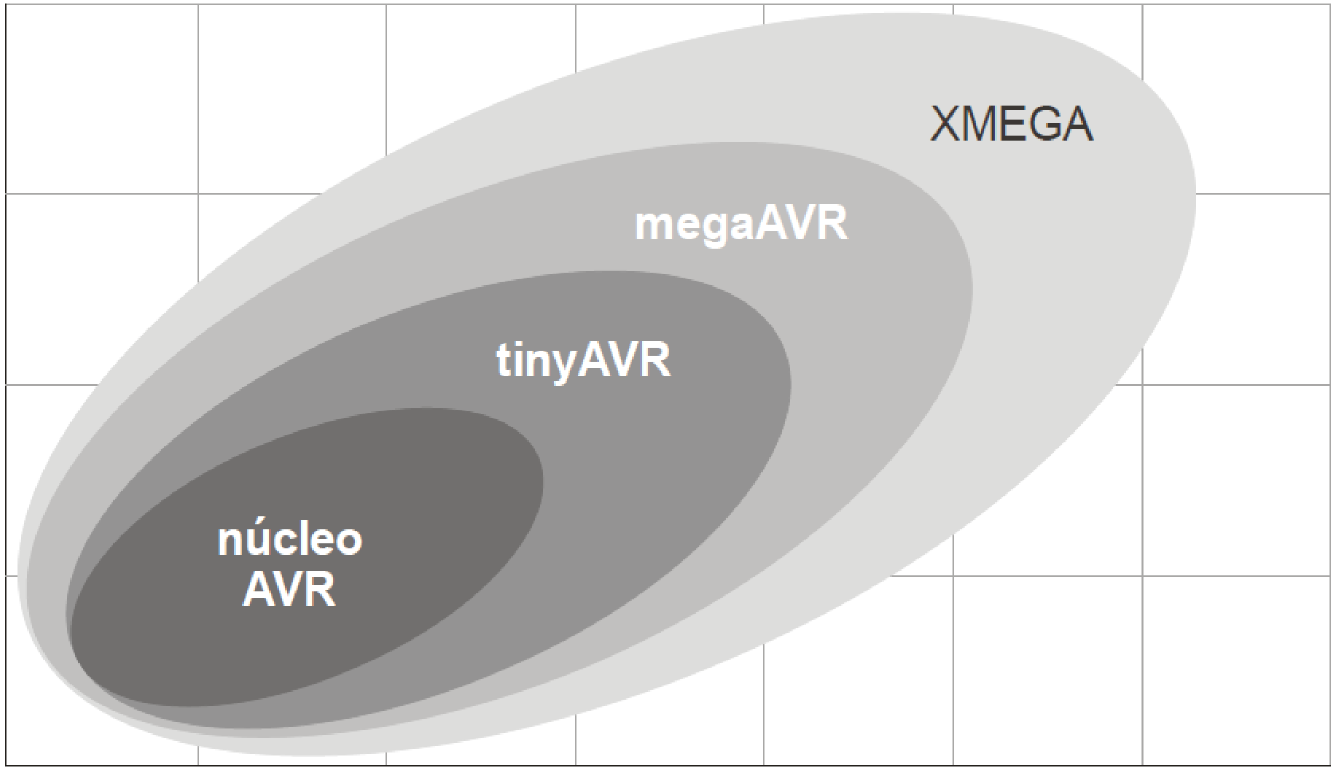
7. A microcontroller in deep

AVR Architecture: Family



- 8-bits RISC Architecture.
- Harvard architecture → Flash + (SRAM + EEPROM)
- Execution model Register-Register

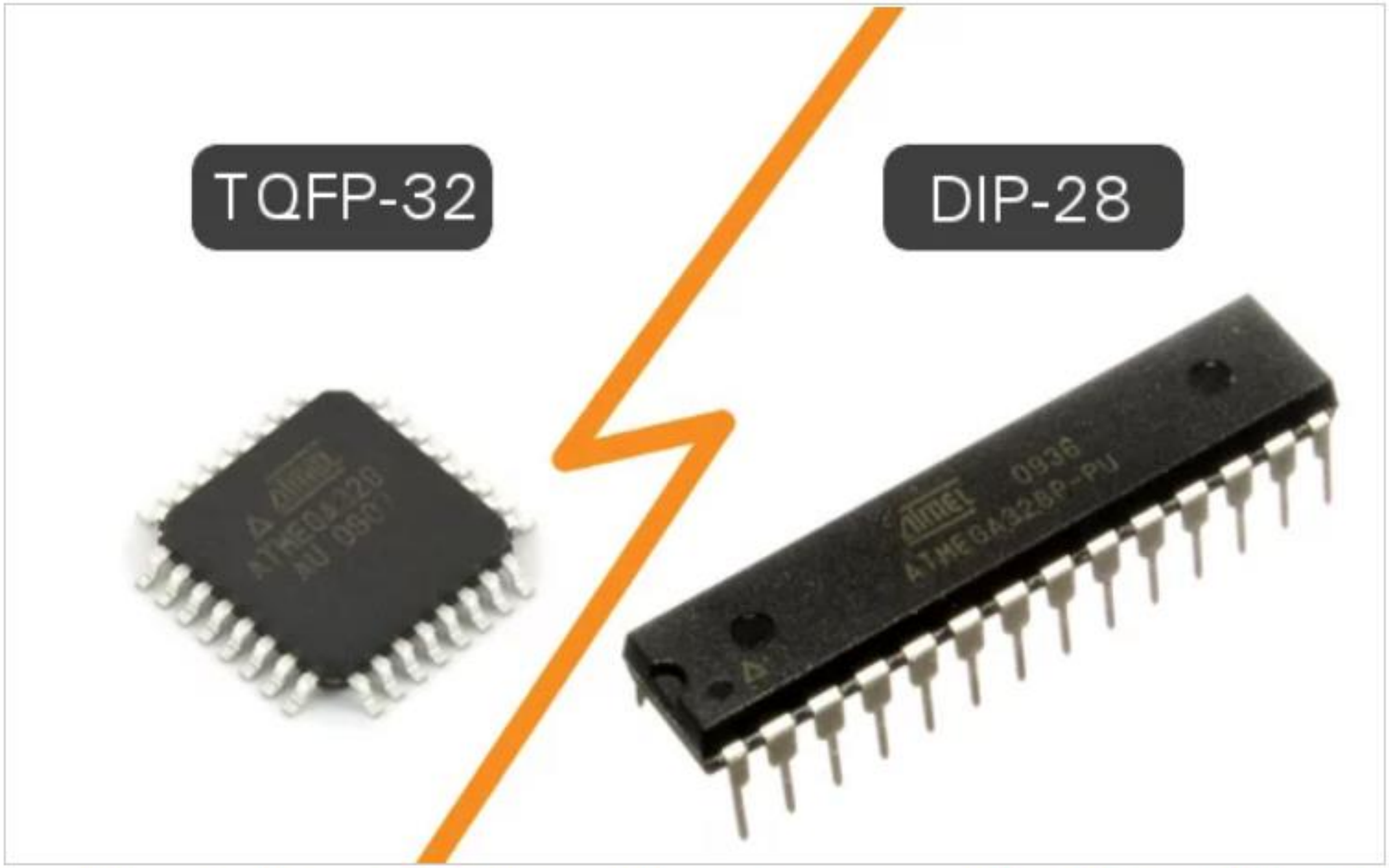
7.1. AVR Architecture (ATMega328)

AVR (ATMega328)

ATmegaX8PA

Dispositivos	**Flash** (Programa)	**EEPROM** (datos)	**SRAM** (datos)	Tamaño vector interrupción
ATmega48PA	4K Bytes	256 Bytes	512 Bytes	1 instrucción
ATmega88PA	8K Bytes	512 Bytes	1K Bytes	1 instrucción
ATmega168PA	16K Bytes	512 Bytes	1K Bytes	2 instrucciones
ATmega328P	32K Bytes	1K Bytes	2K Bytes	2 instrucciones

AVR PAckage (ATMega328)



Two different packages of the ATmega328. Images courtesy of Sparkfun and Wikimedia.

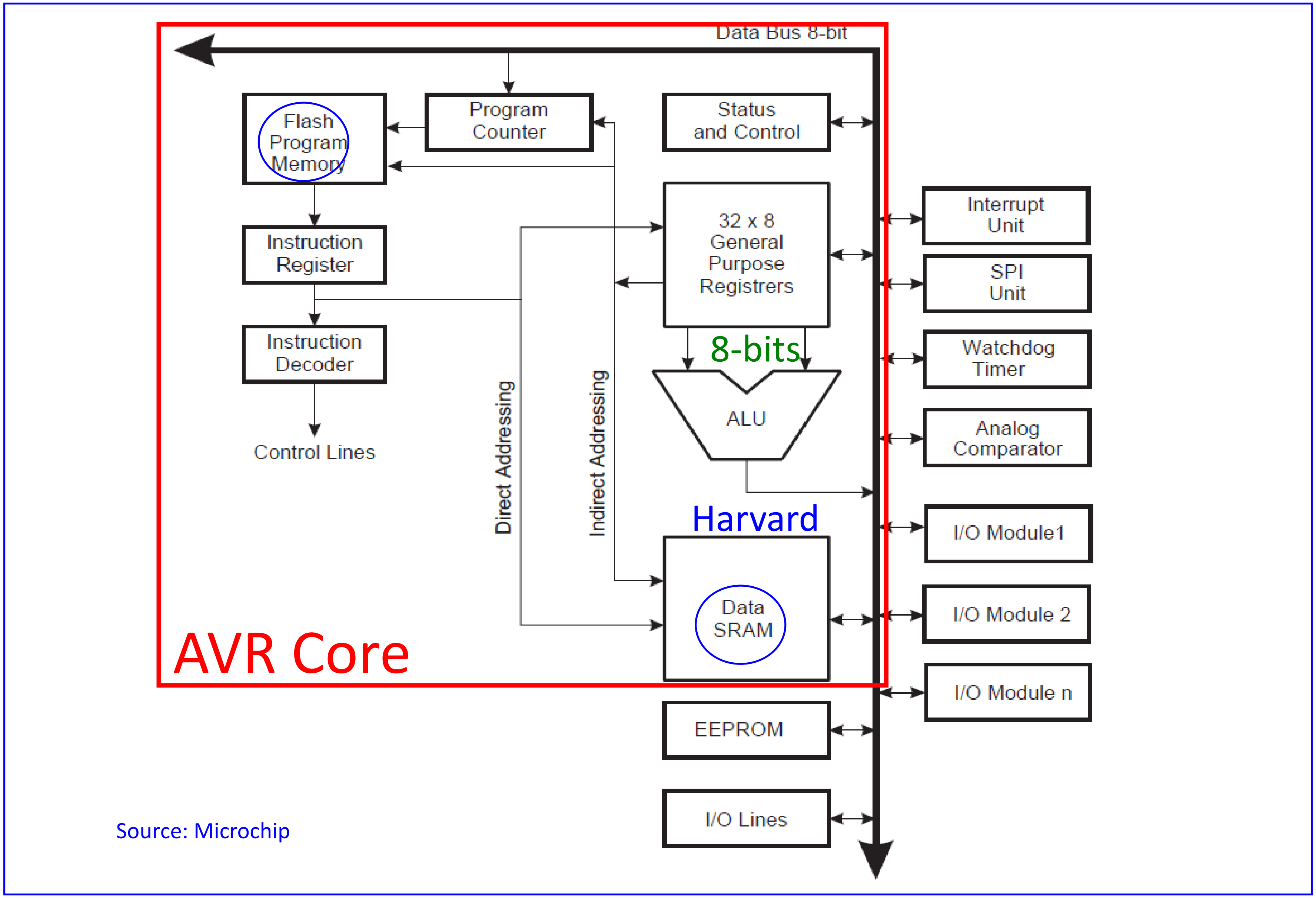
AVR Features (ATMega328)

- /4/8/16/32KBytes of In-System Programmable Flash
- 256/512/512/1Kbytes EEPROM
- 512/1K/1K/2Kbytes SRAM
- 32 general purpose 8-bit registers
- Three flexible Timer/Counters with compare modes
- Internal and external interrupt
- Serial programmable USART
- A byte-oriented 2-wire Serial Interface (TWI) → I2C
- SPI serial port
- 6-channel 10-bit ADC
- A programmable Watchdog Timer with internal Oscillator
- Five software selectable power saving modes

AVR Features (ATMega328)

- Supply voltages → 1.8 to 5.5 V.
- 5 power saving modes (Software)
- Clock speeds → 0 to 20 MHz (@4.5V)
- AVRs feature an on-chip oscillator and external clock options
- Some AVRs also have a system clock prescaler→ by up to 1024.
- Cycle-clocks per instruction:
  - With registers → 1 cycle
  - Memory, branch → 2 cycle

AVR Architecture: Core

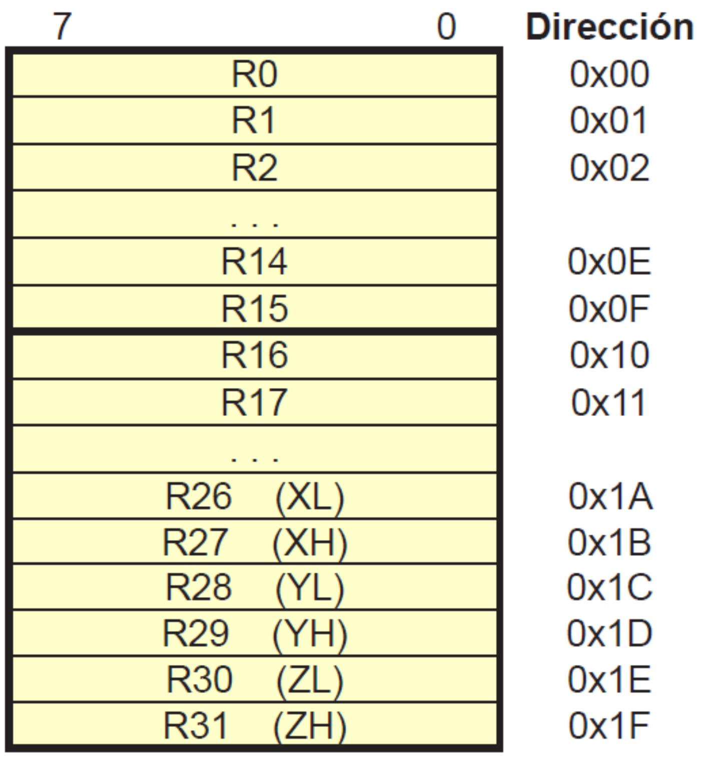


AVR Architecture

- Harvard architecture (Modified)
- The program memory is In-System Reprogrammable Flash memory.
- Program Flash memory space is divided in two sections:
  - Boot Program
  - Application Program
- Instructions → 16-bit or 32-bit
- Program flow is sequential → conditional and unconditional jump and call instructions.

AVR Architecture: Register-file

- 32 x 8-bit general purpose
- Single clock cycle access time→ single-cycle ALU operation
- In a typical ALU operation, two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File – in **<u>one clock cycle.</u>**



- 6 of the 32 registers → 3 pointers for Data Space addressing
- One of the these → for look up tables in Flash program memory.

AVR Architecture: More features

- Stack → data SRAM
- The Stack Pointer (SP) →I/O space (RAM).

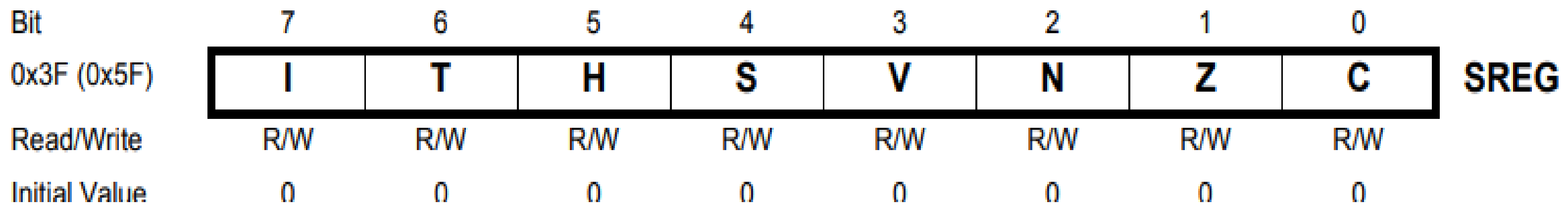
- Data SRAM → five addressing modes

- Global Interrupt Enable (I) bit in the Status Register.
- One Interrupt Vector for each interrupt.
- Interrupt Priority → The lower the Interrupt Vector address, the higher the priority.

AVR Architecture: More features

- ALU → arithmetic and logic operations between registers or between a constant and a register.
- Single register operations can also be executed in the ALU.
- The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions.
- Some implementations → multiplier

- Status Register updated after ALU



Bit	7	6	5	4	3	2	1	0	
0x3F (0x5F)	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

AVR Architecture: Instruction Execution Timing

Figure 7-4. The Parallel Instruction Fetches and Instruction Executions

16MHZ → 16 MIPS

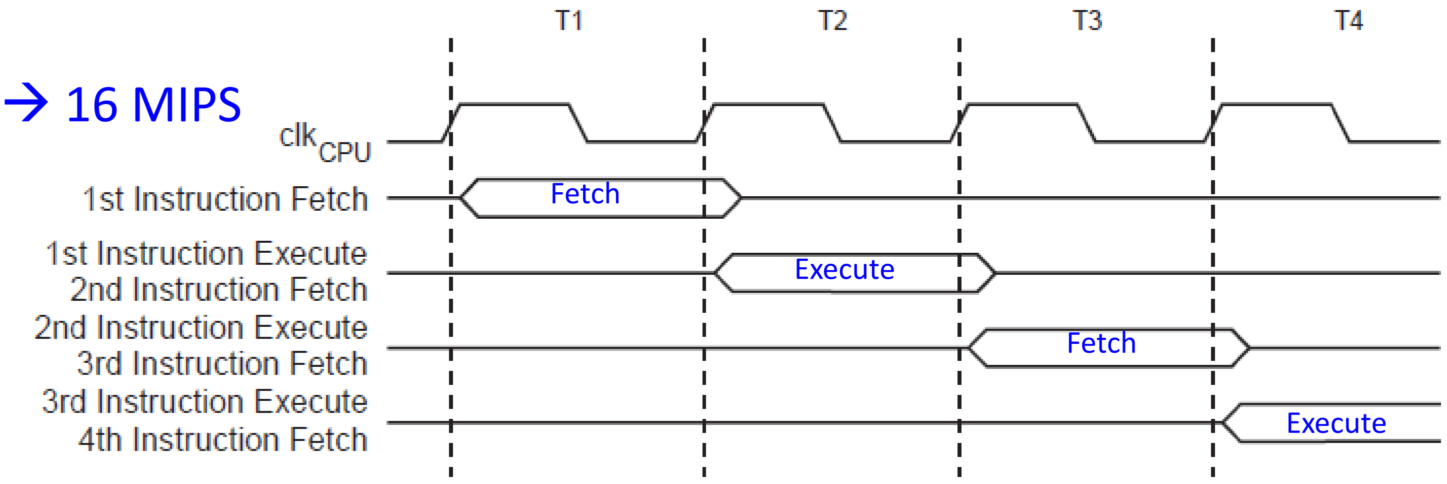
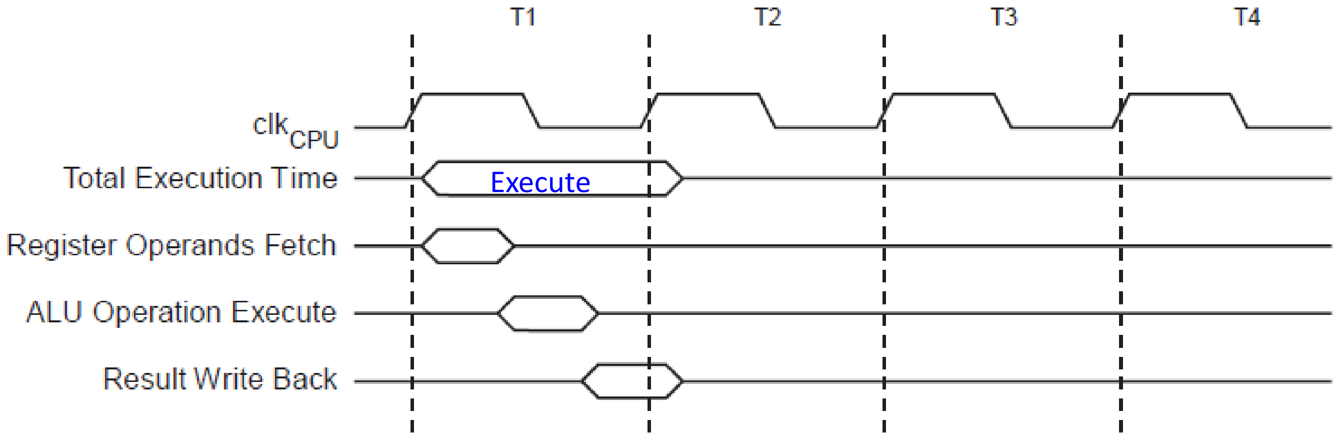
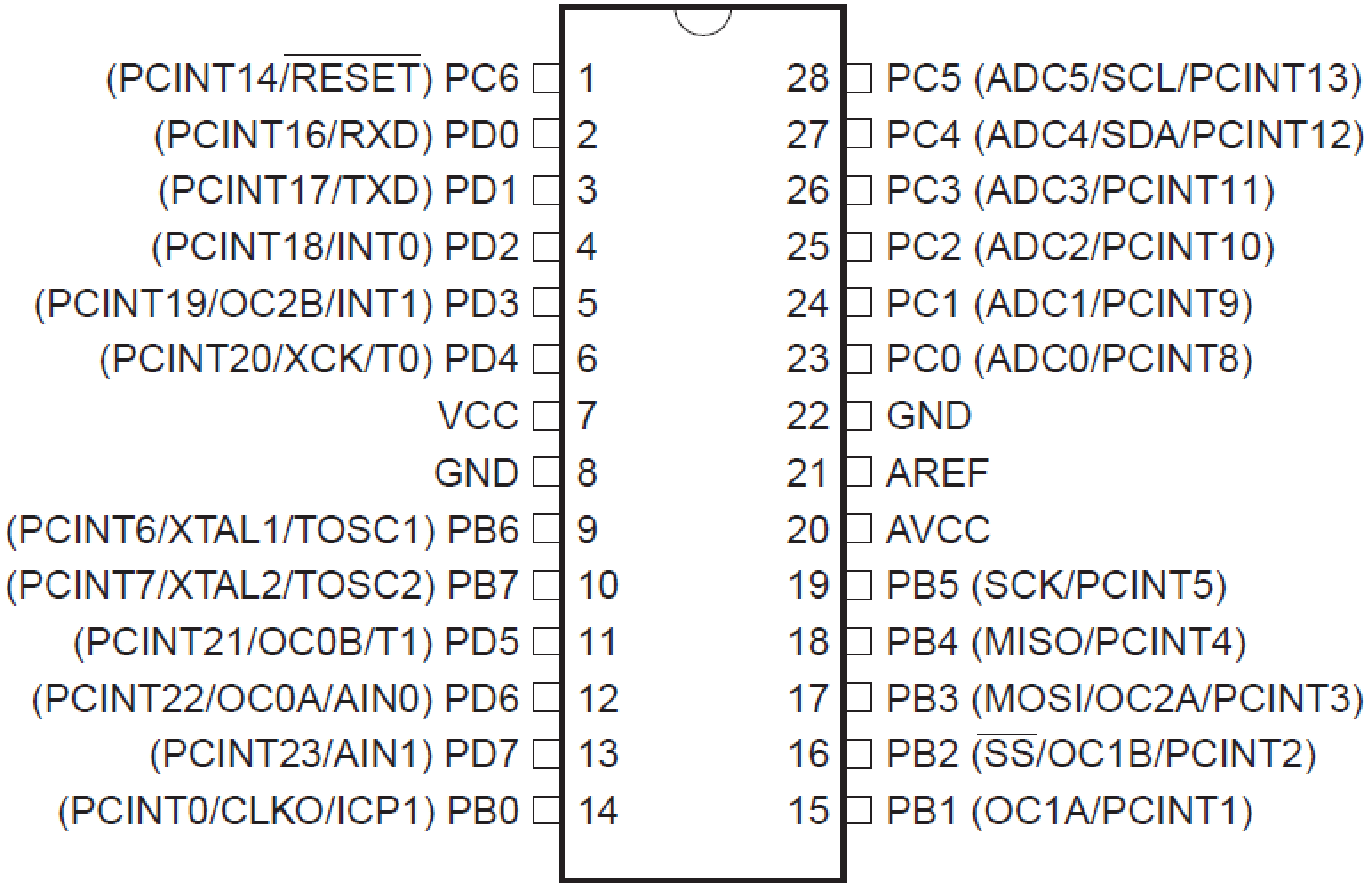


Figure 7-5. Single Cycle ALU Operation



Source: Microchip

I/O Ports



Source: Microchip

AVR Memory