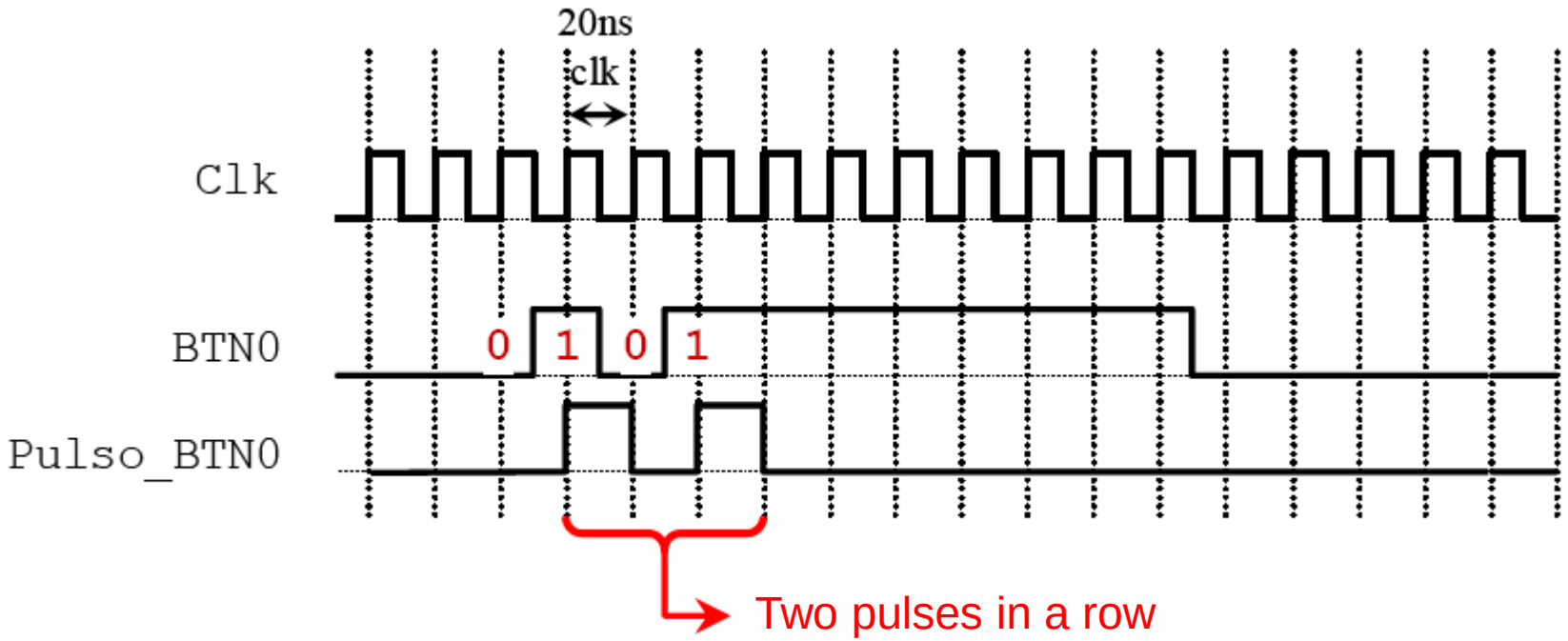
Lab_5. Designing Finite State Machines (FSM) in VHDL

5.1. Debounce circuit

Debounce circuit

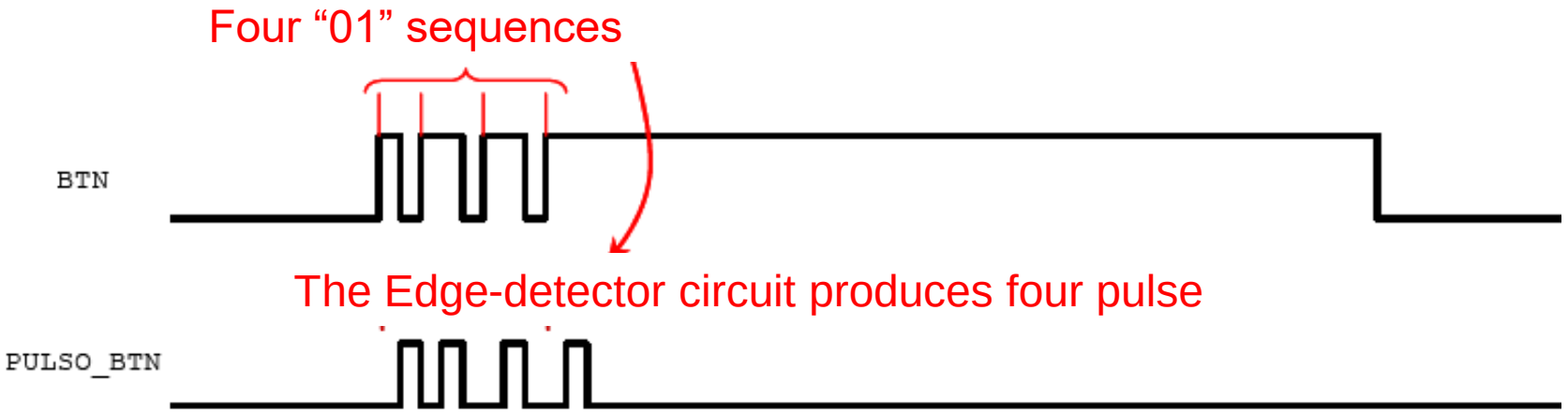
A one-cycle pulse is sent by the "edge detector" every time a “01” sequence is detected. However, following sequences could be detected because by the bouncing in the push button.

(An example is shown in the below image.)



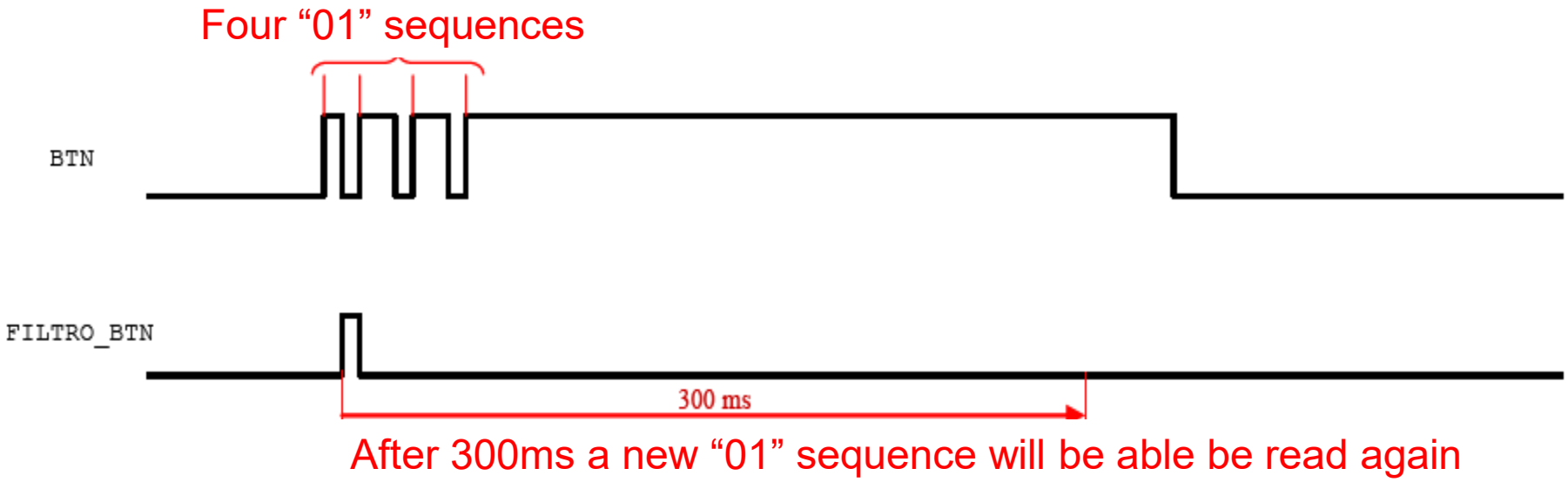
Debounce circuit

PROBLEM: the edge-detector circuit could not be enough. The image below shows four sequences detected.



Debounce circuit

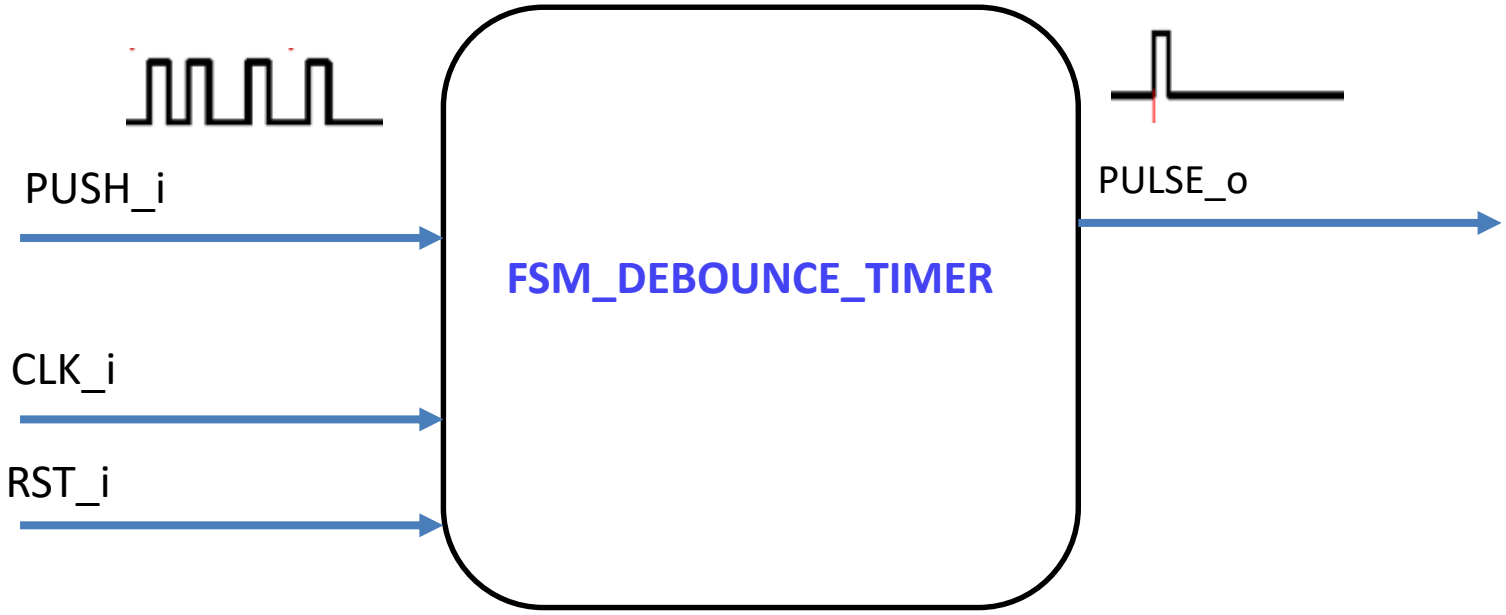
SOLUTION: To disable the edge-detector circuit as long as necessary to avoid reading new sequences coming from the bouncing in the push button.



Debounce circuit

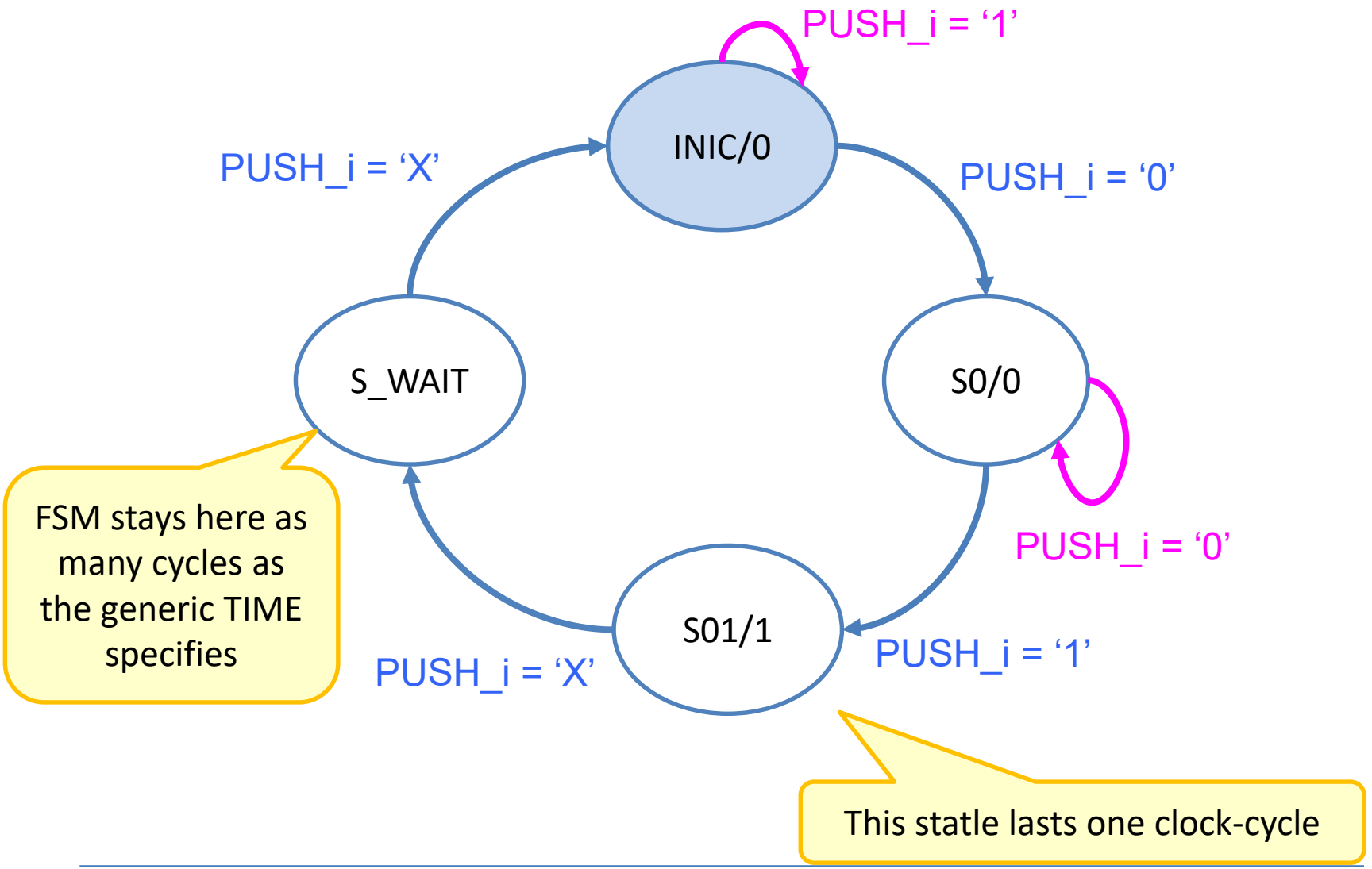
Project 28 : Debounce circuit with TIMER of 300ms

Project name: “P28_FSM_EDGE_DETECTOR”
File name: “FSM_DEBOUNCE_TIMER.vhd”



Debounce circuit

Project 28 : Debounce circuit by using FSM

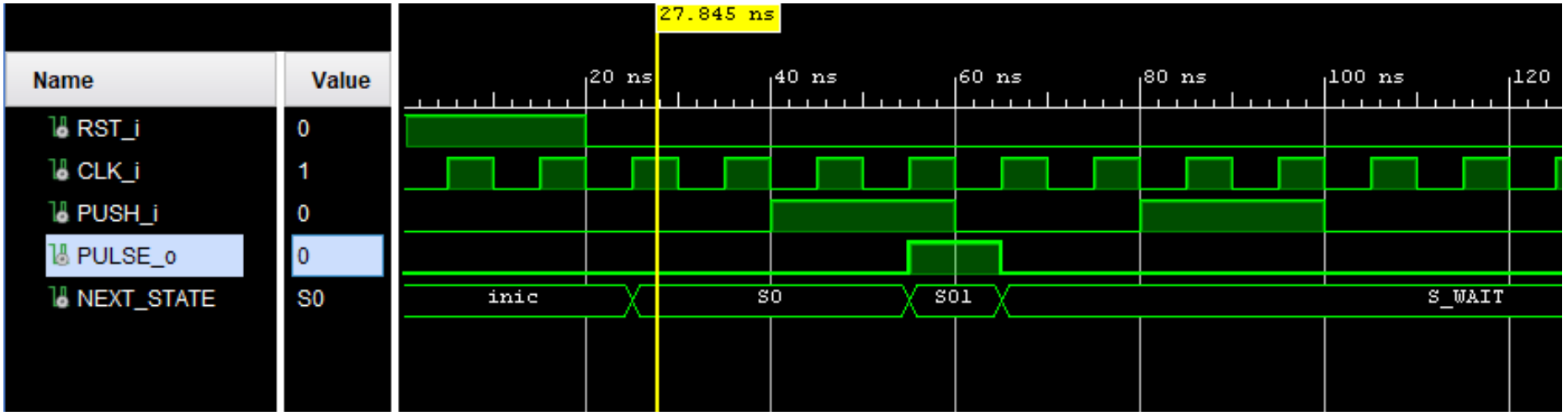


Debounce circuit

Project 28 : Debounce circuit with TIMER of 300ms

Add a testbench to check the right performance. To mimic the bouncing effect obtained when the button is pressed, assert the input "PUSH_i" several times in a row.

Debounce circuit



PUSH is delayed one clock-cycle