5.3. A very simple computer (DIDACOMP)

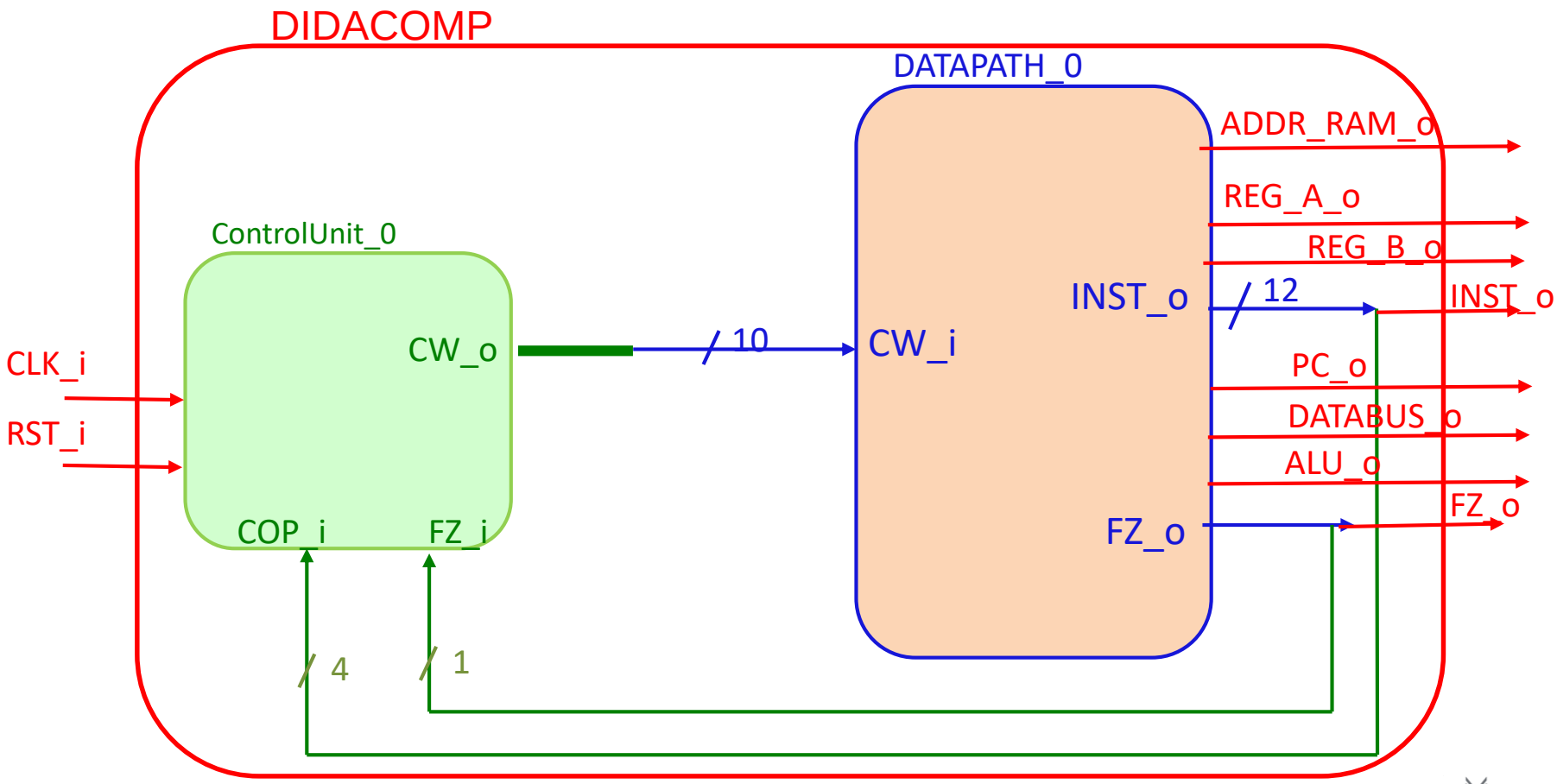
DidaComp

In a new project, **P29_DIDACOMP_ControlUnit**. Add a VHDL file describing the control unit, "**ControlUnit_0**". Add a **testbench** to check the right performance.

Make sure you add the internal signal "NextState" when you launch the simulator. That signal shows the different states of the FSM for each clock cycle.

DidaComp

In a new project, **P30_DIDACOMP_SIM**. Add a VHDL file to describe **DIDACOMP** in a structural way. **DIDACOMP** is the connection between the ***DATAPATH_0*** and ***ControlUnit_0***. Add a **testbench** to check the right performance.

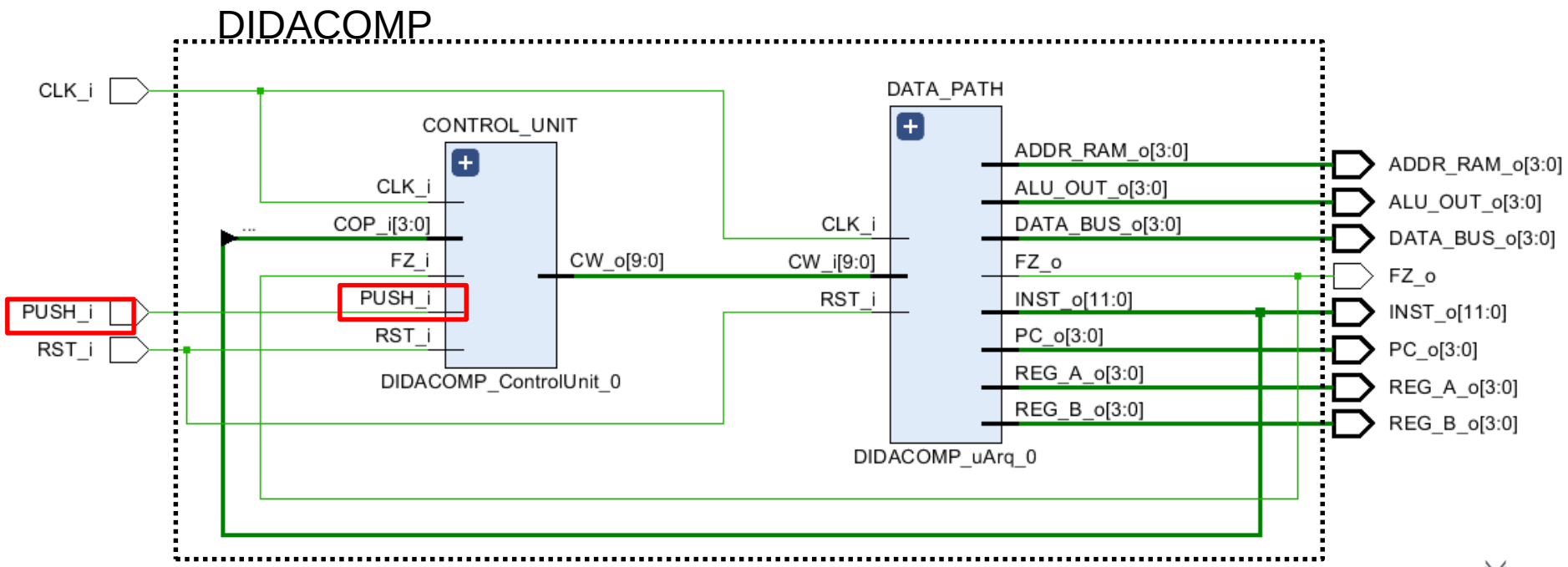


DidaComp_Nexys4

In a new project, **P31_DIDACOMP_Nexys**, add a new VHDL file, "**DIDACOMP_Nexys4**". It is consists of *uArq* and *ControlUnit_0*.

Some **modifications** must be done to see a right performance onto Nexys4:

1. In the file "ControlUnit_0" (make sure it is located as local), add a input called "PUSH_i".
2. Add it to the file "DIDACOMP_Nexys4" also and connect it as necessary.

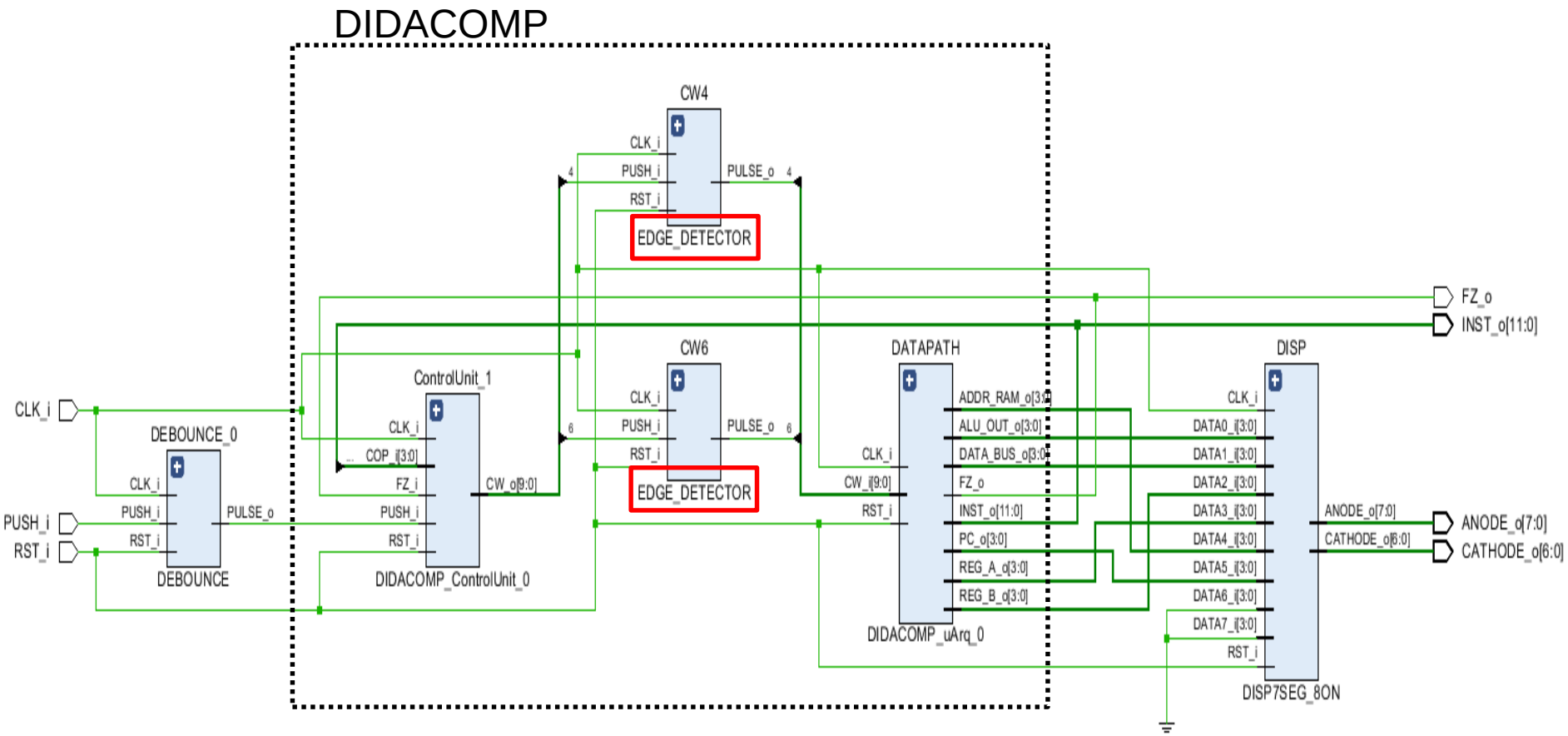


3. Modify the VHDL code to add the input “PUSH_i” in such only when it is pressed, the FSM changes.

```
----------------------------------------------------
--   3. FSM
----------------------------------------------------
if (PUSH_i = '1') then
    case NEXT_STATE is
    -- State "IDLE"
       when IDLE=>
            NEXT_STATE  <= LOAD;
    -- State "LOAD"
       when LOAD=>
           NEXT_STATE  <= DECO;
    -- State "DECO"
       when DECO=>
```

DidaComp_Nexys4

4. Modify Didacomp to add two “EDGE_DETECTOR” modules (P14) to turn into pulses the CW_o(6) and CW_o(4), REG_PC and REG_INST respectively.

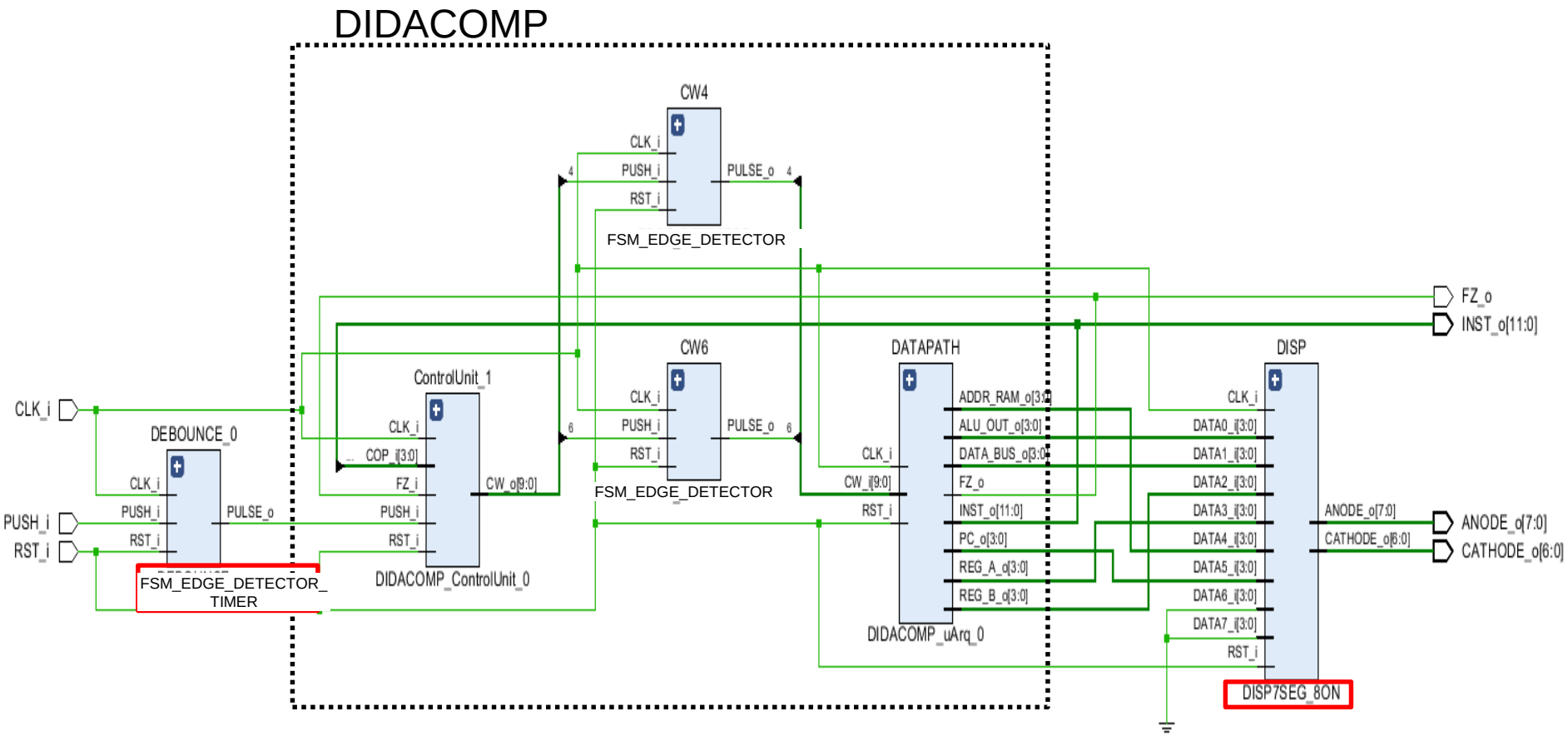


DidaComp_Nexys4

5. Add ”DEBOUNCE” (P27) module to avoid the bouncing in the pushbutton which controls “PUSH_i”.

6. As usual, connect the “DISP7SEG_8ON” module to monitor the ports in DIDACOMP

7. Do not forget assign the signals INST and FZ to the ports INST_o and FZ_o (LEDs in board)



DidaComp_Nexys4

- Finally, add the constraints file and generate the bitstream. Connect the LED for showing the instructions and FZ, ANODE and CATHODE, and one pushbutton for RST_i and another one to PUSH_i.
- Download the bitstream and verify the right performance of DIDACOMP in Nexys4.