```vhdl
----------------------------------------------------------------------------------
-- Company: UCA
-- Engineer: Mirian Cifredo
--
-- Create Date: 15.10.2018 11:41:34
-- Design Name:
-- Module Name: ALU_0_N_bits - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
-- ----------------------------------------------------------------------------------
-- Generic ALU --> Operations:
--                     * MOV A
--                     * INC A
--                     * A + B
--                     * A - B
-- ----------------------------------------------------------------------------------
-- Dependencies: No.
-- ----------------------------------------------------------------------------------
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- ----------------------------------------------------------------------------------
-- Topics:
-- 1. Simple ALU, concurrent statement (WITH-SELECT)
-- 2. ARithmetic operations: ADD and SUB (use IEEE.NUMERIC_STD.ALL, +,-)
-- 3. Casting: STD_LOGIC_VECTOR to SIGNED and UNSIGNED
-- 4. Output assigment with OTHERS
-- 5. Constant ZERO for comparison purpose
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity ALU_0_N_bits is
    generic ( DATA_WIDTH: positive:=4);
    Port ( A_i   : in STD_LOGIC_VECTOR (DATA_WIDTH-1 downto 0);
           B_i   : in STD_LOGIC_VECTOR (DATA_WIDTH-1 downto 0);
           OP_i  : in STD_LOGIC_VECTOR (1 downto 0);
           RESULT_o : out STD_LOGIC_VECTOR (DATA_WIDTH-1 downto 0);
           ZERO_F_o : out STD_LOGIC);
end ALU_0_N_bits;

architecture Behavioral of ALU_0_N_bits is
---------------------------- SIGNALS -------------------------------------
 signal A,B     : unsigned(DATA_WIDTH-1 downto 0);
 signal RESULT  : unsigned(DATA_WIDTH-1 downto 0);
---------------------------CONSTANTS-------------------------------------
 constant ZERO  : unsigned(DATA_WIDTH-1 downto 0):=(others=>'0');
---------------------------------------------------------------------------
begin
-- Inputs casting----
A <= unsigned(A_i);
B <= unsigned(B_i);
---------------------------------------------------------------------------
-- Output Selected assignment depending on the "OP_i" value
-- The value default is filled with '0' thanks to clause OTHERS
with OP_i select
      RESULT <=   A               when "00",  -- MOV
                  A + 1           when "01",  -- INC A
                  A + B           when "10",  -- ADD A,B
                  A - B           when "11",  -- SUB A,B
                 -- (others=>'0') when others; -- Suitable for any DATA_WIDTH
                  ZERO            when others; -- Suitable for any DATA_WIDTH
---------------------------------------------------------------------------
-- Assigning value to the outputs
ZERO_F_o <= '1'  when RESULT = ZERO else '0';
RESULT_o <= STD_LOGIC_VECTOR(RESULT);-- Output casting.

end Behavioral;

```