

IC Design using Open-Source EDA + IHP SG13G2 PDK

Jorge Marin

Research Associate, AC3E-UTFSM

UCLouvain, Belgium – October 30, 2025



UNIVERSIDAD TECNICA
FEDERICO SANTA MARIA



About me

➤ Academic Degrees

- Ph.D. in Electrical Engineering. KU Leuven, Belgium, 2018.
 - KU Leuven Doctoral fellowship + IWT-Flanders research project grant
- MsC degree in Electrical Engineering. KU Leuven, Belgium, 2012.
- BsC/MsC in Electrical Engineering. Universidad de Chile, Santiago, Chile, 2010.

➤ Work Experience

- Research Associate at Advanced Center for Electrical and Electronic Engineering (AC3E), USM, Valparaíso.
- Postdoctoral Research Fellow at AC3E-USM, Valparaíso, Chile, 2022-2023.
- Analog Designer. Sony Depthsensing Solutions 2020 – 2021.
- Analog Designer. ICSense (TDK) 2018 – 2020.
- Engineer Intern/ Engineer. Synopsys R&D Center, Santiago, Chile 2006 - 2009.
- Lecturer and TA, 2008 - 2025
 - Universidad de Chile, Universidad de los Andes (Chile), KU Leuven, USM
 - Digital Systems, Analog Integrated Circuit Design, Analog IC Design Lab

➤ Other roles

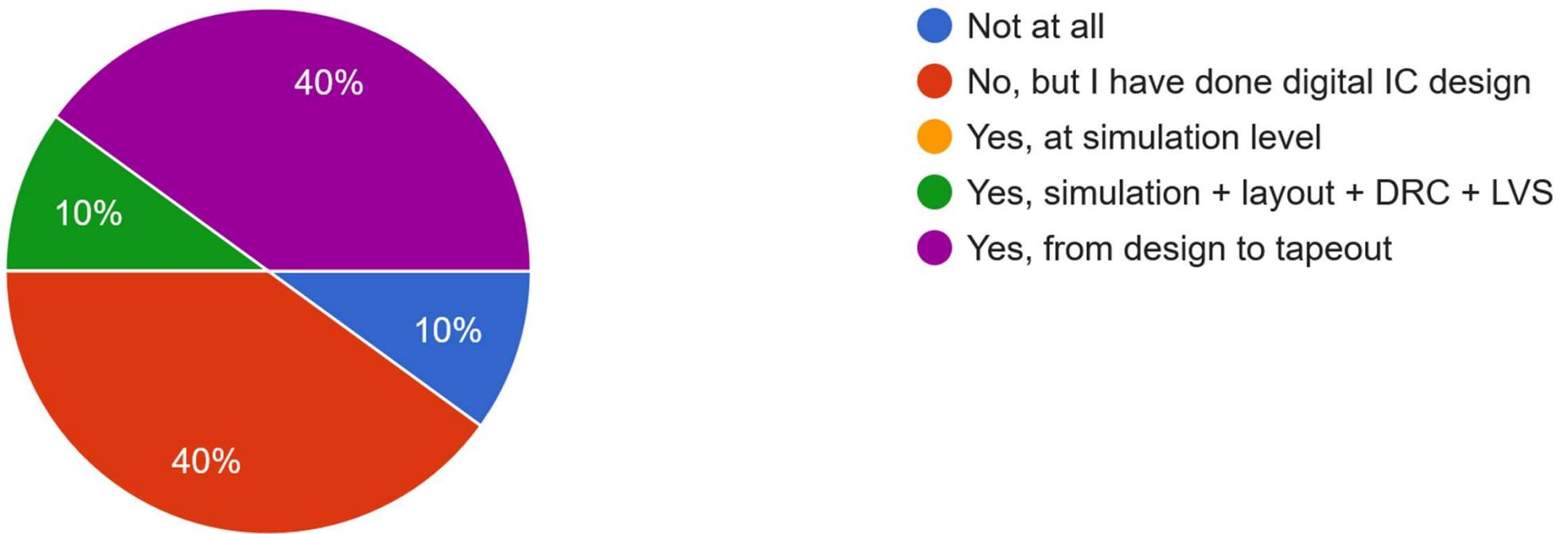
- IEEE CASS/SSCS/EDS joint chapter chair
- IEEE CICC TPC member
- UNIC-CASS educational program team lead



About you

Do you have previous experience with analog/mixed signal IC design?

10 responses



Agenda

- Introduction
- Part I: OS silicon ecosystem overview (1.5h)
 - Open-source EDA tools and PDKs
 - Silicon-verified research using OS tools + PDKs
 - Simulation examples
 - Layout examples
- Part II: hands-on (mini) project (2h)

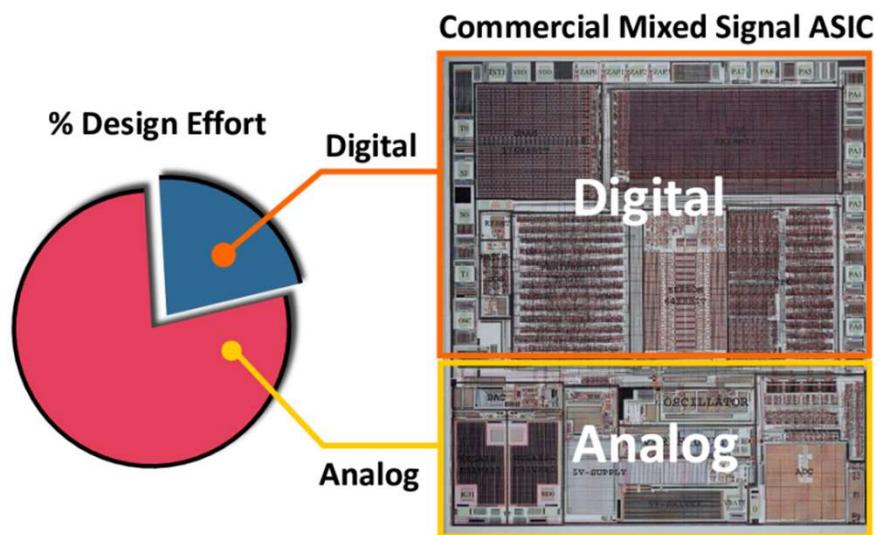
Part I: OS silicon ecosystem overview

Introduction

Introduction

- (1) Analog/mixed-signal design requires large effort

[Rutenbar, 2010]

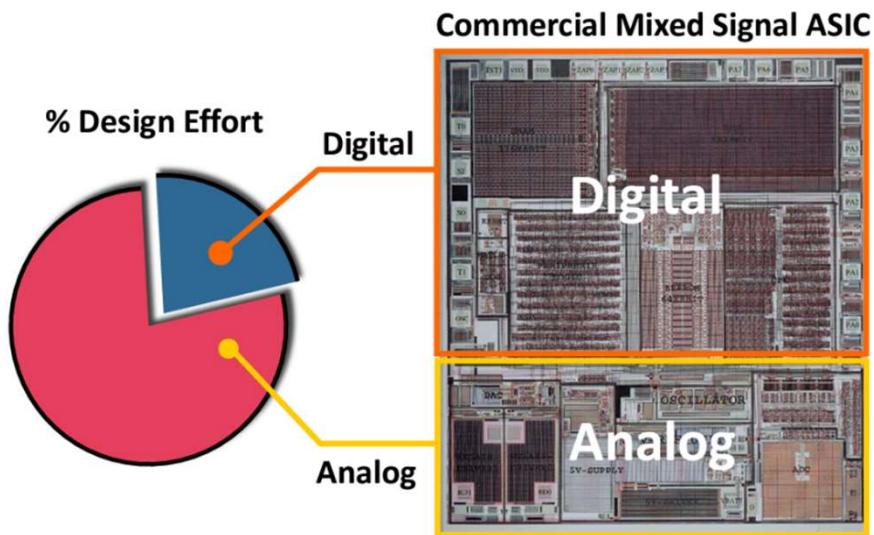


(1)

Introduction

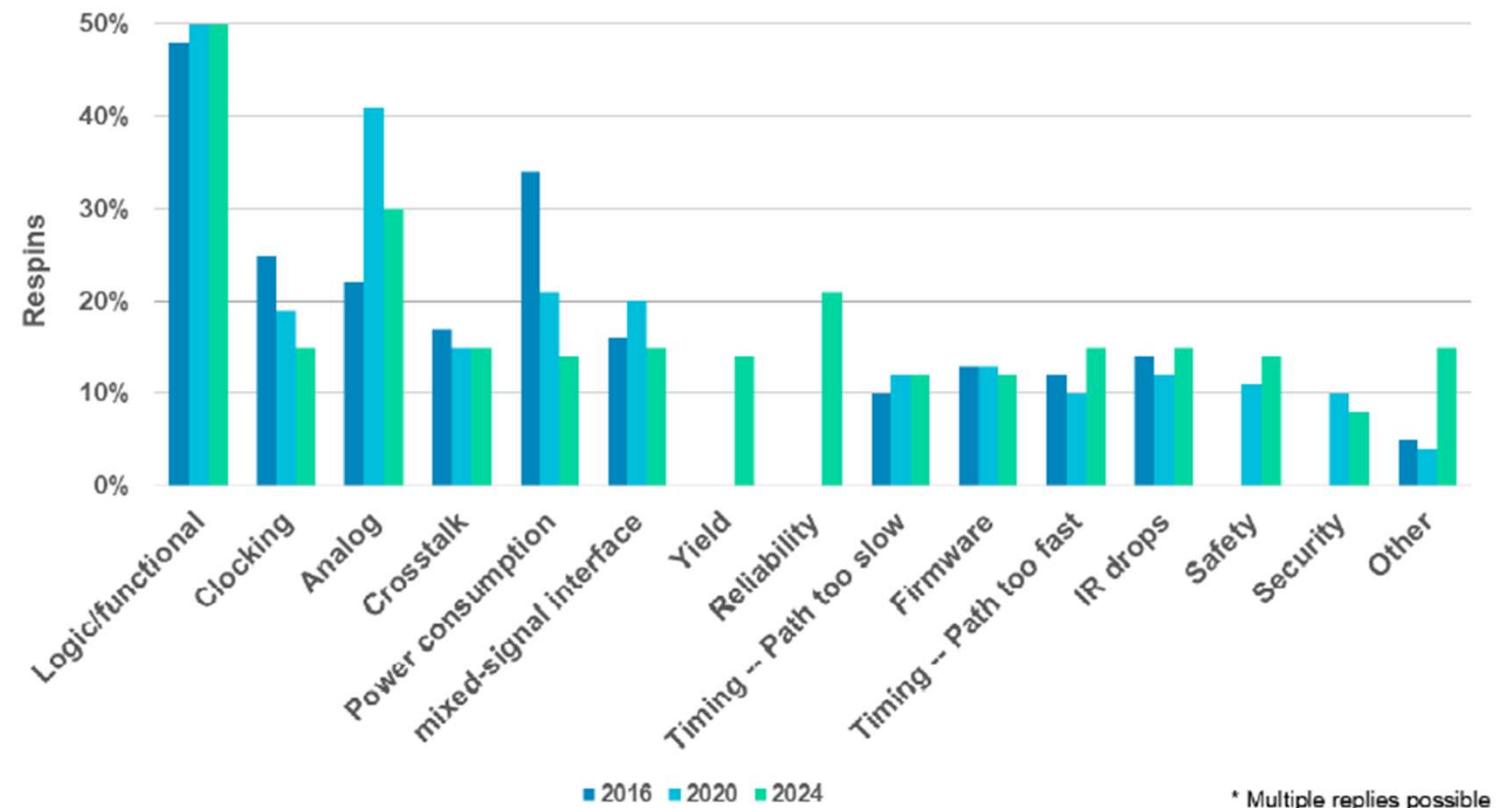
- (1) Analog/mixed-signal design requires large effort
- (2) A large percentage of flaws contributing to respins comes from analog

[Rutenbar, 2010]



(1)

[Siemens, 2024]



(2)

* Multiple replies possible

Introduction

How to move forward in analog/mixed signal chip design innovation?

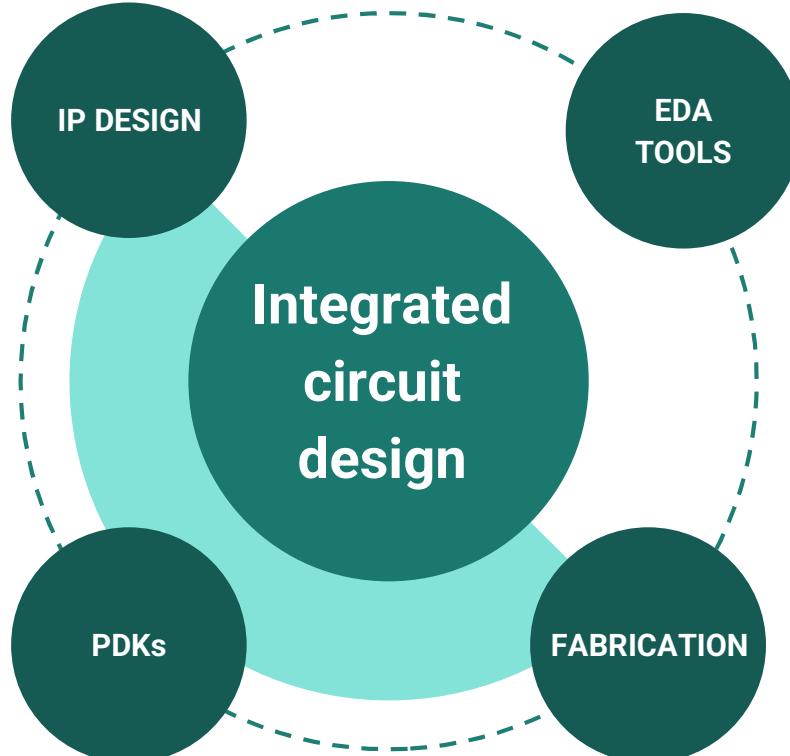
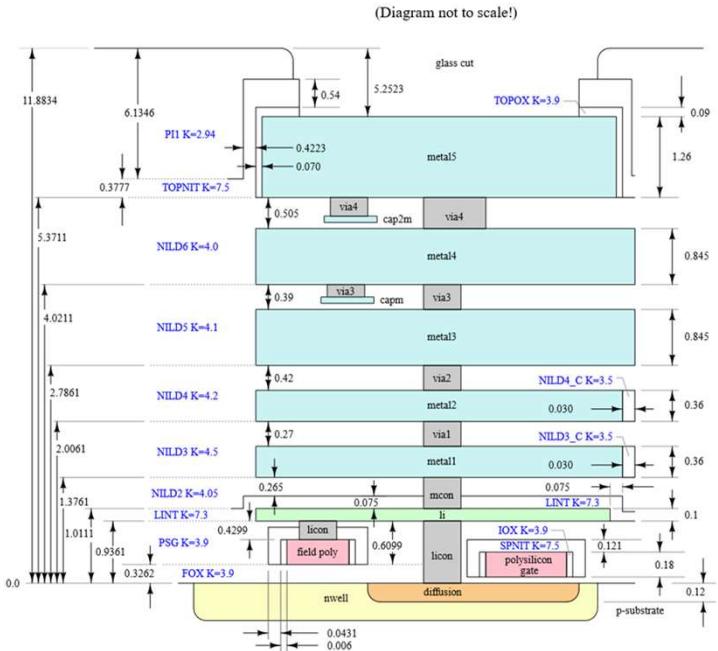
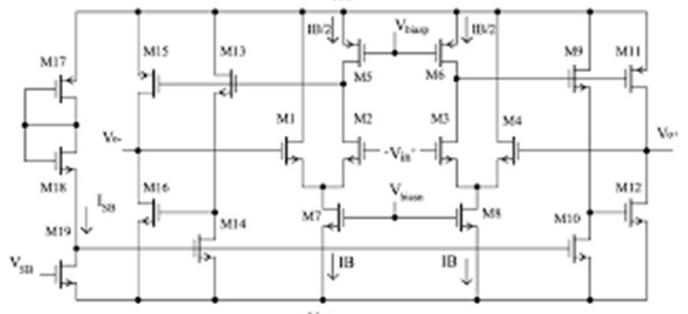
→ Current challenges for academia:

- Expand training capabilities for the next generation of designers
- Figure out flexible and affordable toolkits
- Improve the design-silicon validation cycle

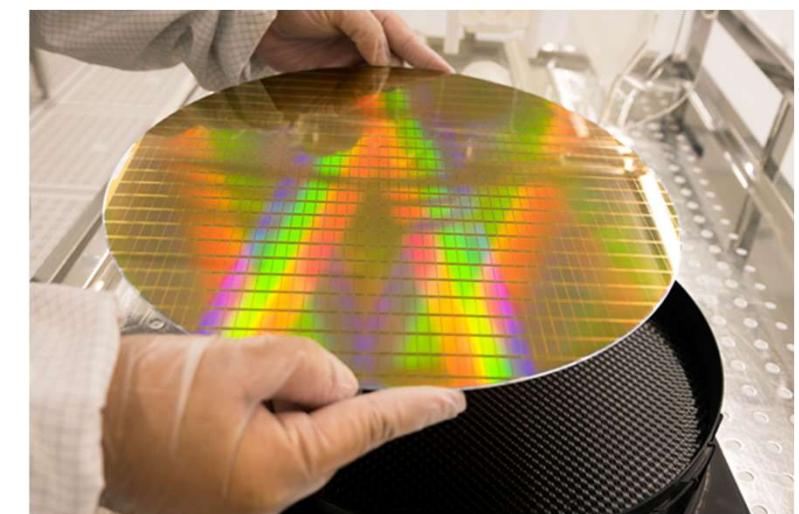
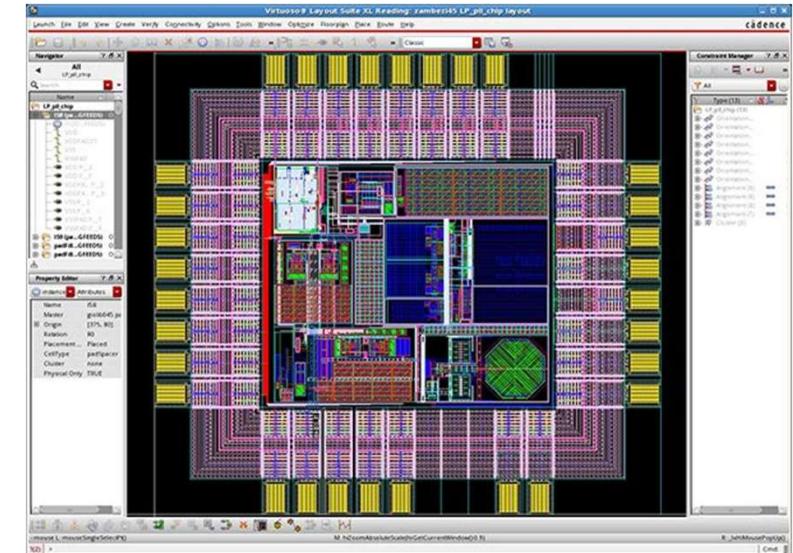
The current IC design ecosystem is not keeping the pace!

Introduction

Entry barriers in traditional IC design

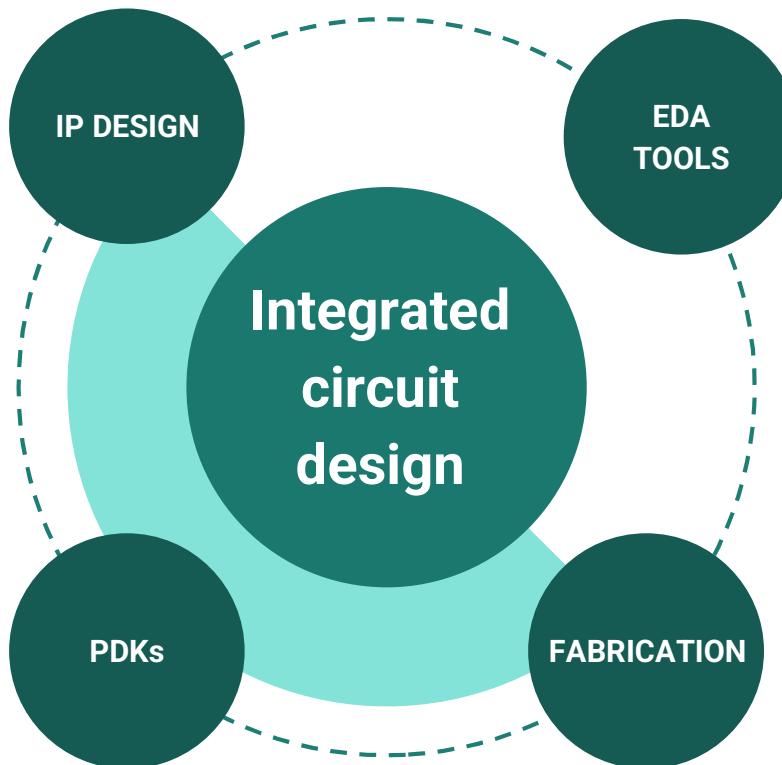
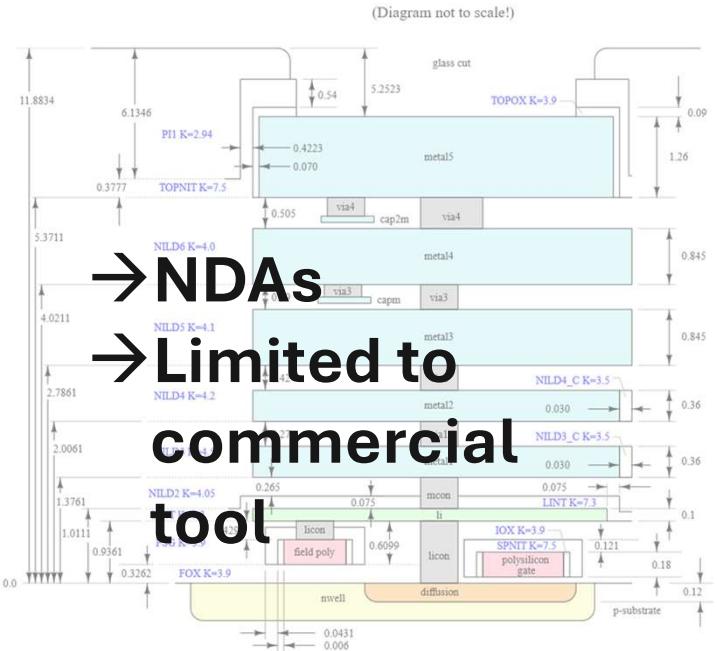
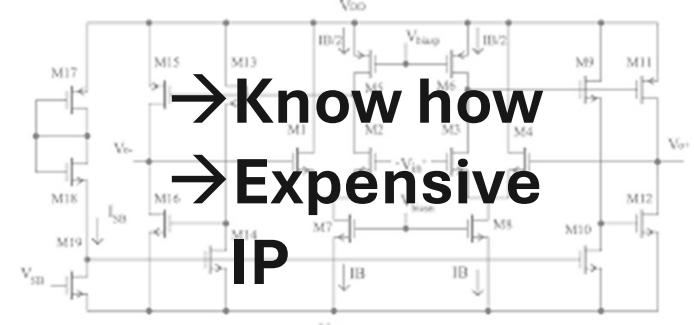


[Tim Ansell, FOSSi Dial-Up2020]

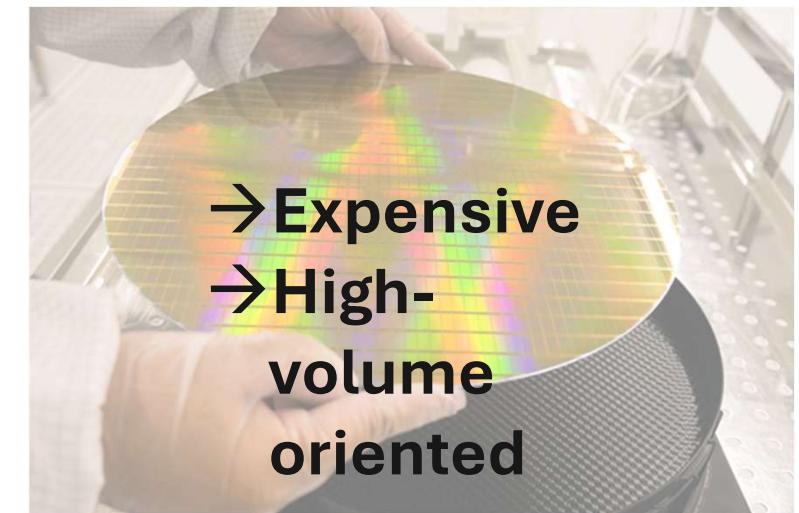
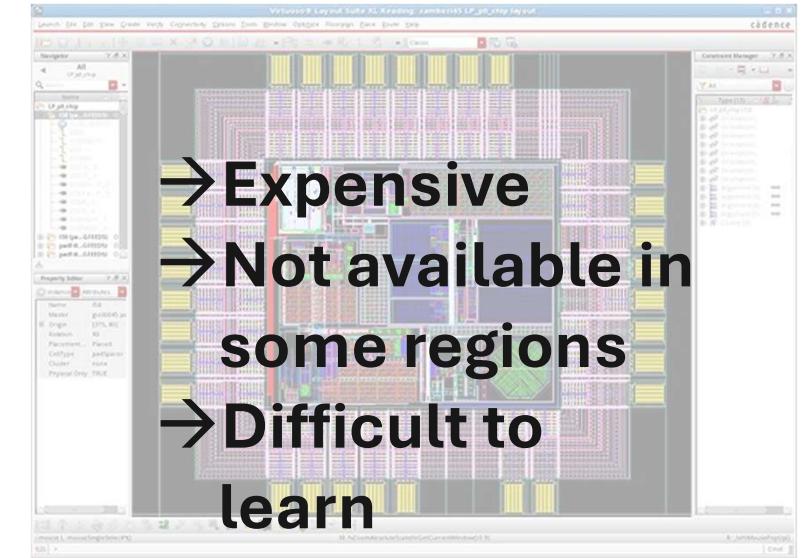


Introduction

Entry barriers in traditional IC design



[Tim Ansell, FOSSI Dial-Up2020]

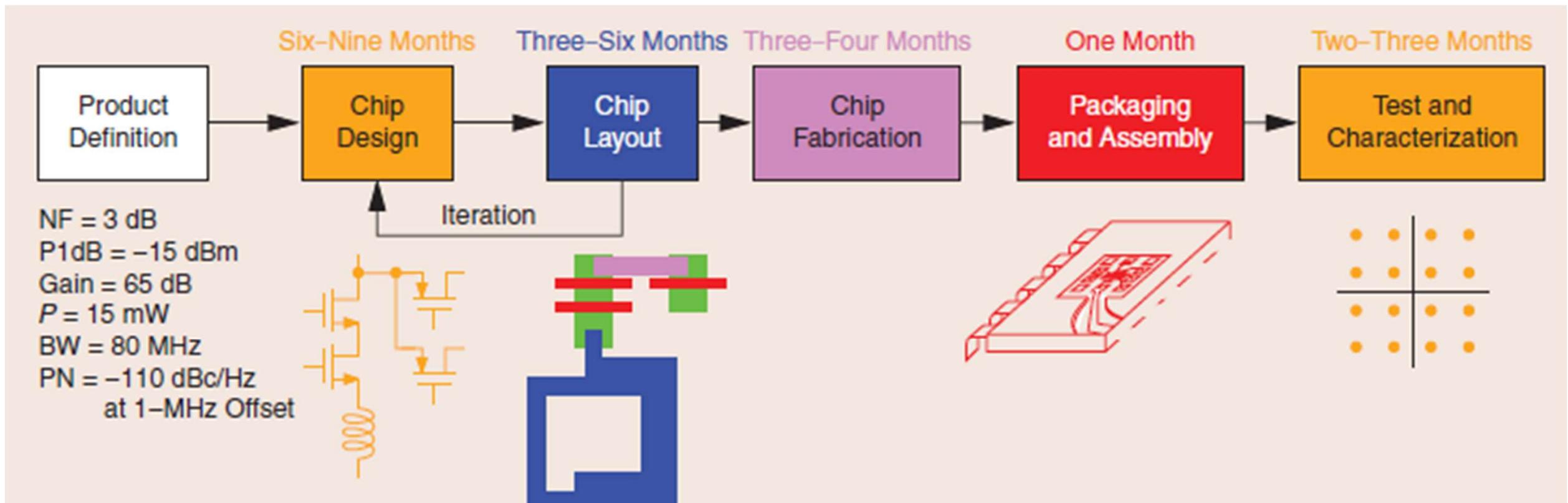


→Expensive
→Not available in some regions
→Difficult to learn

→Expensive
→High-volume oriented

Introduction

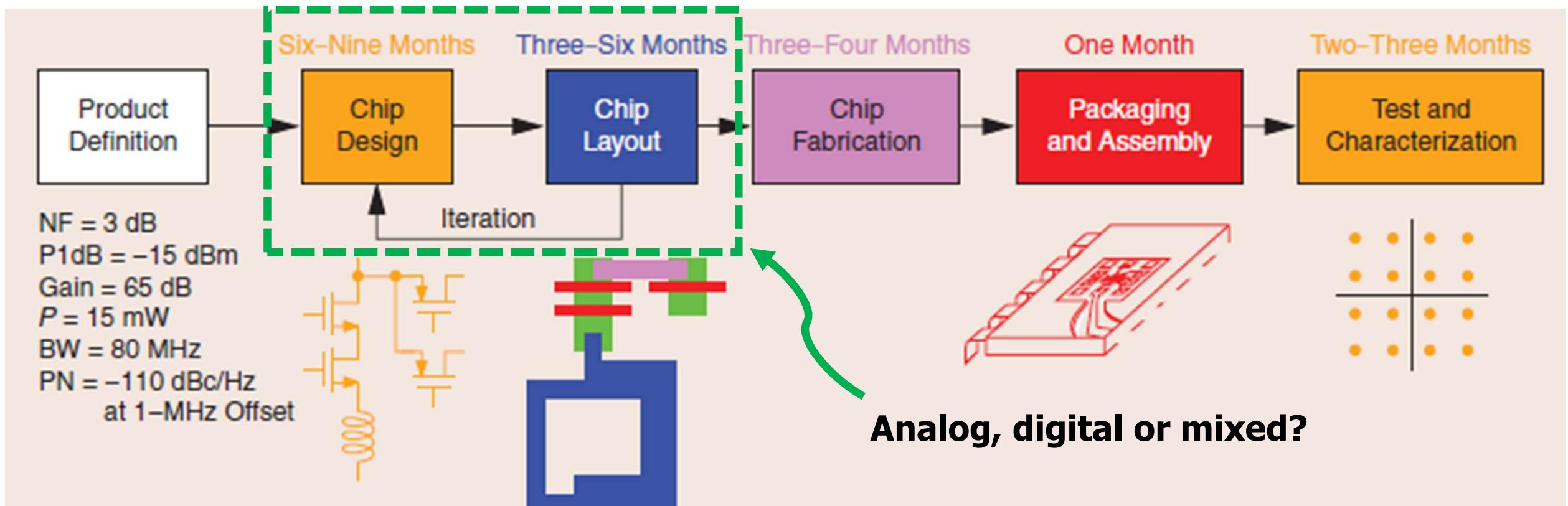
Silicon-proven IC design



[RAZAVI, IEEE SSCMAG 2024]

Introduction

Silicon-proven IC design

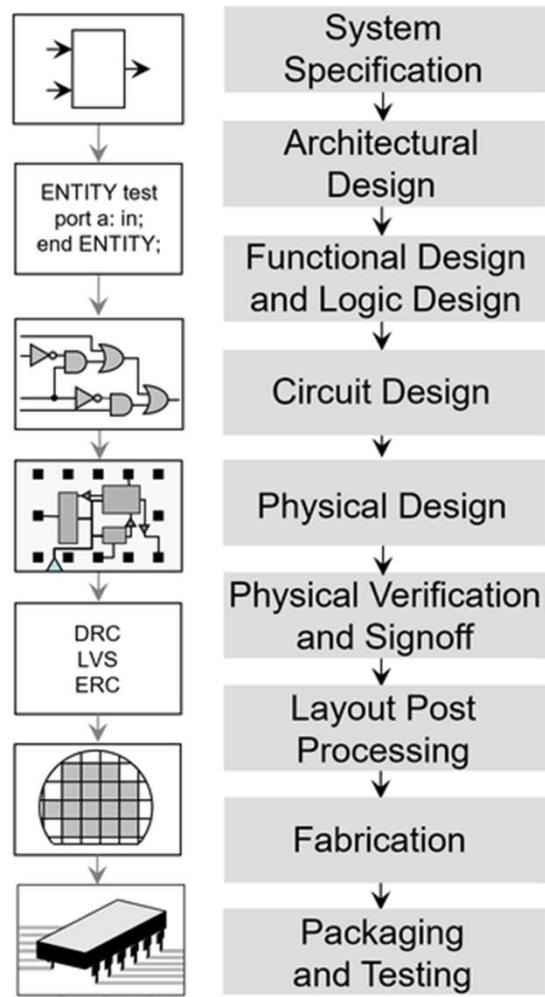


[RAZAVI, IEEE SSCMAG 2024]

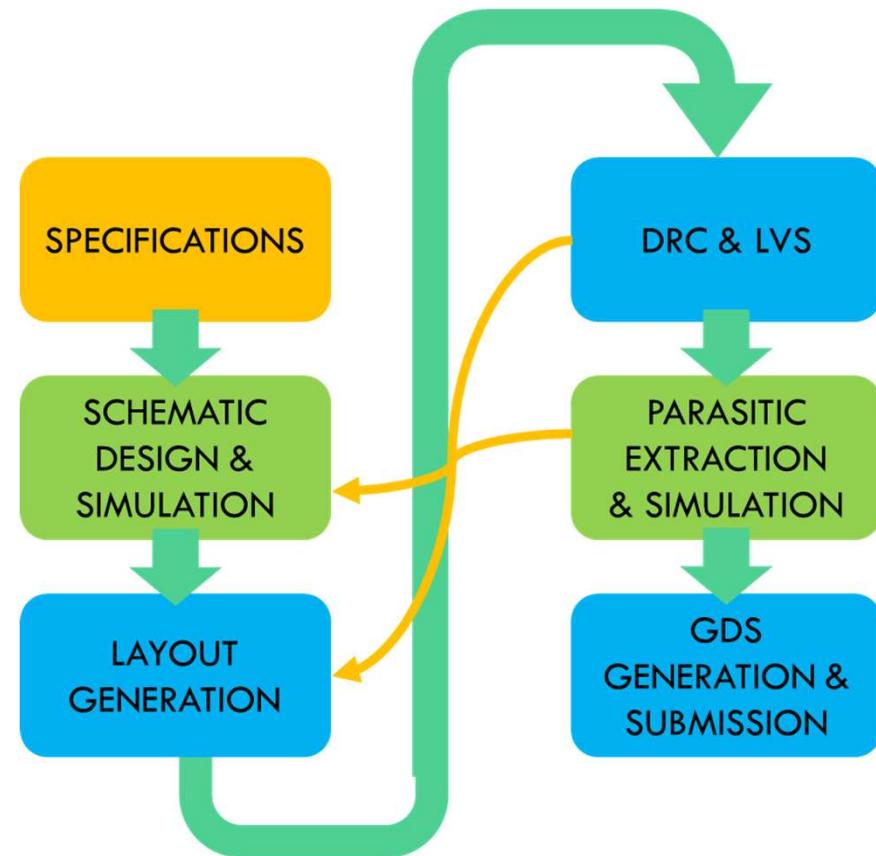
IC design flows

Digital versus analog methodologies

DIGITAL FLOW



ANALOG FLOW



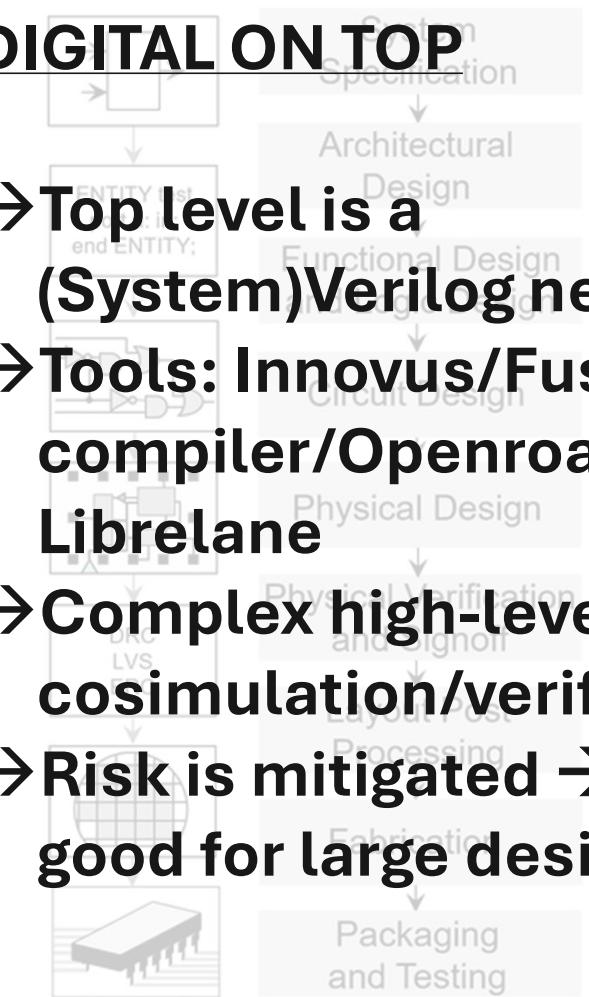
IC design flows

Digital versus analog methodologies

DIGITAL FLOW

DIGITAL ON TOP

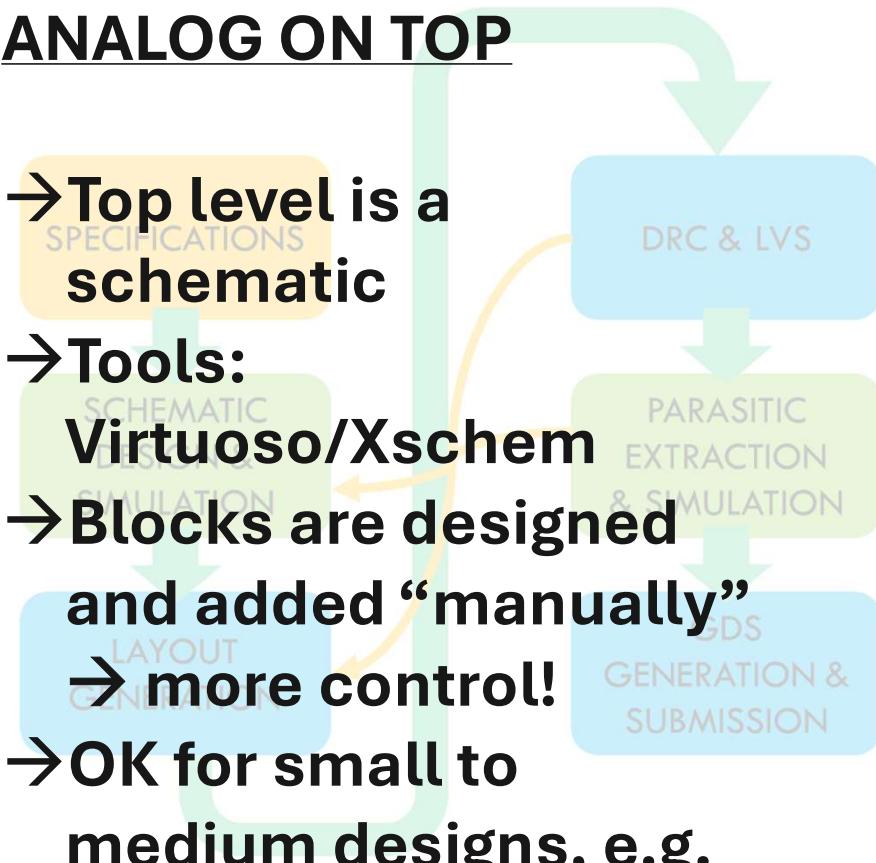
- Top level is a (System)Verilog netlist
- Tools: Innovus/Fusion compiler/Openroad-LibreLane
- Complex high-level cosimulation/verif.
- Risk is mitigated → good for large designs!



ANALOG FLOW

ANALOG ON TOP

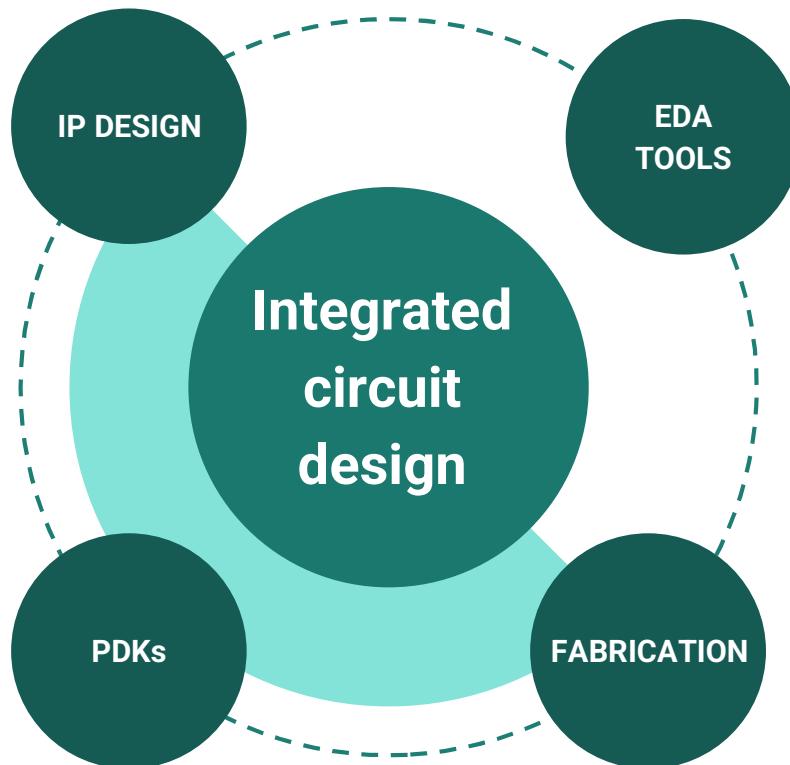
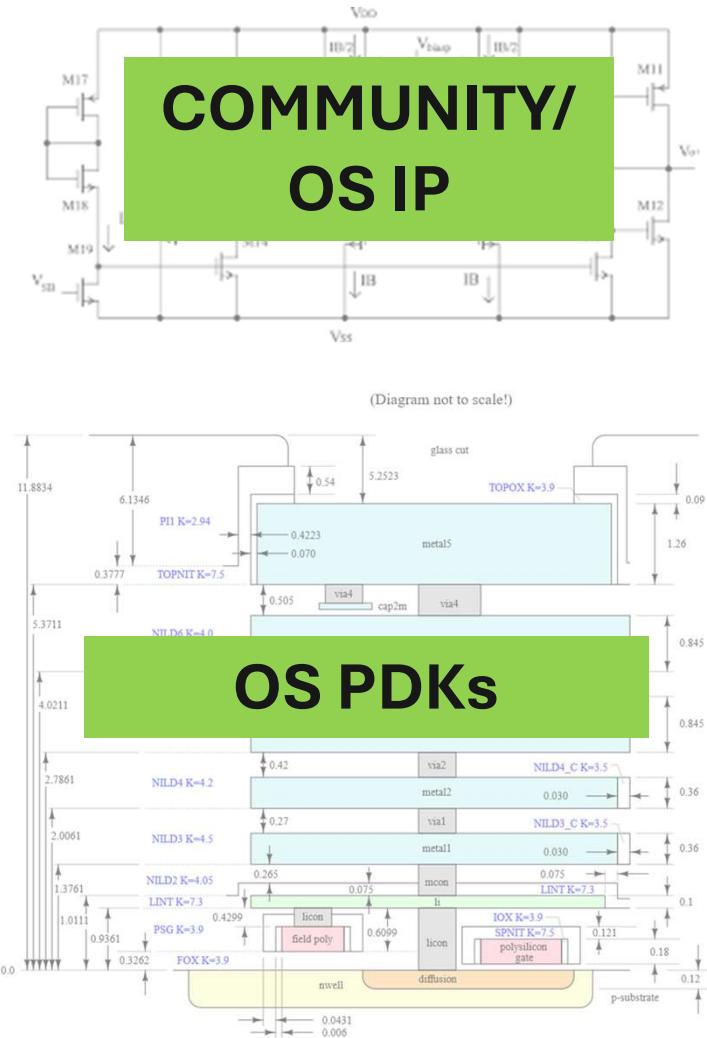
- Top level is a schematic
- Tools: Virtuoso/Xschem
- Blocks are designed and added “manually”
 - more control!
- OK for small to medium designs, e.g. research prototypes



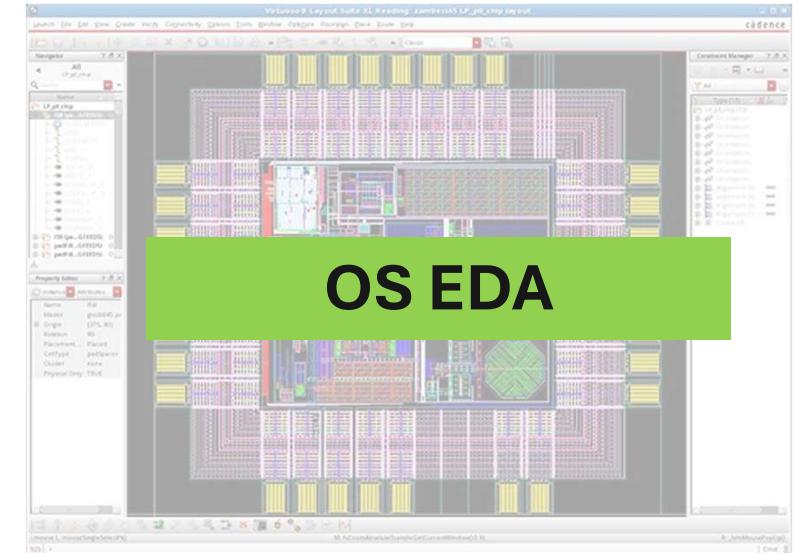
Open-source EDA tools and PDKs

Introduction

Why Open-Source IC design?



[Tim Ansell, FOSSi Dial-Up2020]

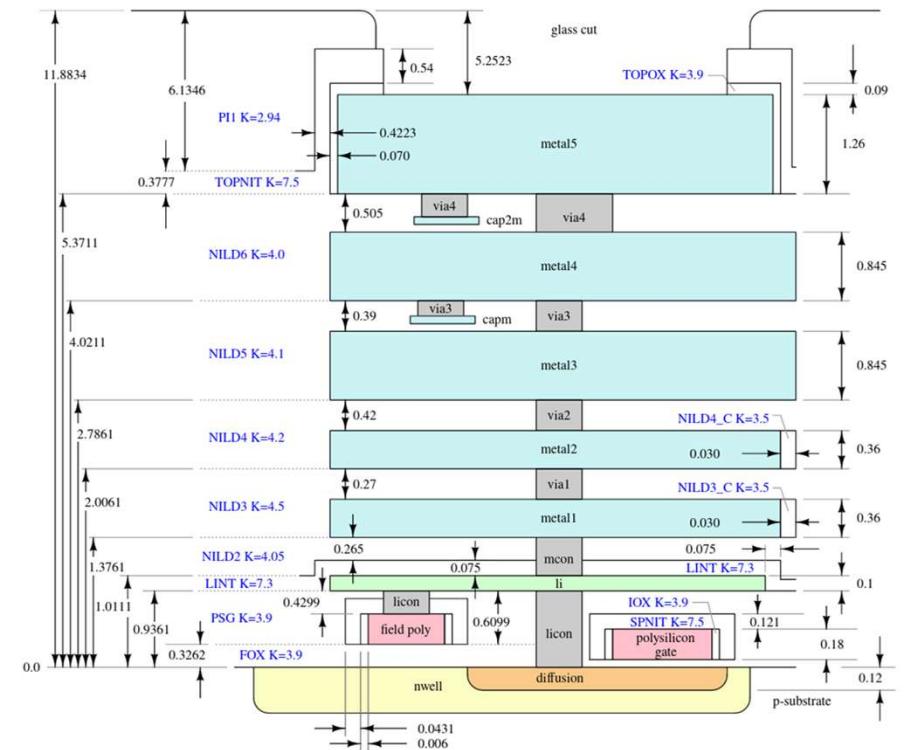
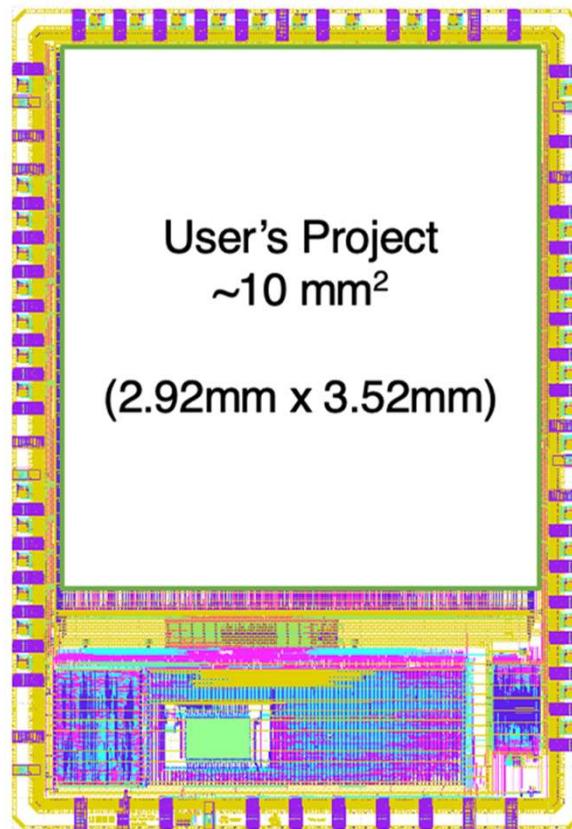


Open-Source Silicon Approach

The OS approach: OS PDKs

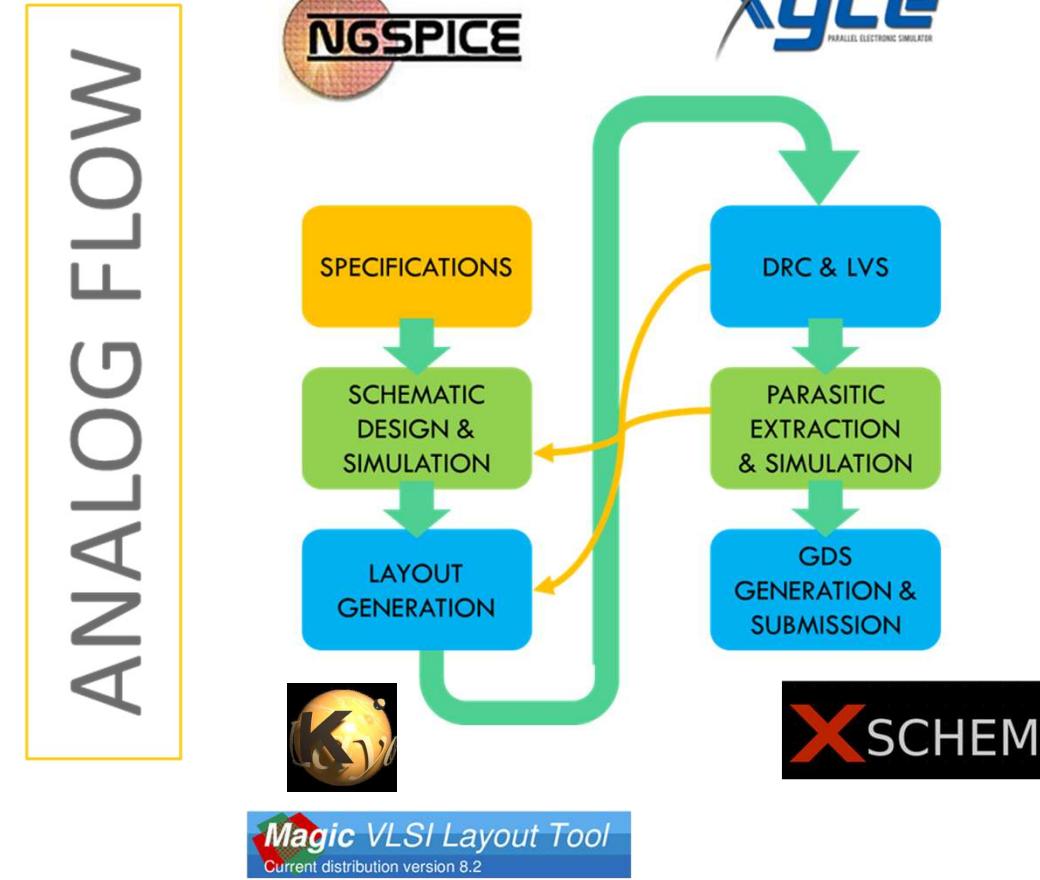
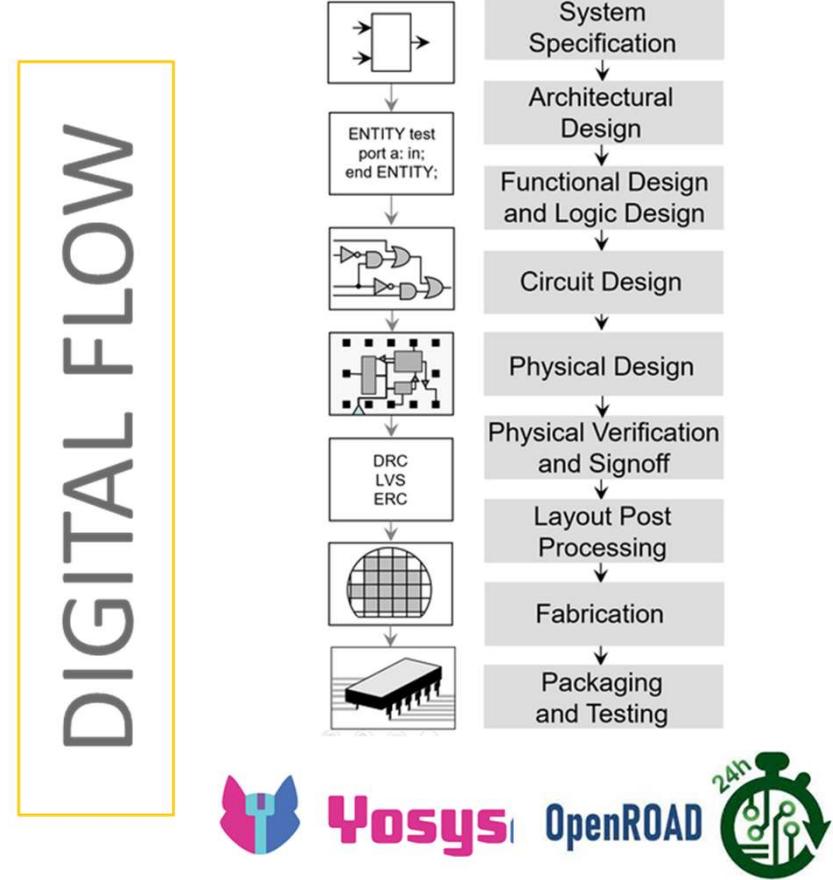


Caravel/ Caravan chip harness



Open-Source Silicon Approach

The OS approach: OS EDA/CAD software



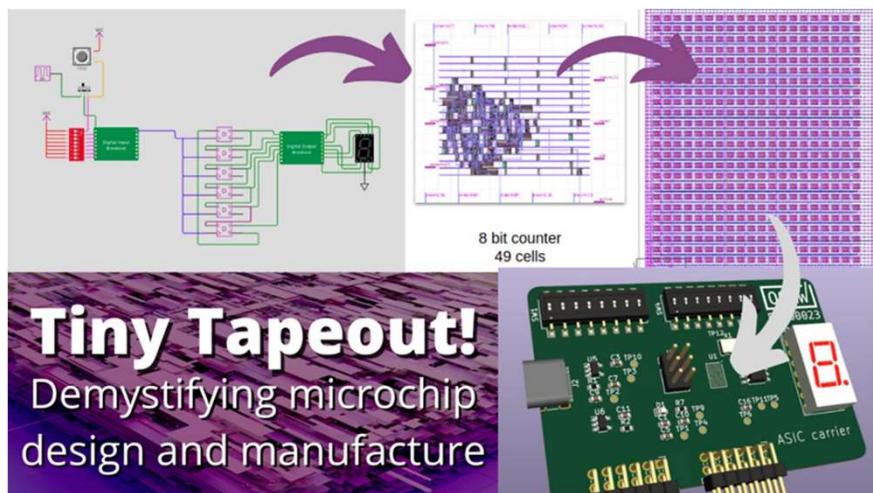
Open-Source Silicon Approach

The OS approach: OS EDA/CAD Docker toolkit

- JKU's IIC-OSIC-TOOLS → <https://github.com/iic-jku/IIC-OSIC-TOOLS>
 - Widely used Docker by JKU's IIC team (Harald Pretl & co)
 - Includes MANY OS tolos for IC design
- UNIC-CASS's uniccass-icdesign-tools → <https://github.com/uniccass/uniccass-icdesign-tools>
 - Supported version of <https://github.com/ChipUSM/usm-vlsi-tools> (kudos to Aquiles Viza)
 - **Lightweight, tapeout-oriented toolkit, verified with IHP openruns**

Open-Source Silicon Approach

The OS approach: low-cost MPWs



Welcome to IHP-Open-DesignLib documentation!

IHP-Open-DesignLib is repository, which contains open source IC designs using IHP SG13G2 BiCMOS processs. It is also a central point for design fabrication under the concept of IHP Free MPW runs funded by a public German project [FMD-QNC \(16ME083\)](#). Project funds can be used exclusively to produce chip designs for non-commercial activities, such as university education, research projects, and others. In the project, a continuation for the provision of free area for the open source community is to be worked out.

11 Nov 2024	22 Nov 2024	07 Apr 2025	09 May 2025	18 Jul 2025	15 Sep 2025
SG13CMOS 220	SG13G2 20	SG13G2 140	SG13G2 30	SG13G2 30	SG13CMOS 220



ChipCreate

Chip Design, Fabrication and Bring-up for Product Companies, Startups and university programs

\$14,950 per tapeout

The ChipCreate offering includes:

- Pre-built SoC design with RISC-V subsystem and peripherals
- Up to 15mm² of die space with a standard I/O ring
- 38 fully -configurable I/Os supporting both digital and analog signaling
- Option of 100 QFN-packaged parts or Bare Die
- Plug and play development board with software support
- Complete RTL-to-GDSII Open Source design flow



GF180MCU Shuttle Slot Bare Dies

\$ 7,000 USD

GF180MCU Process

~20mm² silicon

3.88mm x 5.07mm die size

1,000 raw dies

Open-Source Silicon Approach

The OS approach: community

The screenshot shows a web-based chat interface from Element, a Matrix client. The URL in the address bar is <https://element.fossi-chat.org/#/room/#ihp-sg13g2:fossi-chat.org>. The interface has a sidebar on the left listing various rooms: Inicio (780 unread messages), librelane (100), sky130 (87), magic (117), digital-design (8), xschem (65), ihp-sg13g2 (selected), cace (9), analog-design (22), and general (74). The main area shows a message from Roel Jordans: "hi all, I'm playing around with the IHP PDK in the iic-osic-tools docker but am having some issues when I try to simulate with Xyce. ngspice worked out of the box but I tried running the example...". Below it, navalhermawan replies: "Sorry for replying to an old question but I'm trying to run xyce using qucs-s and got the exact same error as this, but couldn't find the simulate with Xyce button on qucs-s. Seems like there's only one button for simulation and this drop down to change the simulation type. Is that button on xscheme?". A reply from Roel Jordans follows: "Xyce also needs some plugins loaded, could be that ...". The footer of the interface includes a message input field "Enviar un mensaje..." and various status icons.

<https://element.fossi-chat.org>

Open-Source Silicon Approach

The OS approach: community

- JKU’s “Analog Circuit Design course” → <https://github.com/iic-jku/analog-circuit-design>
 - Fully-open content for intermediate-level MOSFET circuit design course
 - Based on Xschem and Ngspice examples + IHP technology
 - Uses JKU’s IIC-OSIC-TOOLS Docker
- University of Hawai’i’s “Analysis and Design of Integrated Circuits” tapeout course → <https://github.com/bmurmann/EE628>
 - Open content for lectures and assignments
 - Design of a Sigma-delta converter using OS design flow + IHP technology

Open-Source Silicon Approach

The OS approach: community

- A growing number of other resources:
 - Carsten Wulff's course:
https://youtube.com/playlist?list=PLybHXZ9FyEhb9-A3QR1NRlt6VxeTXYr5&si=31ccv4rhnWps0_Ci
 - Tiny tapeout: <https://tinytapeout.com/specs/analog/>
 - IHP Analog Academy: <https://github.com/IHP-GmbH/IHP-AnalogAcademy>

Open-Source Silicon Approach

The OS approach: OS IP

- Analog IP components and specifications in Sky130A for Efabless next-generation Caravel (Chipalooza):

<https://docs.google.com/spreadsheets/d/132YkMiYaM0iHML5feT1yWLQIvP-pCM0ICArM9f1LxhM/edit?gid=0#gid=0>

The screenshot shows a Google Sheets spreadsheet with the following data:

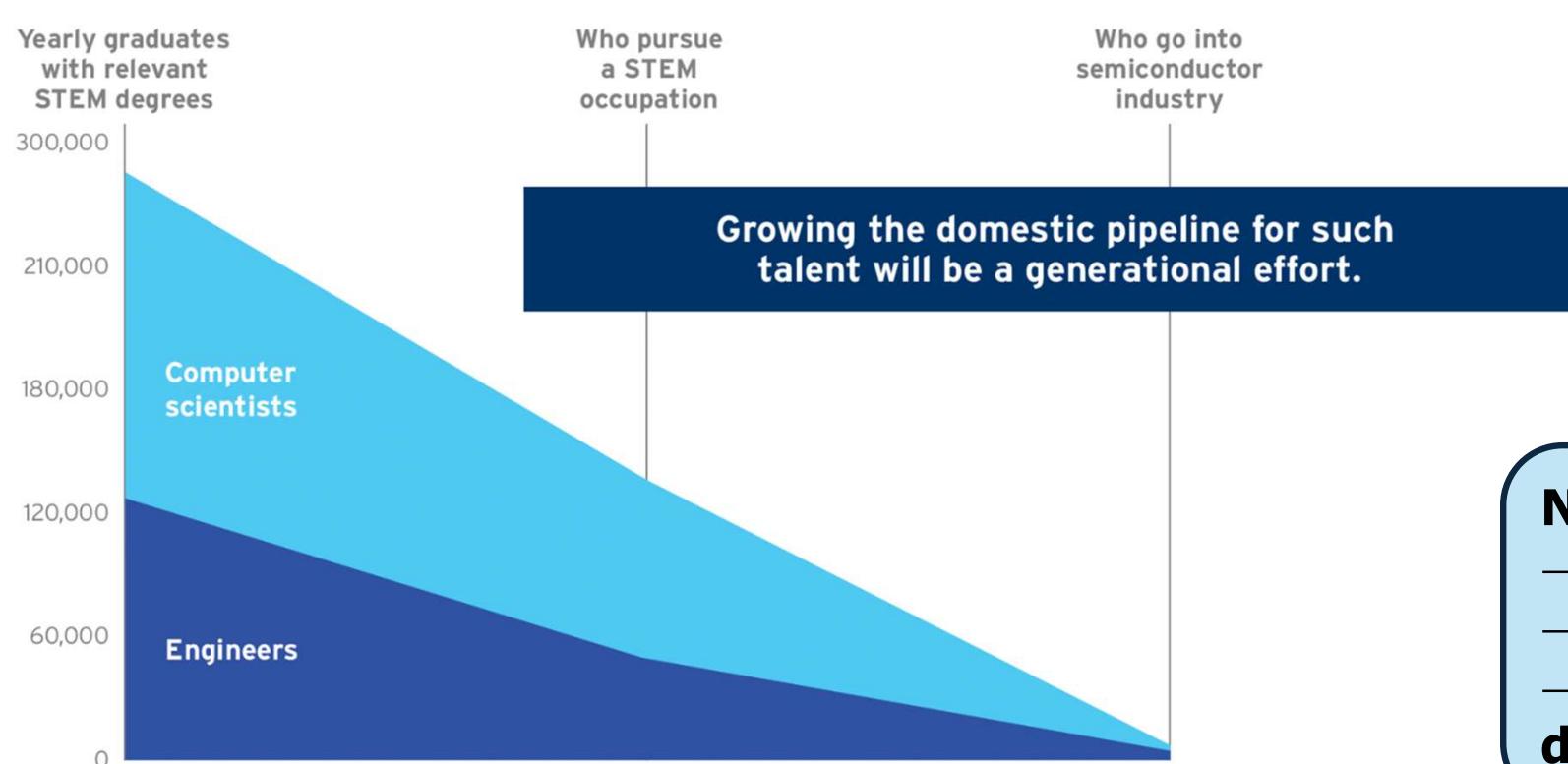
IP block	Rank Criticality	Required for ML SoC	URL of Chipalooza challenge submission(s)
			D
Ultra low-power comparator	2	✓	https://github.com/JYSquare2/sky130_icrg_ip_ulpcomp https://github.com/3x10e8/sky130_rhythmic_ip_dynamic_comparator
Comparator	2	✓	https://github.com/Create5517/sky130_pmc_ip_cmp.git
1.8V Precision bandgap	3	✓	https://github.com/adankvitsch/sky130_ak_ip_cmos_vref
Low-power 1.8V LDO	3	✓	https://github.com/dcdc10893/sky130_deser_ip_lowpowerLDO https://github.com/AlexMenu/sky130_am_ip_Ido_01v8
Current reference bias generator	2	✓	https://github.com/tatzelbrunn/sky130_cm_ip_biasgen
16-bit capacitive DAC	1	✓	
12-bit resistive DAC	2	✓	

- IHP opensource designs (per tapeout), e.g.:

https://github.com/IHP-GmbH/TO_Nov2024

Open-Source Silicon Approach

Lower barriers for new designers



USA career choice
CS → 830.000
EE → 70.000

New skills in designers:
→ Analog + digital background
→ AI/ML knowledge
→ Programmatic/systematic design skills

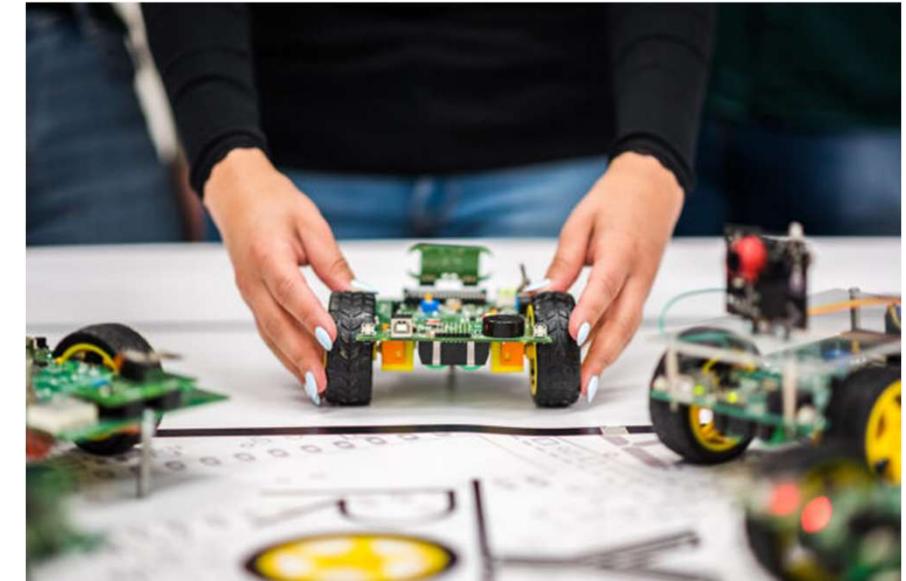
Source: <https://www.semiconductors.org/chipping-away-assessing-and-addressing-the-labor-market-gap-facing-the-u-s-semiconductor-industry/>

Open-Source Silicon Approach

Lower barriers for new designers



Makers' philosophy: do it yourself



**The IC design workflow
is conservative
→ need for openness and
collaboration!**



Open-Source Silicon Approach

Industrial initiatives for OS silicon education



SUMMERSCHOOL 2023
18-22 SEPTEMBER

AnaGen

Next level
chip design!



Certificate Course: Analog Design with IHP SG13G2
Open-Source PDK

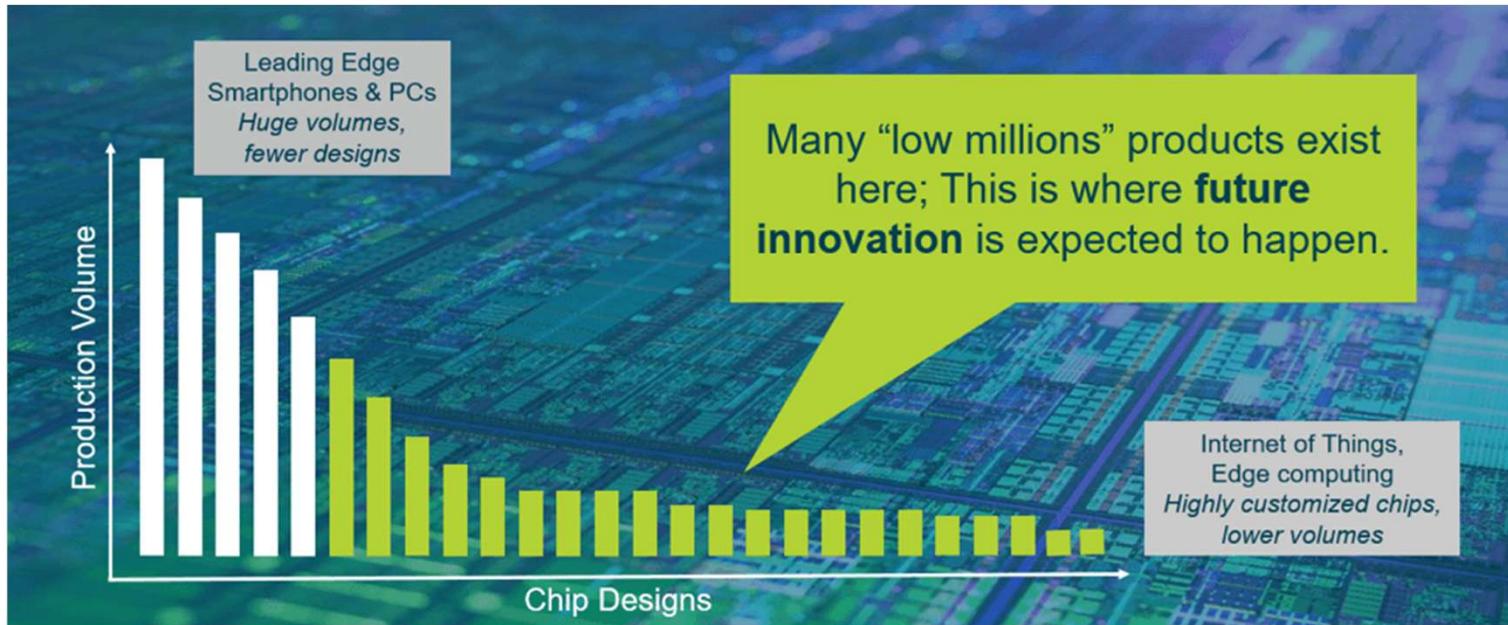
cadence®

Cadence and SkyWater: Fostering
the Next Generation of Innovators

Open-Source Silicon Approach

Industry: why to care about opensource?

- Some pioneer companies are starting to build their business models around open source silicon movement
- Mostly focused on education, OS EDA and enabling chip design for low-volume projects
- But some of them are already working on design (Mabrain, Spherical), and soon more will come



Source: <https://www.skywatertechnology.com/sky130-open-source-pdk/>



Zero to ASIC



Tiny Tapeout



Mabrain



Open-Source Silicon Approach

Research & education using AMS OS tools

- Traditional IC design flows are not designed for educational/academic purposes
 - The wide variety of tools and workflows can be overwhelming for beginners
 - High costs and restricted PDK availability limit accessibility
 - Limited documentation and minimal community-driven collaboration hinder learning
- Tapeout courses require significant budgets, making them inaccessible to many universities and regions
- IC design environments have traditionally been restrictive
 - Strict NDAs restrict access to essential resources
 - Information sharing is trust-based and highly limited
 - However, this landscape is rapidly evolving, opening new opportunities for education

Open-Source Silicon Approach

“Potential of OS Design for AMS IC Education” Forum @ CICC 2025

Harald Pretl, Johannes Kepler University, Austria



Bio: Harald Pretl received the Dr. techn. Degree from the Johannes Kepler University in Linz, Austria, in 2001. From 2000 to 2022, he developed cellular RF transceivers at Infineon, Intel, and Apple. Since 2015, he is a full professor, heading the Institute for Integrated Circuits (IIC) at JKU.

Title: Using Open-Source EDA Tools in Hands-On IC Design Education

Abstract: Our group maintains a collection of open-source IC EDA tools (<https://github.com/iic-jku/IIC-OSIC-TOOLS>), available pre-integrated as a virtual machine image, for analog, mixed-signal, and digital design using the available open-source PDKs. We are using this tool collection, hosted on a browser-accessible server, to teach an undergraduate digital design course (using Tiny Tapeout for IC fabrication) and a graduate analog design course, freely available at <https://iic-jku.github.io/analog-circuit-design>. In this talk, we will detail our approach and talk about our experience using open-source tools.

Jaeduk Han, Hanyang University, South Korea



Bio: Jaeduk Han is an Assistant Professor of Electronic Engineering at Hanyang University. He earned his B.S. and M.S. from Seoul National University and Ph.D. from UC Berkeley. With experience at TLI, Intel, Xilinx, Apple, and SK Hynix, his research focuses on high-speed analog and mixed-signal circuit design and automation.

Title: Custom Circuit Layout Generation Technologies for Open Source IC Design and Education

Abstract: The increasing complexity of circuit design at advanced semiconductor nodes, coupled with limited academic access to cutting-edge processes, poses challenges in training skilled engineers. This talk explores automating layout design using open-source PDKs and software tools, focusing on teaching these methods to undergraduate and graduate students. Experiences in adapting these techniques to advanced processes for developing industry-ready talent will also be shared.

Elles Raaijmakers, Eindhoven University of Technology, Netherlands

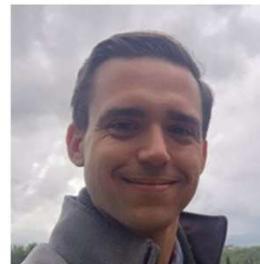


Bio: Elles Raaijmakers obtained her master degree in electrical engineering from Eindhoven University of Technology in 2015. Elles performed her PhD (2023) part-time at the University of Amsterdam. Additionally, she worked as an illustrator for the faculty and university magazines. To inform the general public, Elles has published a comic book of her collected research results.

Title: IC tycoon

Abstract: Chip designers are in high demand. In contrast with the ever-growing need of new engineers, there is a growing skepticism regarding science among a portion of the general public. We seek the answer through enabling people to experience chip design themselves. We use the open-source PDKs to enable interested laymen to design their own chip, which we will produce and measure for them. And for a younger audience, we are working on a game about IC design.

Dan Fritchman, Stealth Mode Startup, USA



Bio: Dan Fritchman serves as the CEO of San Francisco, CA based Generation Alpha Transistor, a provider of AI-based IC design tools. He holds a PhD in Electrical Engineering & Computer Sciences from the University of California, Berkeley, MS from Santa Clara University, and BS from Duke University.

Title: Lessons From Where Open Source Has (And Hasn't) Worked

Abstract: Open-source distribution has transformed the software industry – or at least parts of it. This talk examines where its impacts have been greatest and most muted, and offers a roadmap for open-source IC design by way of analogy. We feature the design suites principally authored at UC Berkeley for both digital and analog IC design as primary examples.

Tim Edwards, Efabless Corporation, USA



Bio: Tim Edwards is SVP Analog and Design at Efabless Corporation, where he has worked since 2014. He is a well-known advocate of open source silicon, and is the developer and maintainer of multiple open source software tools for EDA, including magic, netgen, and open_pdk. He was one of the principle developers of the sky130 and gf180MCU open PDKs, has helped develop the IHP sg13g2 open PDK, and architected the Efabless Caravel harness chip.

Title: Efabless Frigate: Open source analog and mixed-signal harness

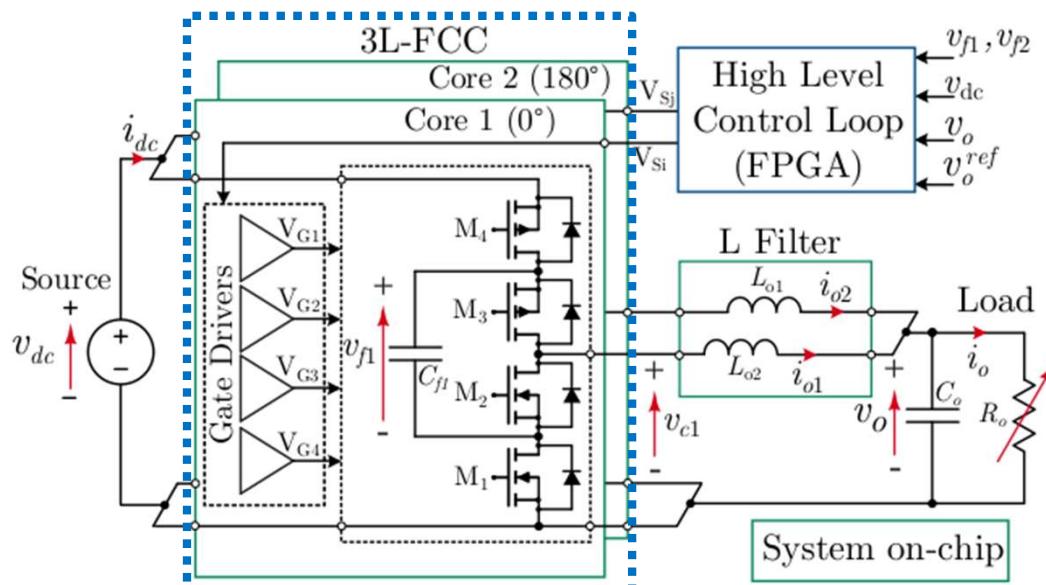
Abstract: The Efabless chipignite program and the Caravel “harness” chip design have enabled access to tools, PDKs, instruction, and community for small businesses, students, makers, bringing real silicon to anyone unable to afford the cost of traditional chip design and manufacture. The Efabless Frigate chip is the next generation of harness, including an improved RISC-V SoC and configurable analog and mixed-signal hardware components, all open source and developed in part by our community of users.

Silicon-verified research using OS
tools + PDKs (Analog-on-top)

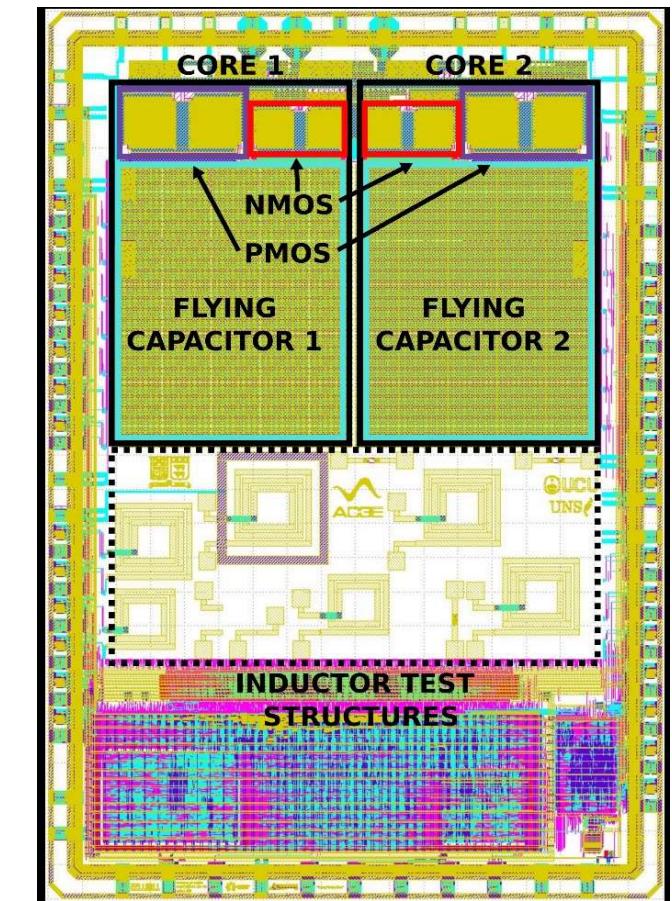
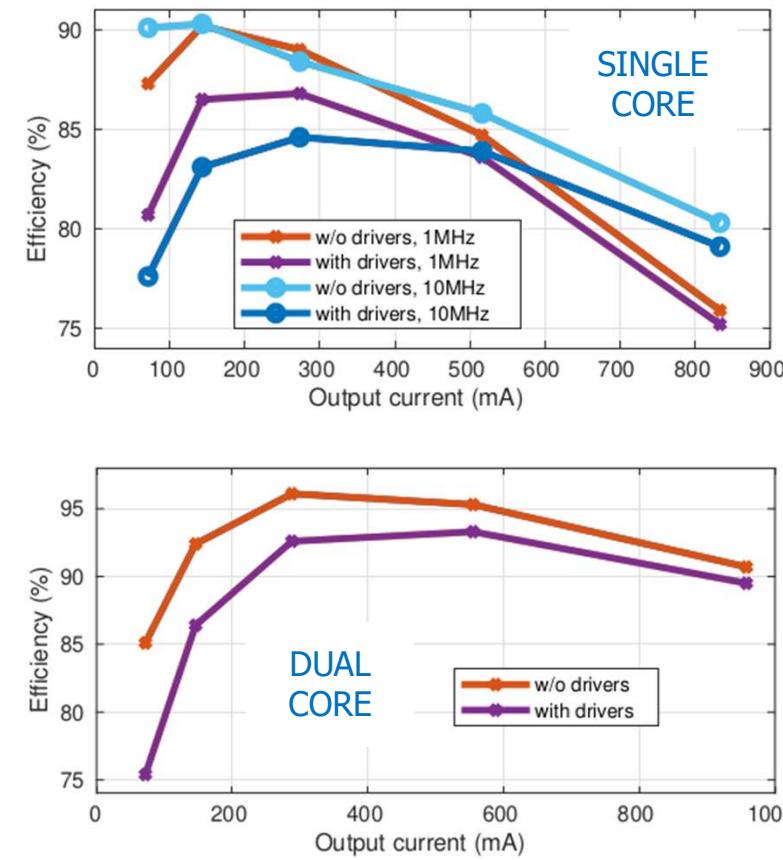
Previous research: OSIC design and testing using SKY130

3-level flying capacitor DC-DC converter

- Simulations: Efficiency analysis under different conditions
- Implementation: Modular approach → testable subcircuits
- Tapeout: December 2022 → chip delivery: November 2023



ON CHIP BLOCKS

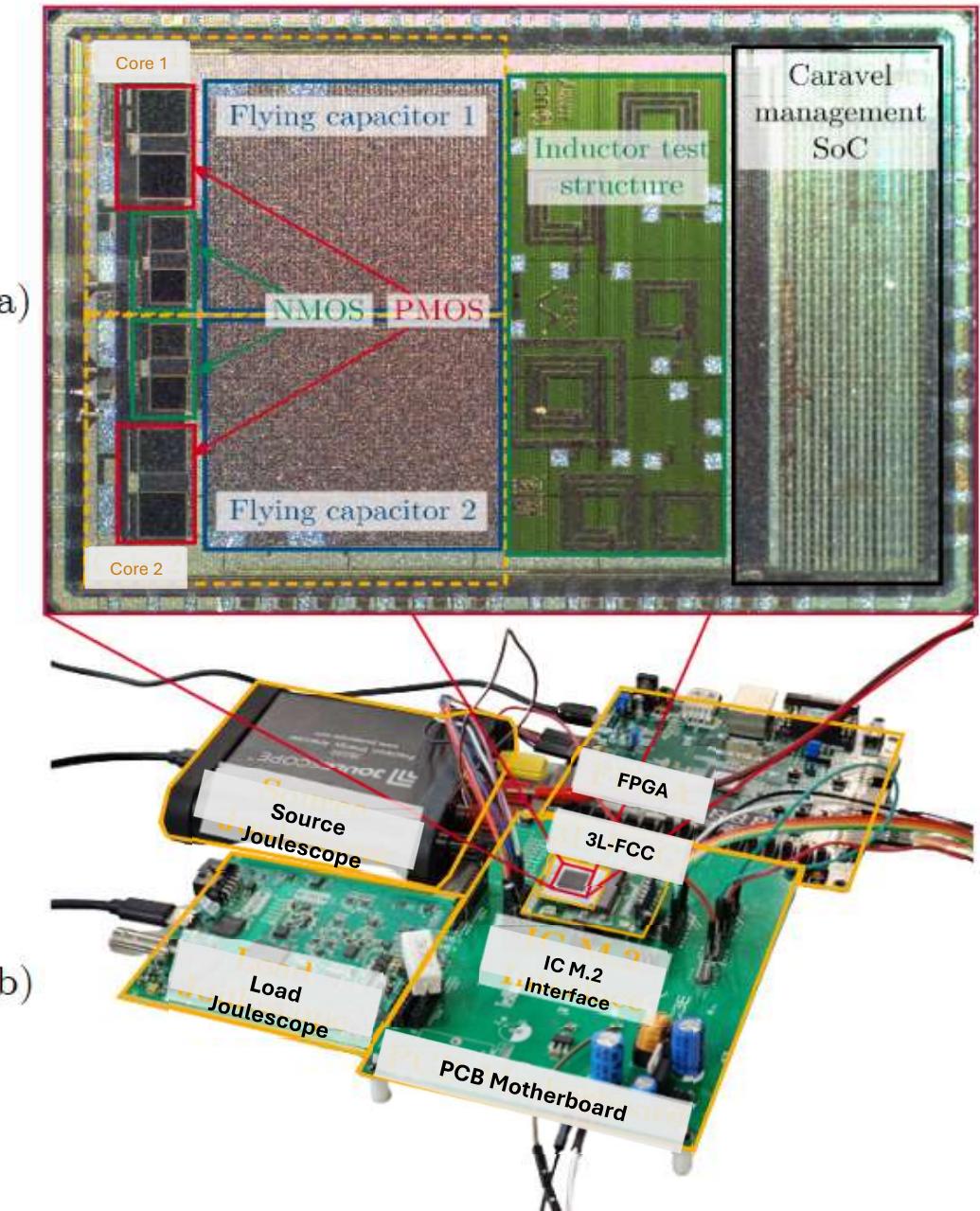


[MARIN, CAE2023]

Previous research: OSIC design and testing using SKY130

Test setup

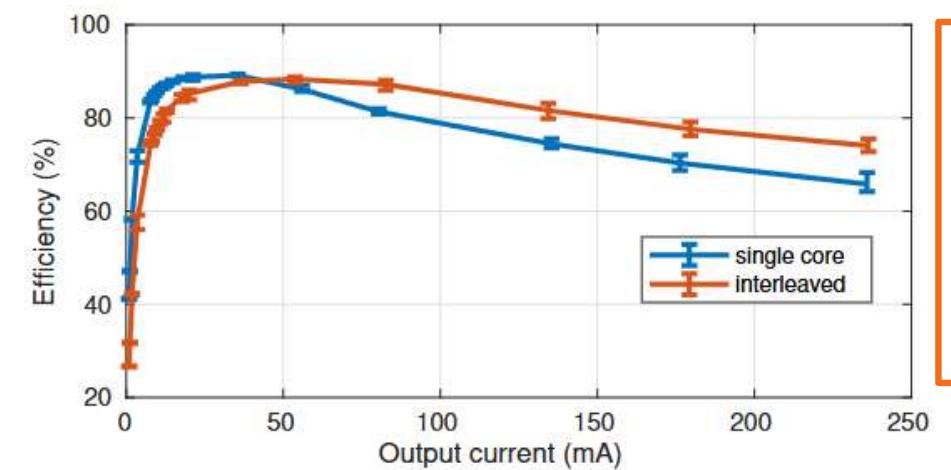
- QFN packages soldered to M2 boards
- Adaptation board for the M2 boards
- Open loop control
 - DC-DC modulator was implemented using a Nexys A7 FPGA
 - 16ns minimum dead time
- Efficiency as main figure of merit for now
 - Internal vs external flying caps
 - Joulescopes
- Other generic equipment: oscilloscope, active probes, power supplies



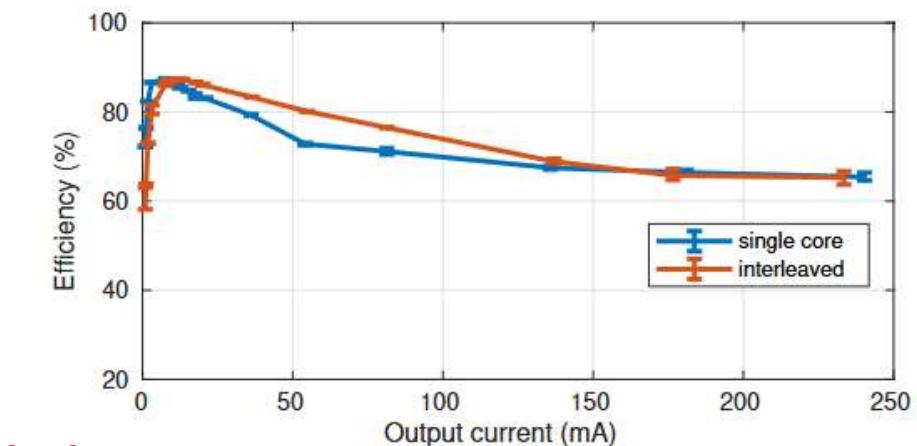
Previous research: OSIC design and testing using SKY130

Preliminary efficiency measurement results of 3 samples

- 3 samples were fully characterized
 - moderate measurement error
- Internal FC:
 - 89,3% for 21 mA, 1 core
 - 88,9% for 37 mA, 2 cores
- External FC:
 - 87.5% for 8 mA , 1 core
 - 87.4% for 12 mA , 2 cores



(a)



(b)

Internal FC

External FC

Previous research: OSIC design and testing using SKY130

Code-a-chip automated power IC specs-to-GDS flow

[Rutenbar, 2010]

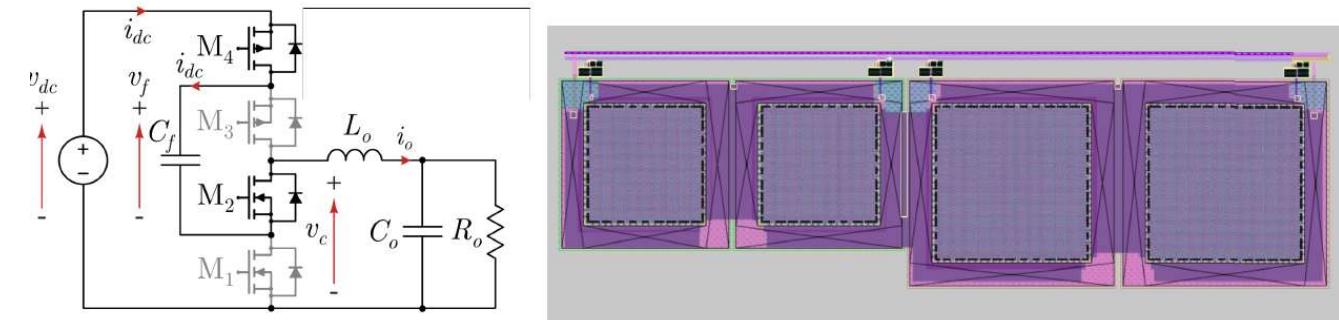
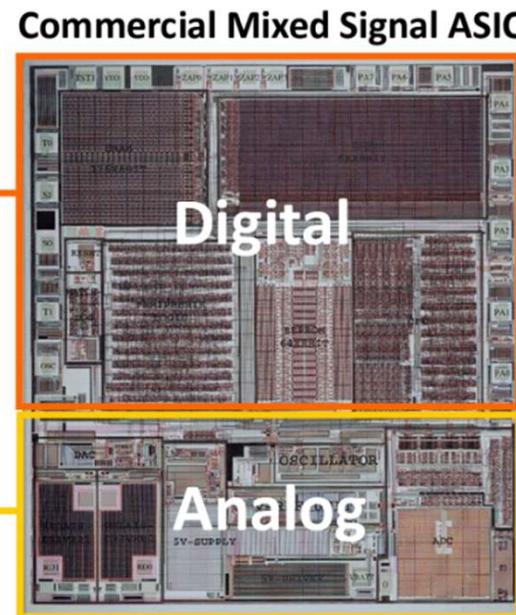
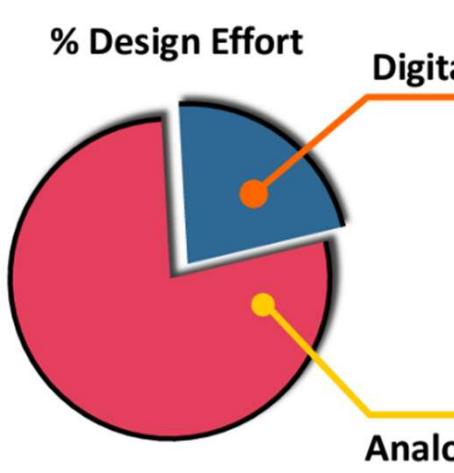
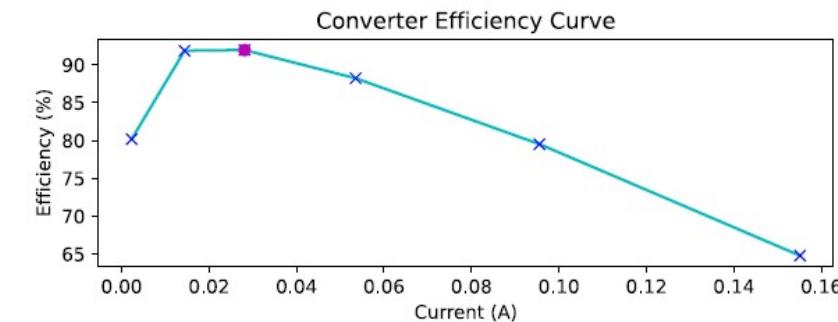


Figure 3: 3LFC Converter schematic (left) and layout (right)



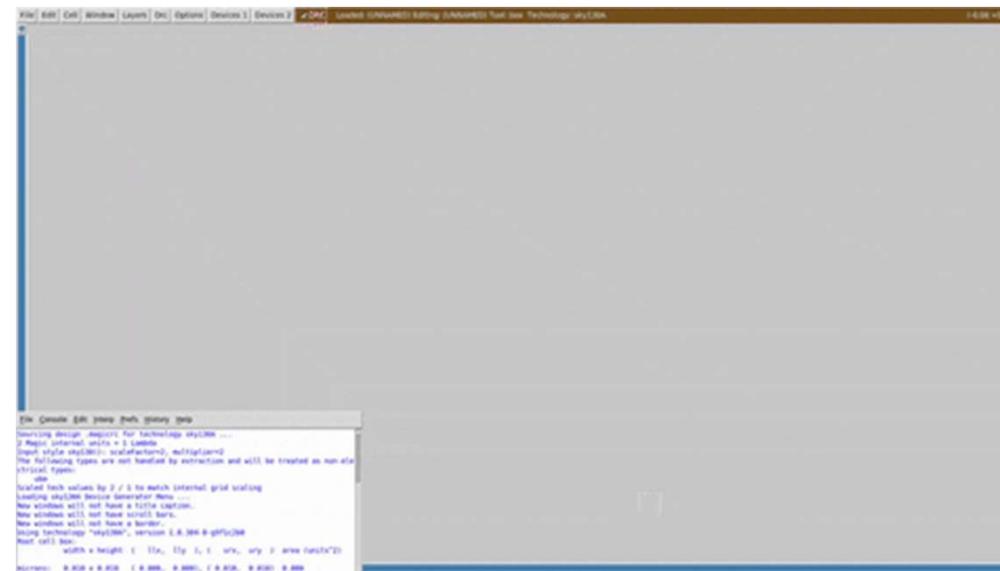
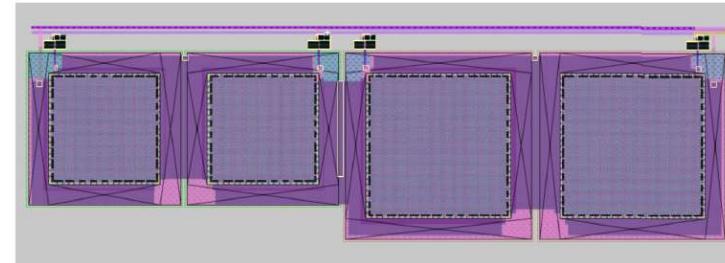
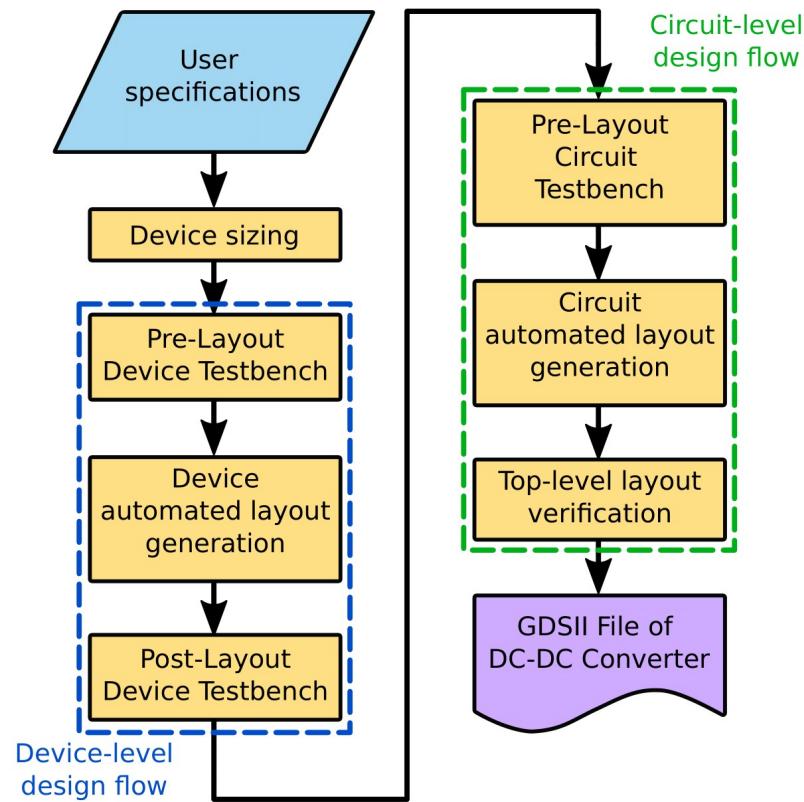
Automated design
and evaluation?

Previous research: OSIC design and testing using SKY130

Code-a-chip automated power IC specs-to-GDS flow

- Full Python-based automated flow using opensource toolkit
 - From current, voltage, area and frequency specs to manufacturable layout (GDS file)
 - Presented at VLSI Symp. Kyoto 2023

[OSORIO, CAE 2025]



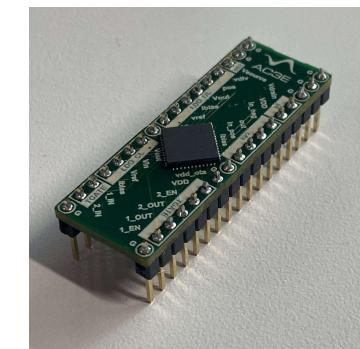
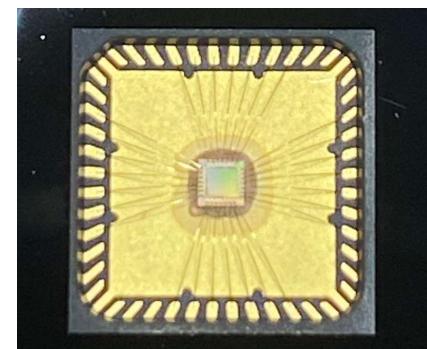
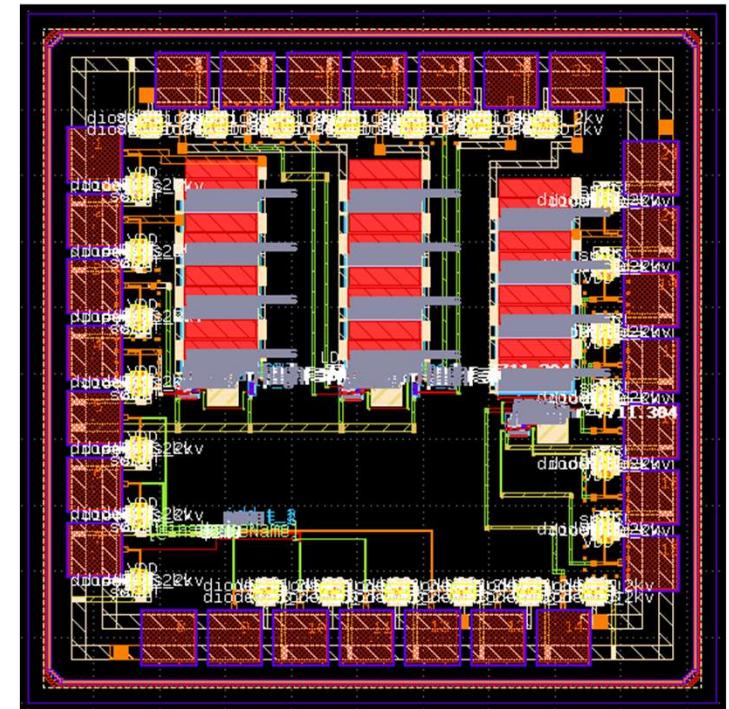
Chip example #1: full analog

Automated Analog LDO in IHP 130nm CMOS

- Scripted generation of pad ring (custom pad cells)
- Manual placement and routing of:
 - 2 LDOs (open and closed loop)
 - Miller OTA
 - Pass transistor
- Currently under lab testing



Daniel Arévalos
(MsC thesis)

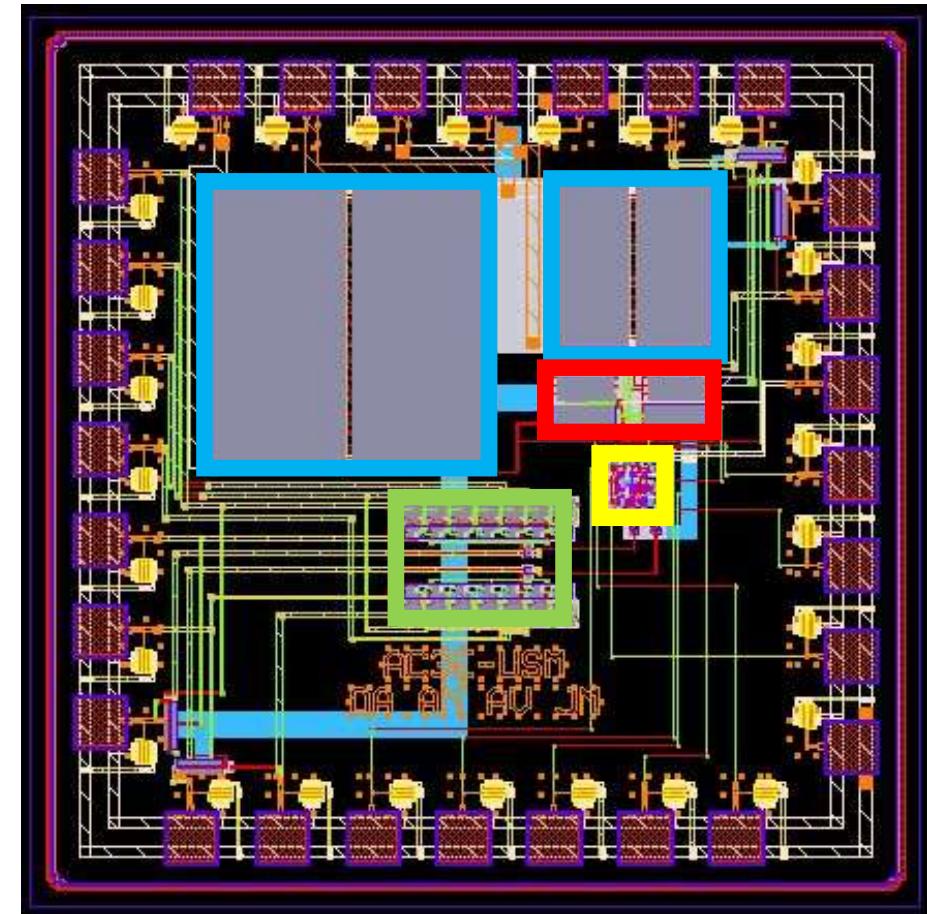


D. Arévalos, et al. “A Topology-Independent and Scalable Methodology for Automated LDO Design Using Open PDKs”, *Electronics* 2025

Chip example #2: mostly analog + digital blocks

Time-based-controlled DC-DC buck converter in IHP 130nm CMOS

- Chip area: 1.4mmx1.4mm (2mm²)
- Building blocks
 - PMOS and NMOS power devices
 - Gate drivers
 - Digital block (phase detector + non-overlap circuit)
 - VCOs
- Layout methodologies
 - Analog blocks: exploration of Glayout + manual design
 - Digital block: use of SCH2GDS Flow
- Chips to be delivered soon

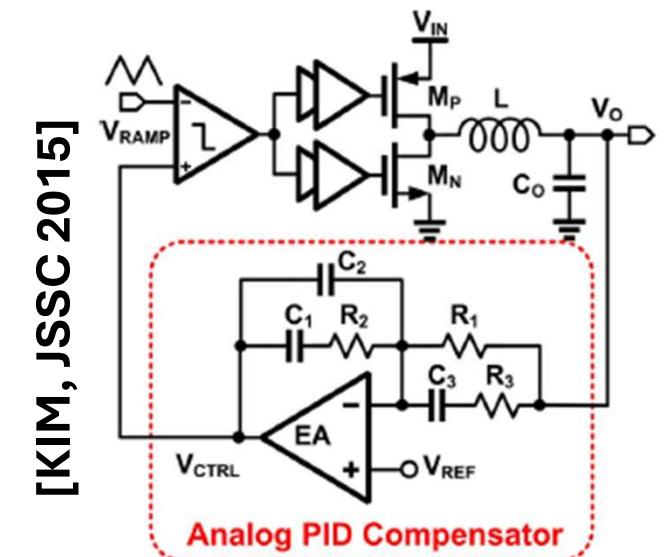


J. Marin, et al. “Systematic Design of a PVT-Robust CMOS Time-Based-Controlled DC-DC Converter Using Open-Source Tools”, NORCAS 2025

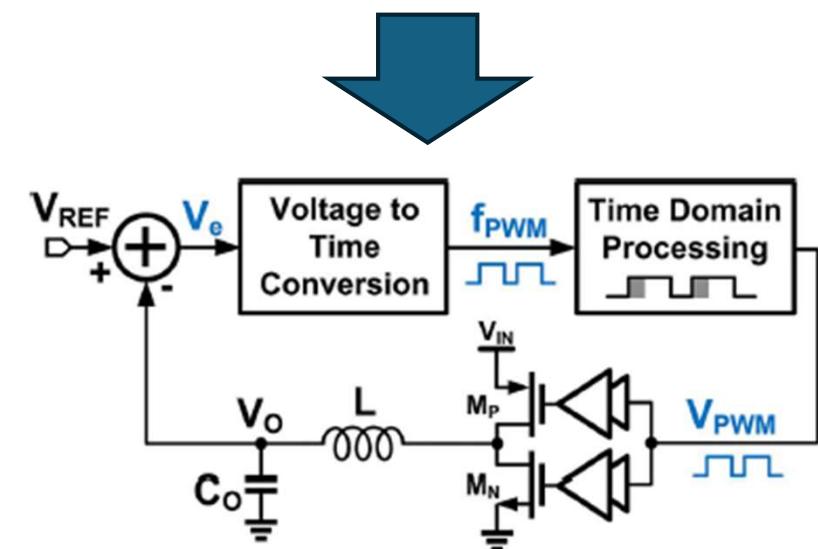
Chip example #2: mostly analog + digital blocks

Time-based-controlled DC-DC buck converter in IHP 130nm CMOS

- Research: time-based (TB) control
 - eliminates the pulse-width modulator and the error-amplifier employed in conventional controllers → compatible with new technology nodes
 - fast transient response and less control loop latency
 - reduced area and quiescent power
- Teamwork: “Tiny IC design house” tapeout approach
 - 1 analog designer
 - 1 layout designer
 - 1 top designer
 - 1 project leader (and analog designer)



[KIM, JSSC 2015]



Chip example #2: mostly analog + digital blocks

Design team

- Preliminary design
(Aug-Sep 2024)
- Tapeout implementation
(Oct-Nov 2024)



Jorge Marin
Teamleader and
top circuit design



Andrés Martinez (MsC)
Modeling and circuit
design



Andrés Martinez (MsC)
Modeling and circuit
design



Andrea Núñez (BsC)
Modeling and circuit
design



Aquiles Viza (BsC)
Layout design



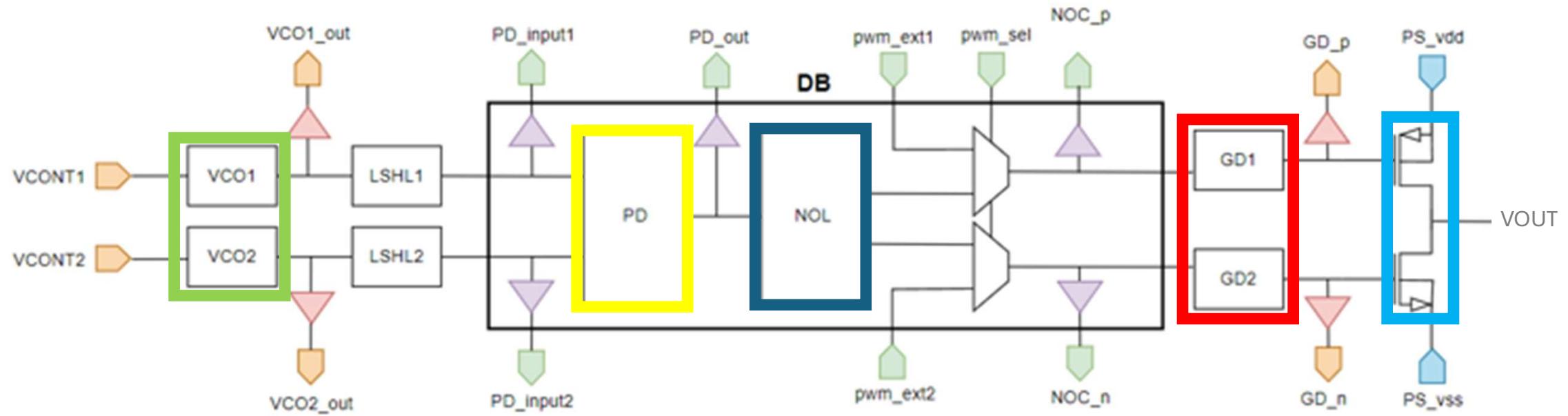
Felipe Torres (MsC)
Layout design



Daniel Arévalos (MsC)
Top design and
documentation

Chip example #2: mostly analog + digital blocks

Time-based-controlled DC-DC buck converter block diagram



Voltage-controlled oscillators

Phase detector

Non-overlap circuit

PMOS and NMOS power devices

Gate drivers

Testability and modularity:

→ isolated power domains

→ variable control parameters

→ multiple probing points

Chip example #3: highly digital

Mismatch characterization matrix



M. Montanares
(IHP)



K. Herman
(IHP)



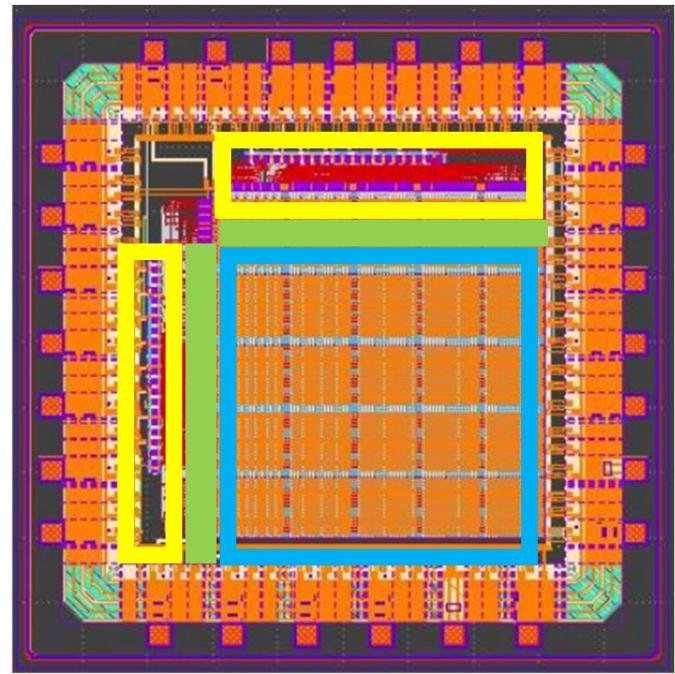
F. Quintana
(AC3E-USM)



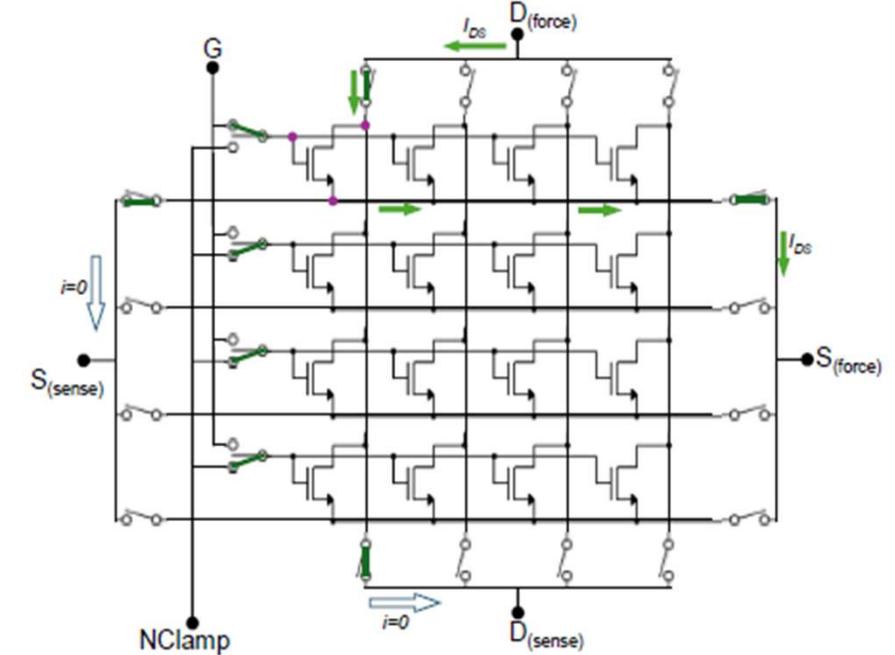
J. Marin
(AC3E-USM)



J. Brito
(CEITEC)

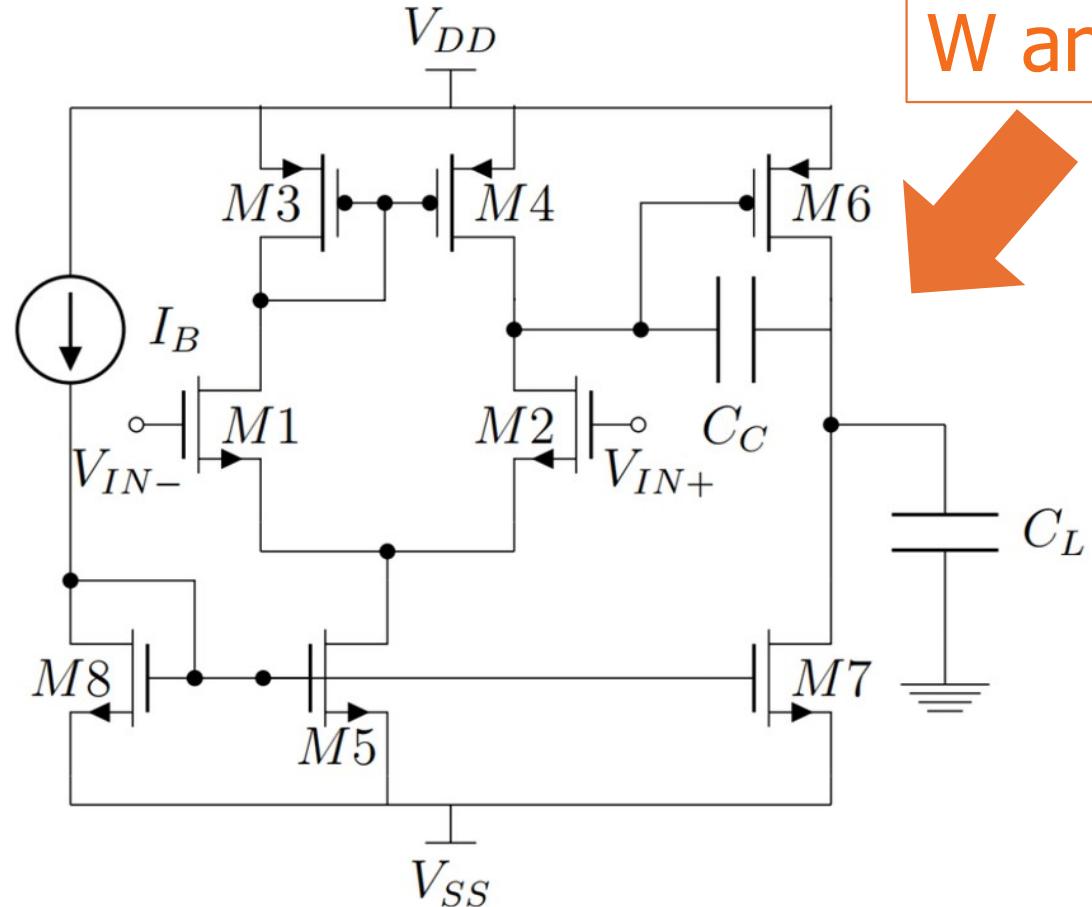


- Chip area: 0.7mmx0.7mm
- Building blocks
 - DUT matrix
 - Digital blocks (row/column decoders)
 - Transmission gates
- Layout methodologies
 - DUT matrix: Python scripting
 - Analog (Tgates): manual analog flow
 - Digital block: Librelane flow
- Sent for fabrication in the September 2025 free IHP shuttle

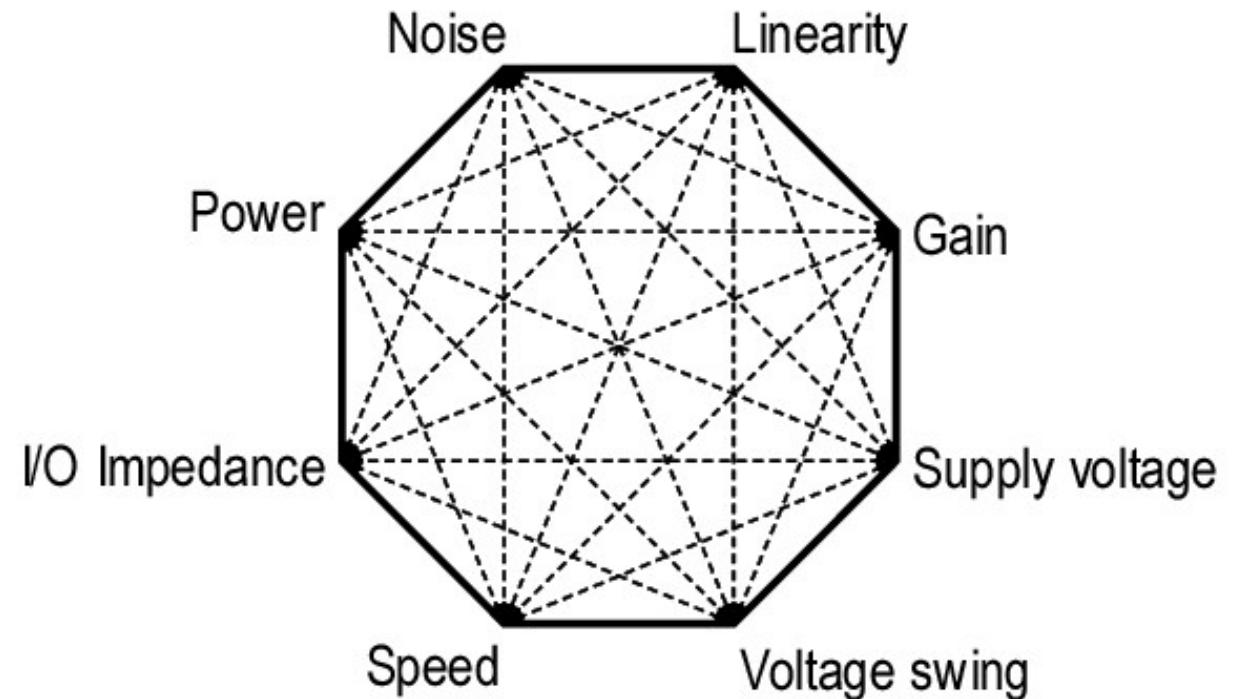


Simulation examples

Tradeoffs in analog design



W and L for each transistor M1 to M8?



Analog block example: Miller OTA

[B. Razavi]

Performance is limited by the tradeoff in target specifications

Schematic design and simulation

- Relevant tools
 - Xschem → schematic entry and netlist generation
 - Ngspice → simulation based on netlist generated by Xschem
- Visualization
 - Ngspice window → quick checks
 - GAW → integrated in Xschem
 - External viewer through raw data (e.g. Python script)

Simulation types

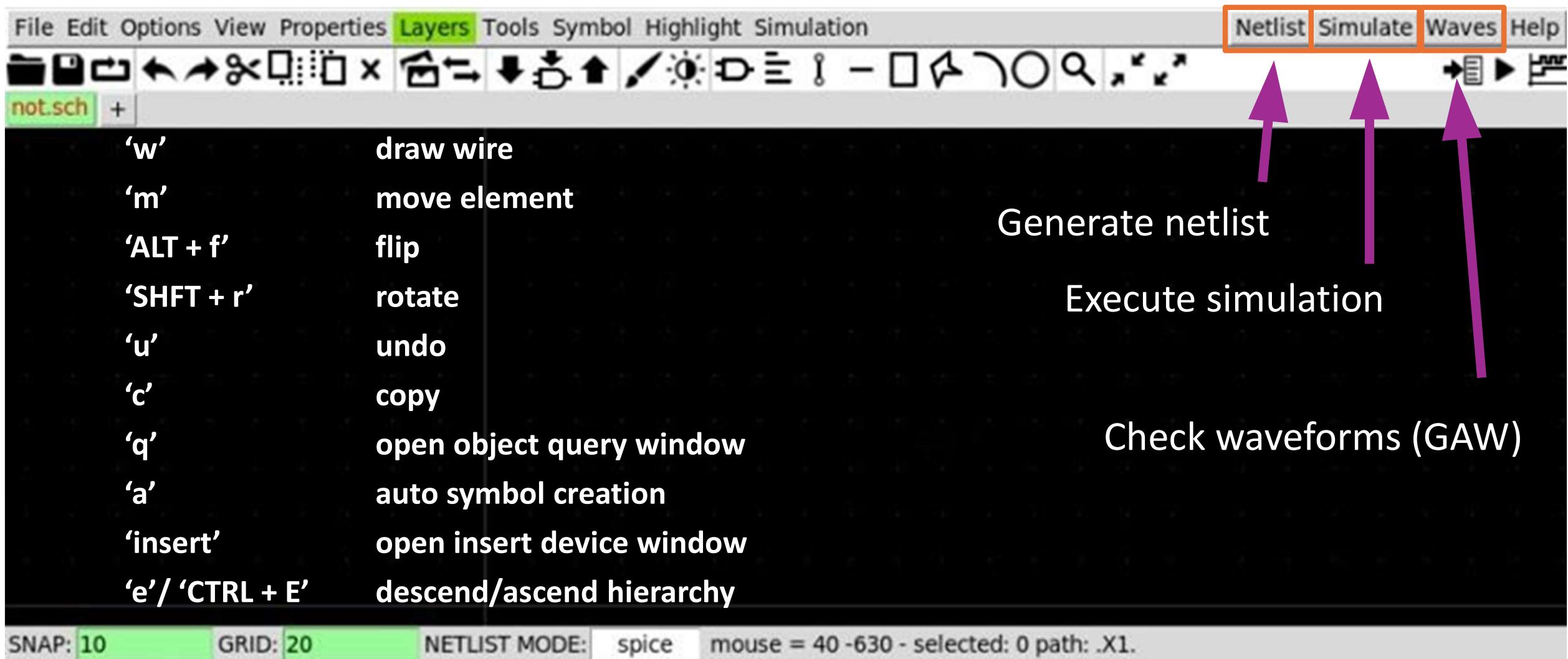
- DC → analysis of the circuit operating point
- Transient → time-domain behaviour
- AC → frequency sweep
- Noise → simulation of device intrinsic noise
- And others...

Ngspice manual will become your best friend!

<https://ngspice.sourceforge.io/docs/ngspice-manual.pdf>

Xschem GUI basics part 1

www.xschem.sourceforge.io



Simulation scope

- Nominal
 - Ideal simulation without considering many fabrication effects
- P(VT) corners
 - Considers global process variation (P) and environment (Voltage, temperature, T)
- Mismatch
 - Considers local statistical variation among devices
 - See examples in /opt/pdks/ihp-
sg13g2/libs.tech/xschem/sg13g2_tests/mc_*.sch
- Parasitic extraction/ post layout simulations
 - Components associated to extrinsic structures (metallization)

```
.lib cornerMOSlv.lib mos_tt  
.lib cornerRES.lib res_typ  
.lib cornerCAP.lib cap_typ
```

Clone Workshop repo

- INSIDE Docker → IHP 130nm is set by default
 - ls /opt/pdks/ → see installed PDKs
 - set_pdk [PDK-NAME]

```
designer ~
$ set_pdk ihp-sg13g2
PDK set to ihp-sg13g2
```

- OUTSIDE Docker:
 - cd [YOUR_INSTALL_FOLDER]\uniccass-icdesign-tools\shared_xserver\
 - git clone https://github.com/JorgeMarinN/OS_AnalogIC_UCLouvain_Oct2025

Example: Transmission gate RON

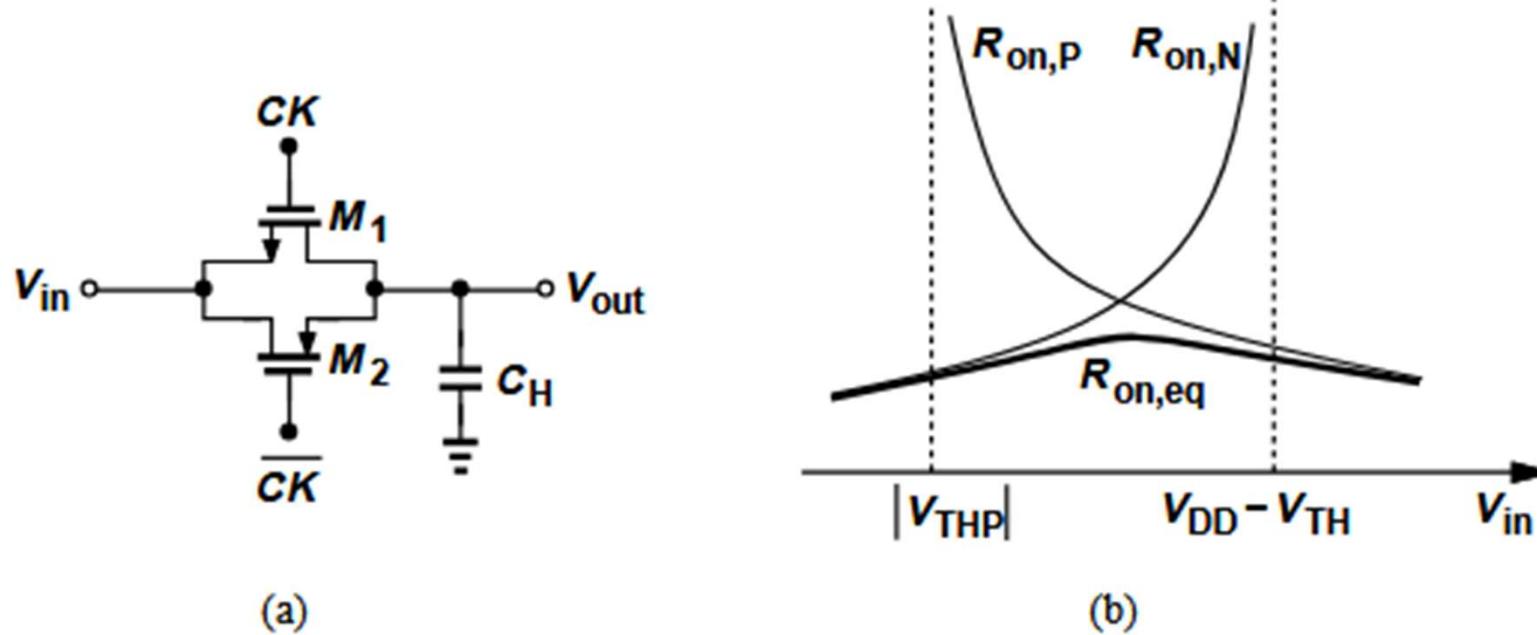
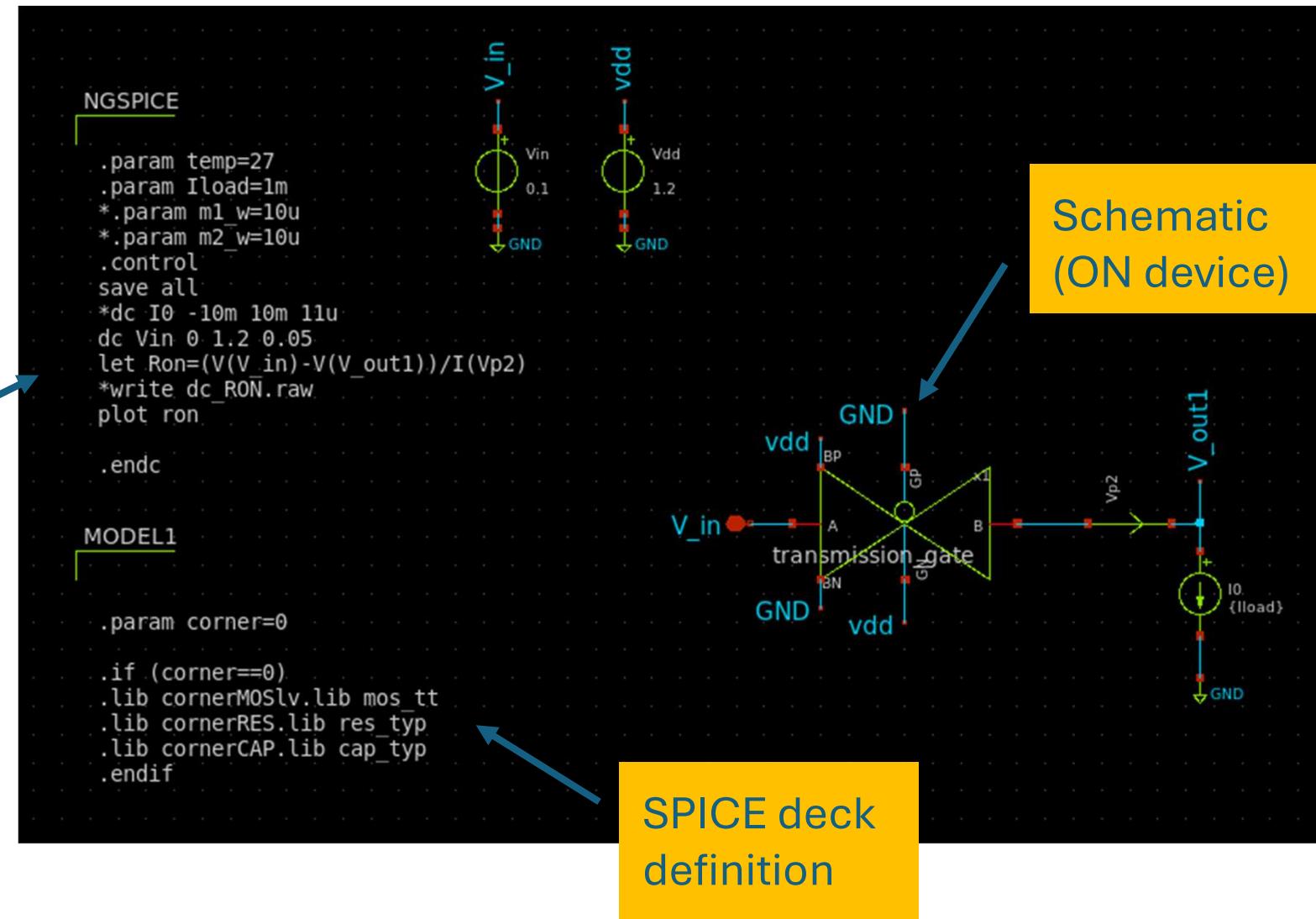


Figure 12.16. (a) Complementary switch, (b) on-resistance of the complementary switch.

Example: Transmission gate RON

- Github link:

→ https://github.com/JorgeMarinN/OS_AnalogIC_UCLouvain_Oct2025/blob/main/design_data/tb_tgate_RON.sch

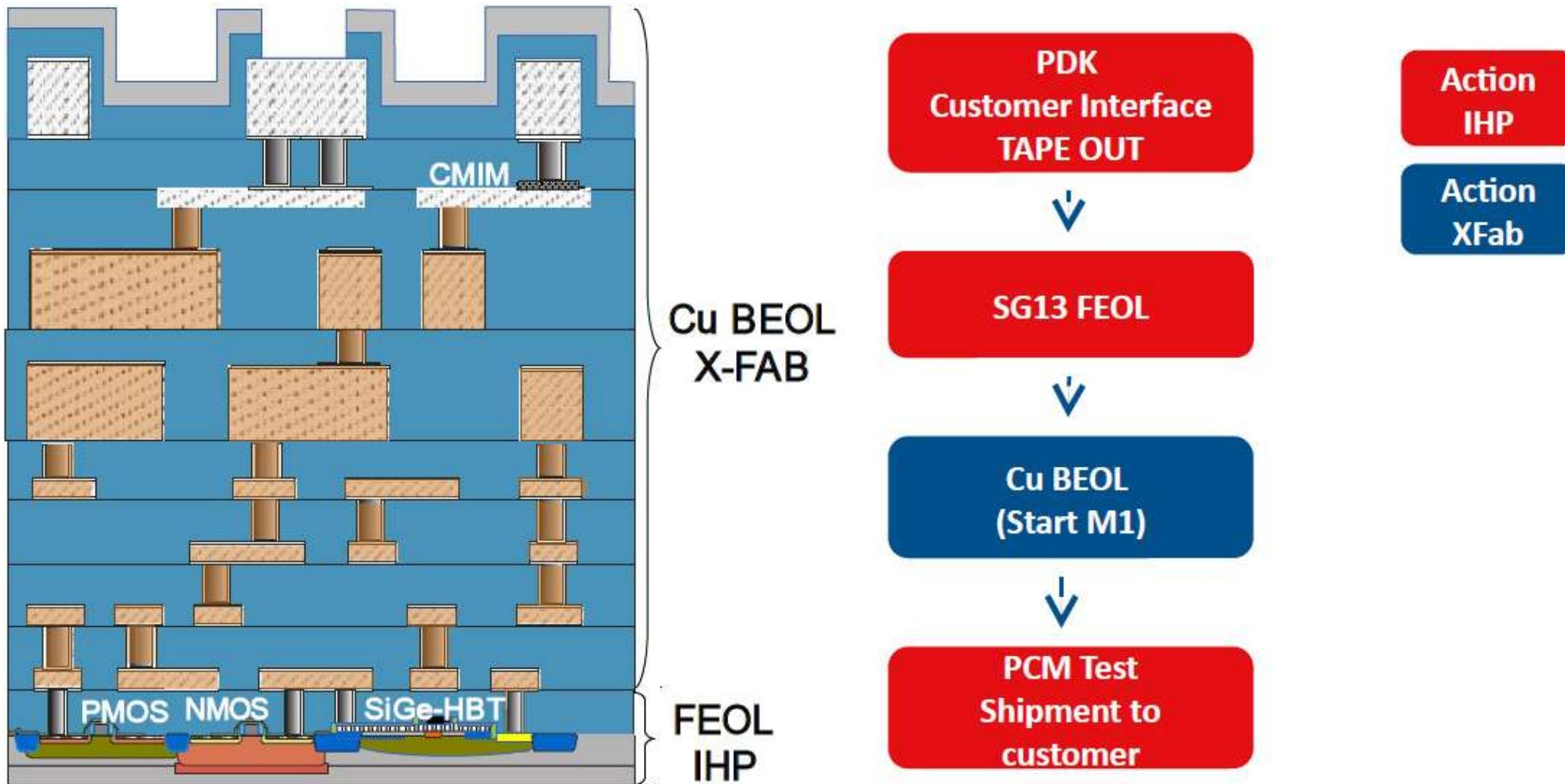


Task

- **SMALL FIX: cp /opt/pdks/ihp-sg13g2/libs.tech/ngspice/openvaf/psp103_nqs.osdi /opt/pdks/ihp-sg13g2/libs.tech/ngspice/osdi/**
- Size the transistors for $RON = 100 \text{ Ohm}$, monitoring the leakage current
 - What about 10 Ohm ?
- Modify the transmission gate block and testbench to include an inverter for the control signal
 - Option 1: add stdcell (see
https://github.com/JorgeMarinN/OS_AnalogIC_UCLouvain_Oct2025/blob/main/design_data/tb_3stage_RO.sch)
 - Option 2: build custom circuit
- [project] Design a 4-bit analog MUX

Layout example

IHP 130nm BiCMOS technology stack

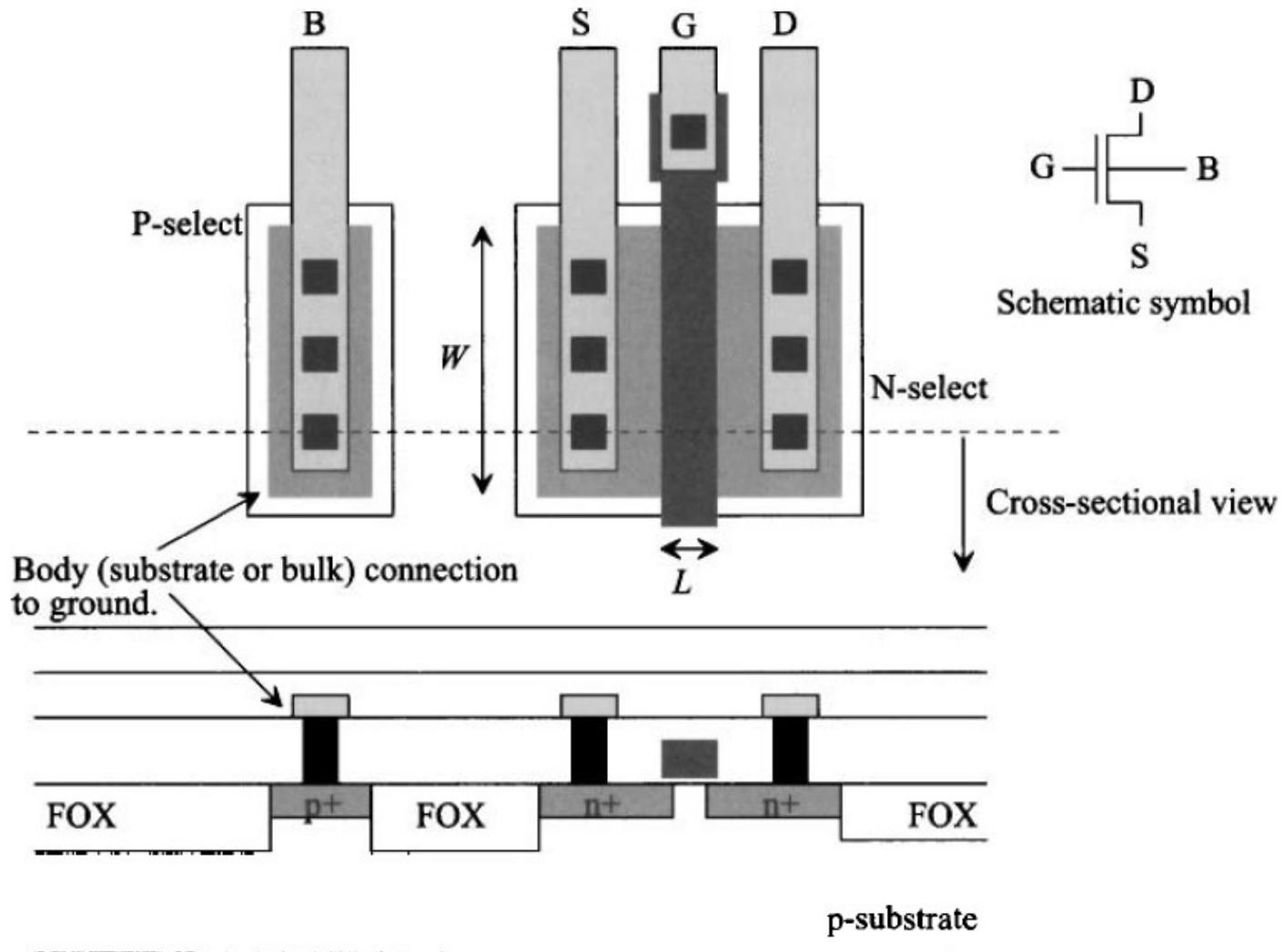


<https://www.ihp-microelectronics.com/services/research-and-prototyping-service/mpw-prototyping-service/sigec-bicmos-technologies>
<https://github.com/IHP-GmbH/IHP-Open-PDK>

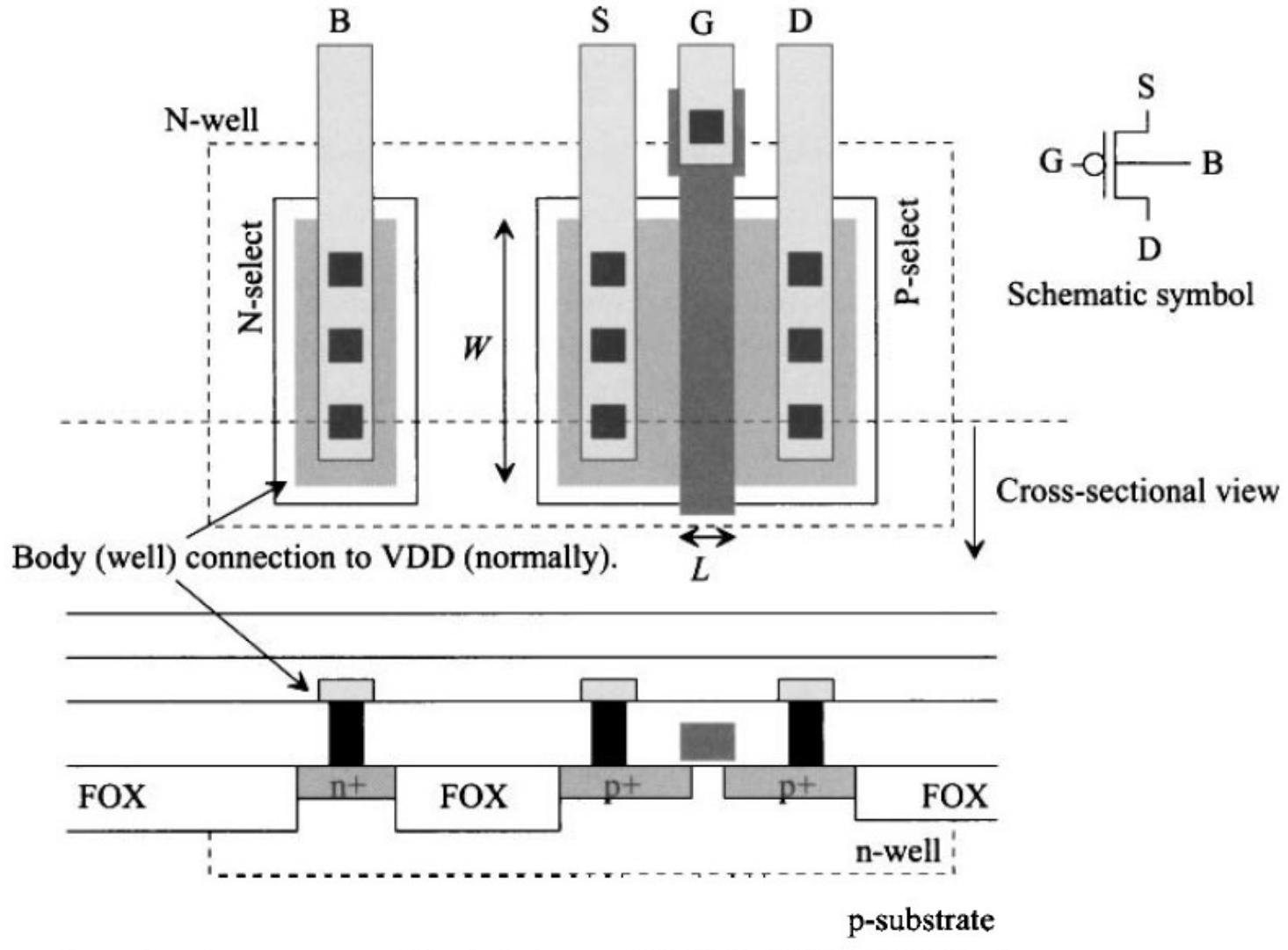
IHP 130nm BiCMOS technology features

- SG13G2 is a high performance BiCMOS technology with a $0.13\text{ }\mu\text{m}$ CMOS process
- 2 gate oxides: A thin gate oxide for the 1.2 V digital logic and a thick oxide for a 3.3 V supply voltage
- PMOS and isolated NMOS transistors are offered
- Passive components like poly silicon resistors and MIM capacitors are available
- 5 thin metal layers, two thick metal layers (2 and 3 μm thick) and a MIM layer

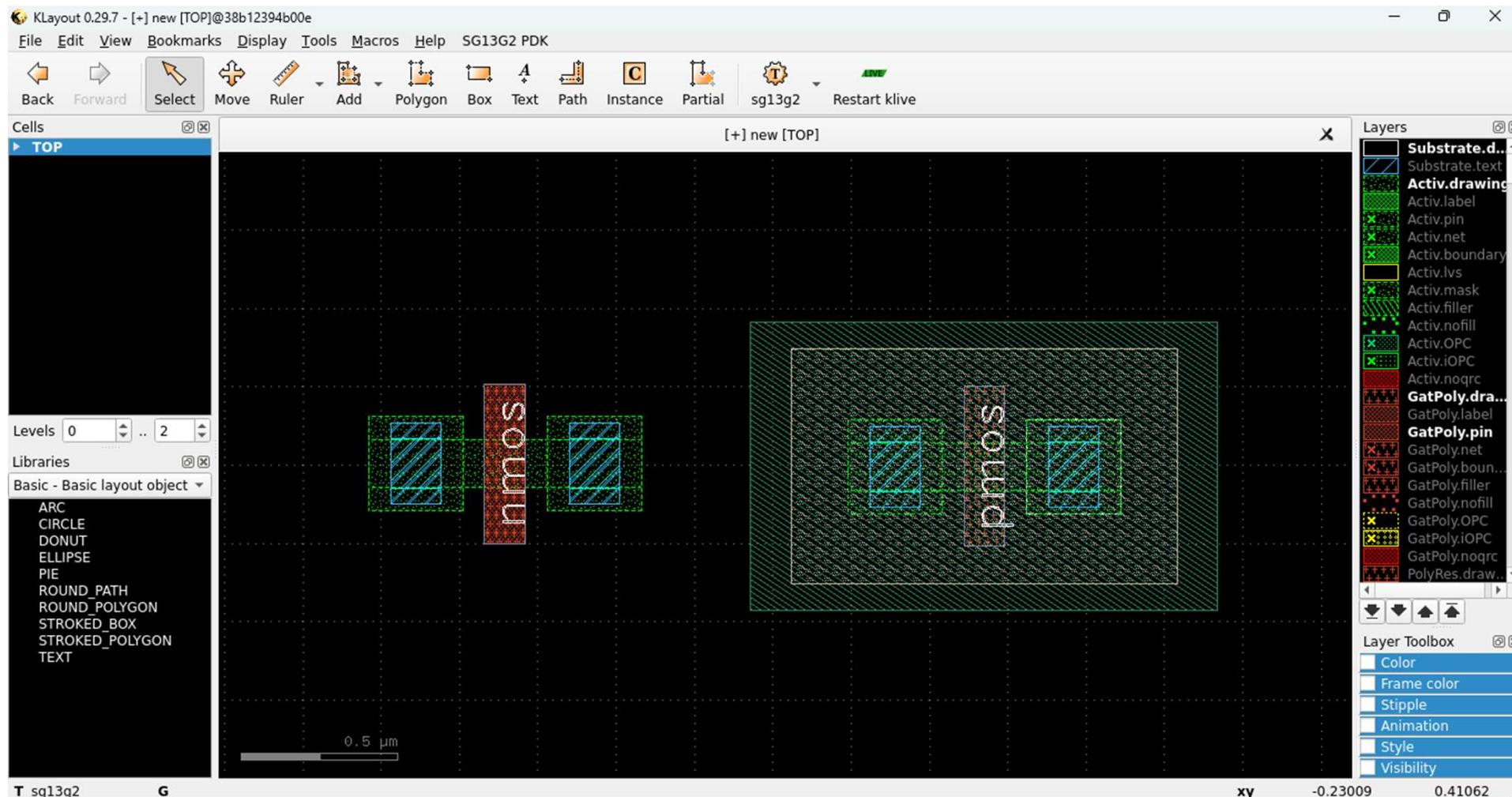
NMOS layout and cross-sectional view



PMOS layout and cross-sectional view



DEMO: IHP NMOS and PMOS PCELLs in KLayout



Layout rules → https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs/doc/doc/SG13G2_os_layout_rules.pdf

Example: Transmission gate
Layout in IHP + KLayout

Example: Tgate Layout in IHP + KLayout

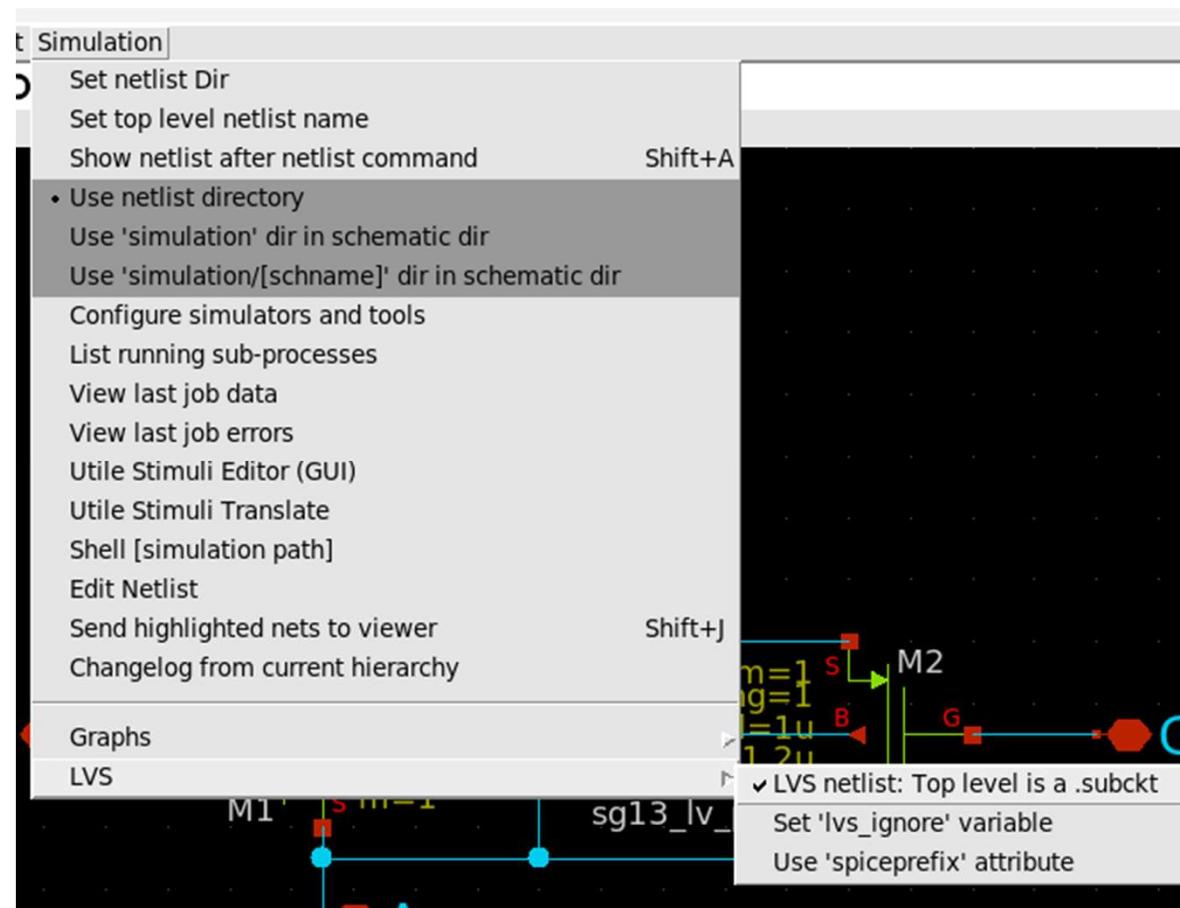
- Start Klayout
 - In the terminal: Klayout –e &
- TOP
 - Rename cell
 - Show as new top
- DRC: design rule check
 - From the GUI: Klayout → Tools → DRC
 - IHP PDK documentation
 - <https://github.com/IHP-GmbH/IHP-Open-PDK/tree/main/ihp-sg13g2/libs/doc/doc>
 - Design rules: https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs.doc/doc/SG13G2_os_layout_rules.pdf

Example: Tgate Layout in IHP + KLayout

- LVS: layout versus schematic
 - Netlist SCH
 - SG13G2 PDK → SG13G2 LVS options
 - SG13G2 PDK → Run Klayout LVS
- Example video (for GF180, from 9.51 on it's different for DRC/LVS):
<https://www.youtube.com/watch?v=vamfMryYPS4>

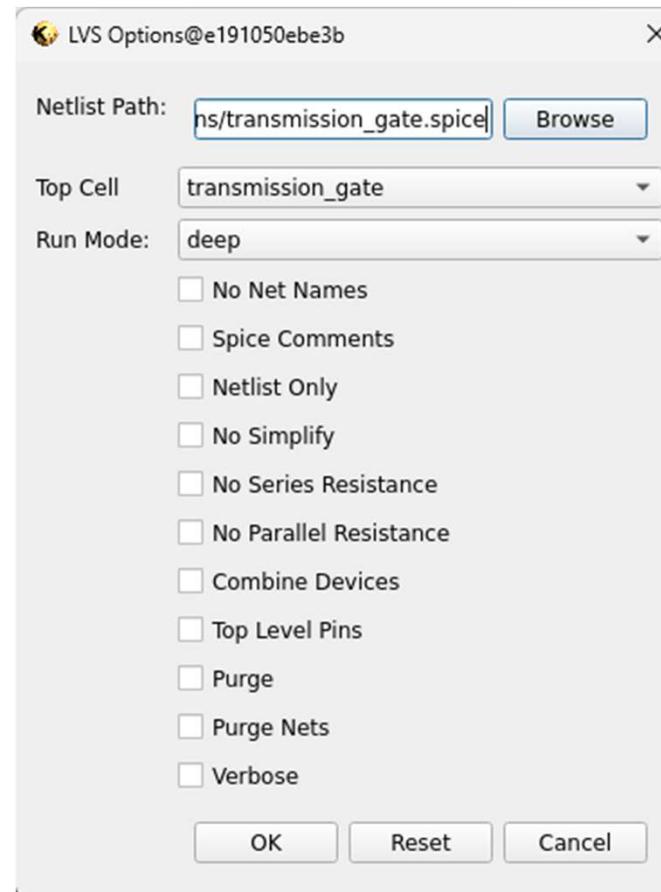
Example: Tgate Layout in IHP + KLayout

- Settings for schematic netlist generation in Xschem



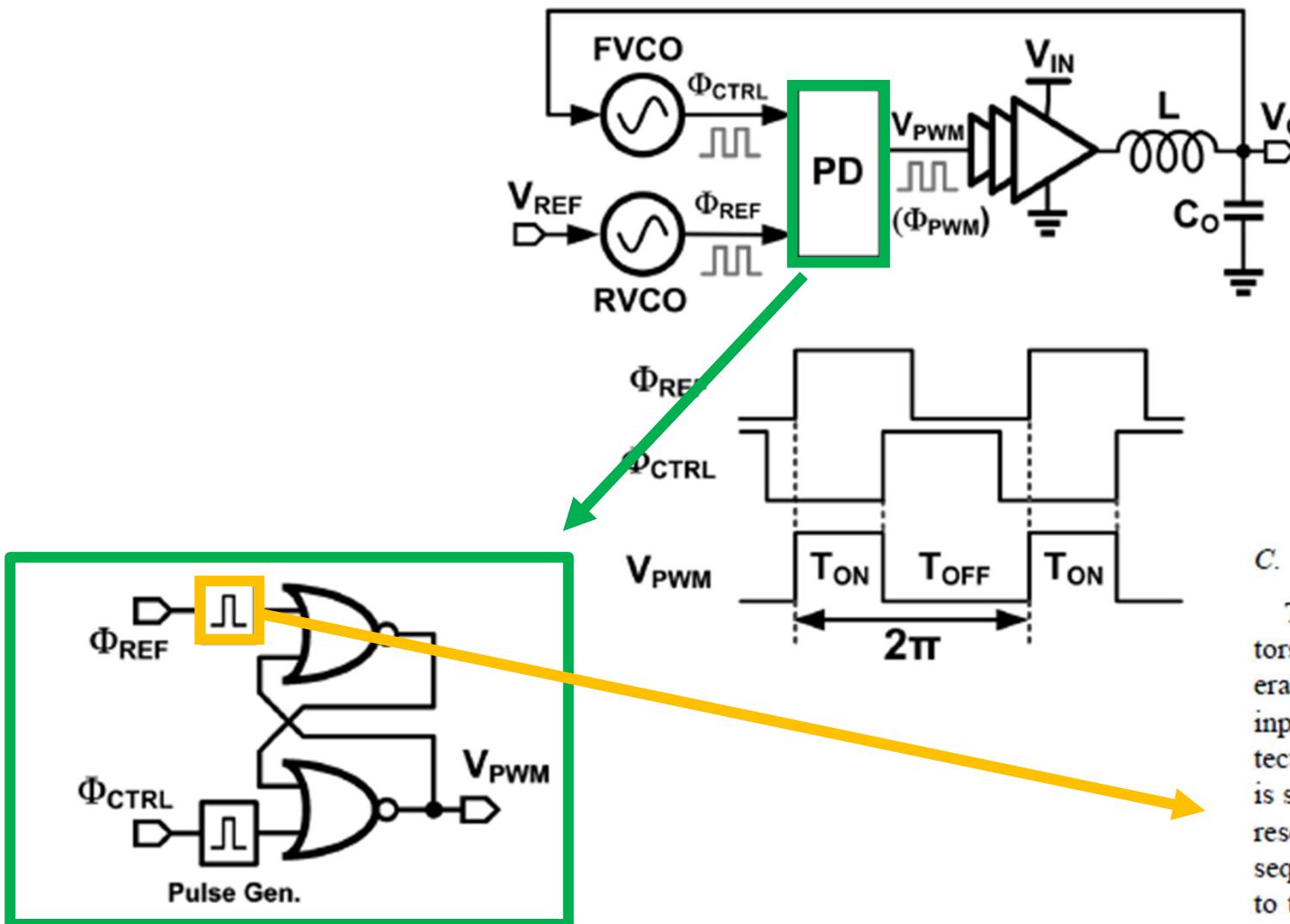
Example: Tgate Layout in IHP + KLayout

- Settings for schematic netlist loading in Klayout



Example: Single-pulse generator

Single-pulse generator in real design

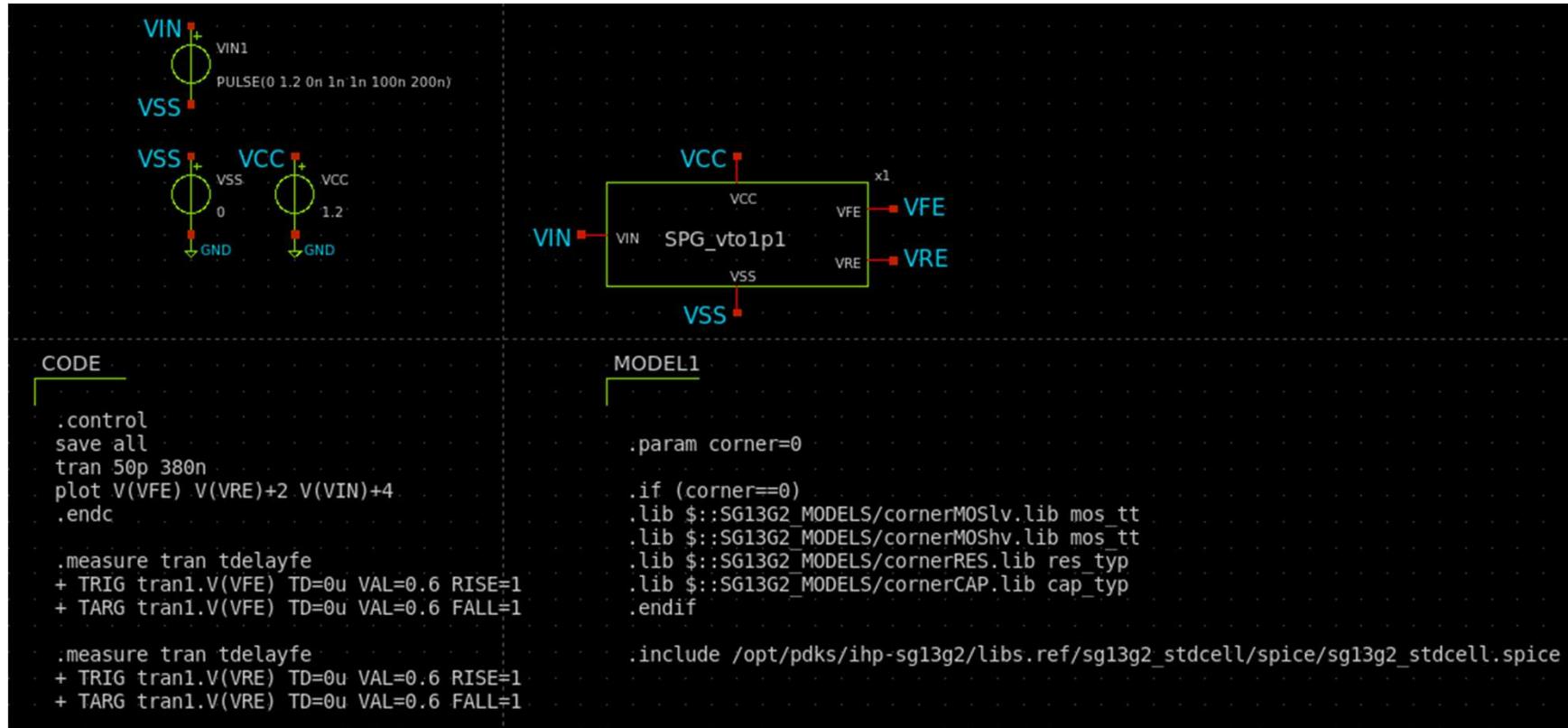


[Kim, JSSC 2015]

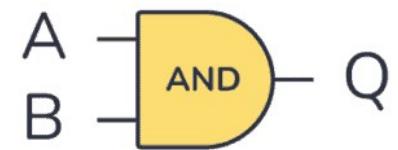
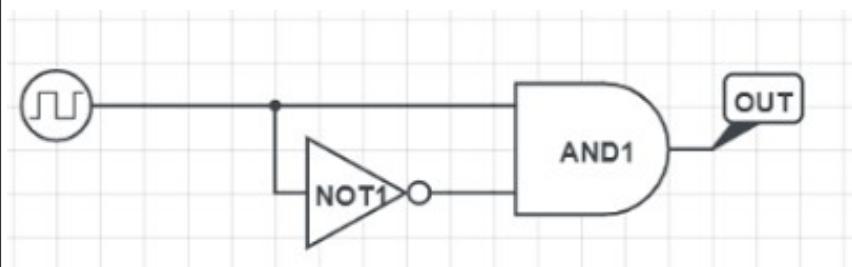
C. Phase Detector

The phase detector is simply an RS latch with pulse generators at its inputs as shown in Fig. 18. The pulse generators generate narrow pulses on every positive edge transition of their inputs, resulting in RS flip-flop like behavior for the phase detector. The duty cycle of pulse width modulated signal, V_{PWM} is set at every positive edge of the reference phase, Φ_{REF} and reset at every positive edge of the control phase, Φ_{CTRL} . Consequently, the duty cycle of V_{PWM} waveform is proportional to the difference of two control phases. As mentioned before, this implementation of phase detector avoids use of an explicit PWM as the output of the phase detector is a digital waveform with CMOS levels carrying the necessary duty cycle information provided by control input phases.

Testbench: SPG

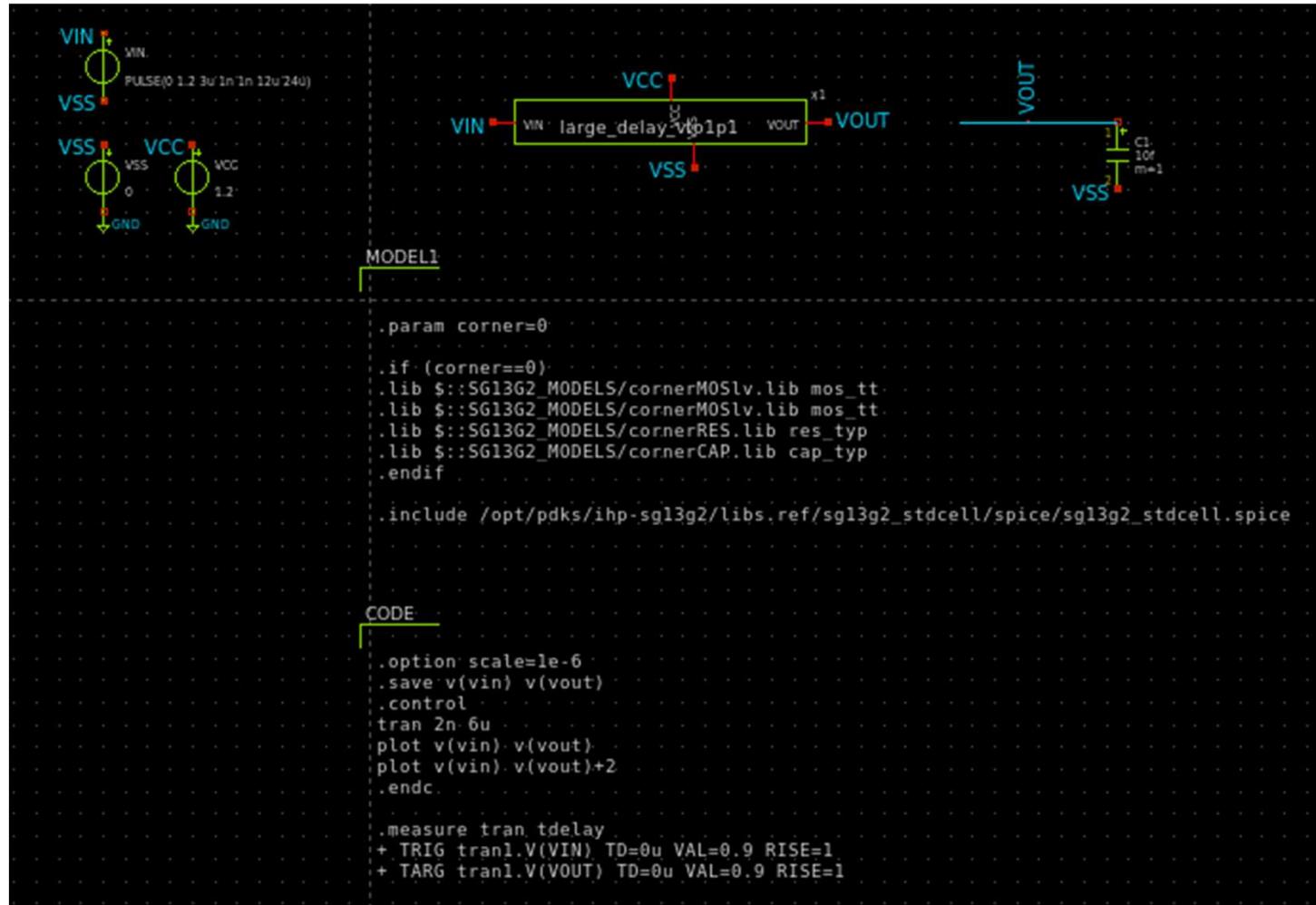


Rising-edge-to-pulse generator



A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

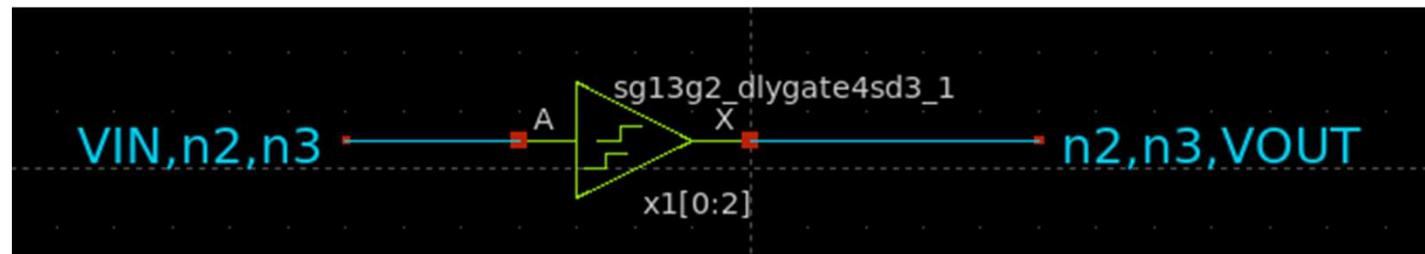
Testbench: large delay



Large delay layout

Python-generated layout

- Macros → Macros development
- Import “add_dly.py” & run
- Add connections and labels



Modifications to schematic netlist

Open

large_delay_vtolp1.spice
~/shared/OS_AnalogIC_UCU_July2025/Day3/large_delay/simulations

```
1 ** sch_path: /home/designer/shared/OS_AnalogIC_UCU_July2025/Day3/large_delay/large_delay_vtolp1.sch
2 .subckt large_delay_vtolp1 VCC VSS VIN VOUT
3 *.PININFO VIN:B VOUT:B VCC:B VSS:B
4 x1[0] VIN VCC VSS n2 sg13g2_dlygate4sd3_1
5 x1[1] n2 VCC VSS n3 sg13g2_dlygate4sd3_1
6 x1[2] n3 VCC VSS VOUT sg13g2_dlygate4sd3_1
7 .ends
8
9 * Library name: sg13g2_stdcell
10 * Cell name: sg13g2_dlygate4sd3_1
11 * View name: schematic
12 * Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
13 * pspice dspf
14 .subckt sg13g2_dlygate4sd3_1 A VDD VSS X
15 MP3 X net3 VDD VDD sg13_lv_pmos w=1.12u l=130.00n ng=1 ad=0 as=0 pd=0 ps=0 m=1
16 MP2 net3 net2 VDD VDD sg13_lv_pmos w=1.000u l=500.0n ng=1 ad=0 as=0 pd=0 ps=0 m=1
17 MP1 net2 net1 VDD VDD sg13_lv_pmos w=1.000u l=500.0n ng=1 ad=0 as=0 pd=0 ps=0 m=1
18 MP0 net1 A VDD VDD sg13_lv_pmos w=420.00n l=130.00n ng=1 ad=0 as=0 pd=0 ps=0 m=1
19 MN3 X net3 VSS VSS sg13_lv_nmos w=740.00n l=130.00n ng=1 ad=0 as=0 pd=0 ps=0 m=1
20 MN2 net3 net2 VSS VSS sg13_lv_nmos w=420.00n l=500.0n ng=1 ad=0 as=0 pd=0 ps=0 m=1
21 MN1 net2 net1 VSS VSS sg13_lv_nmos w=420.00n l=500.0n ng=1 ad=0 as=0 pd=0 ps=0 m=1
22 MN0 net1 A VSS VSS sg13_lv_nmos w=420.00n l=130.00n ng=1 ad=0 as=0 pd=0 ps=0 m=1
23 .ends
24 * End of subcircuit definition.|
```

gedit /opt/pdks/ihp-sg13g2/libs.ref/sg13g2_stdcell/spice/sg13g2_stdcell.spice &
→ Find needed cell and copy .subckt definition

SCH2GDS flow + Librelane example

- <https://github.com/librelane/librelane>
- <https://github.com/lild4d4/sch2gds/tree/librelane>

Task: customized single-pulse
generator

Task

- Modify the large_delay cell to obtain pulses with width > 2ns
- Create a DRC+LVS passing layout for this circuit
- [project] Create a layout for the full SPG

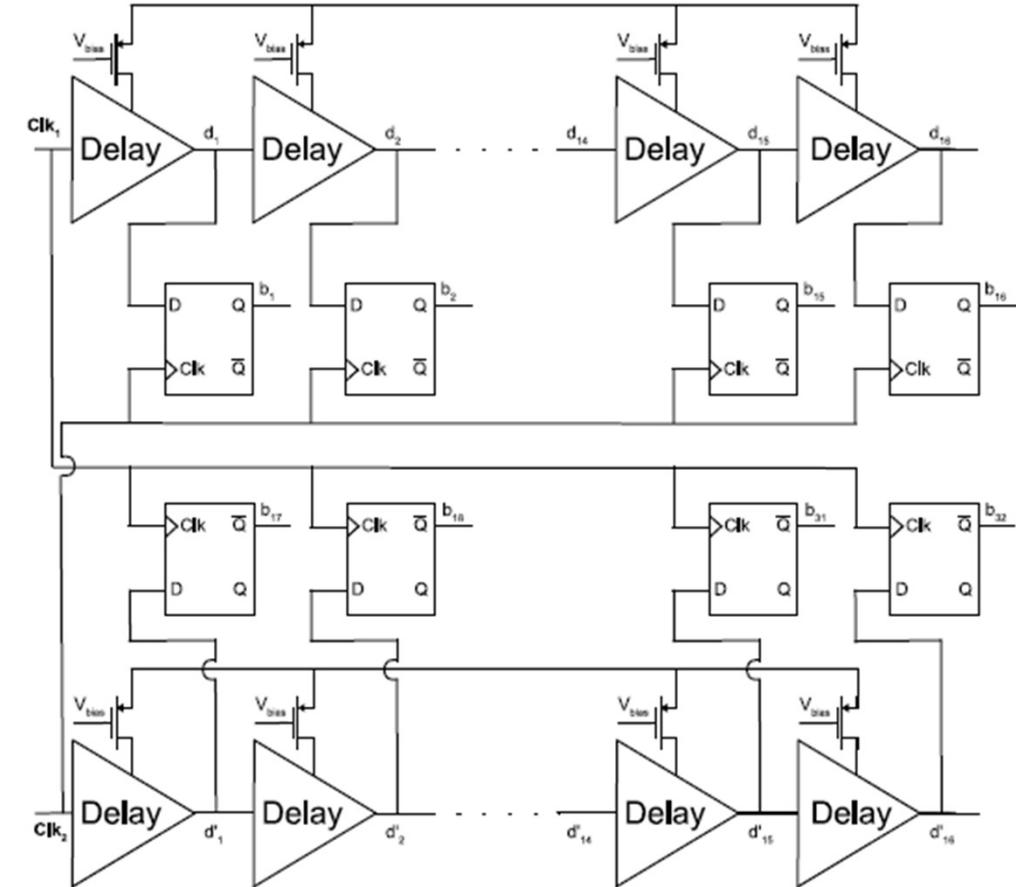
Wrap up

- From concept to transistor level design and customized logic
- First steps in automation at different levels
- OS tools + PDKs have the potential of enabling a full digital-on-top design
 - Meanwhile, analog-on-top is good enough for research/educational chips

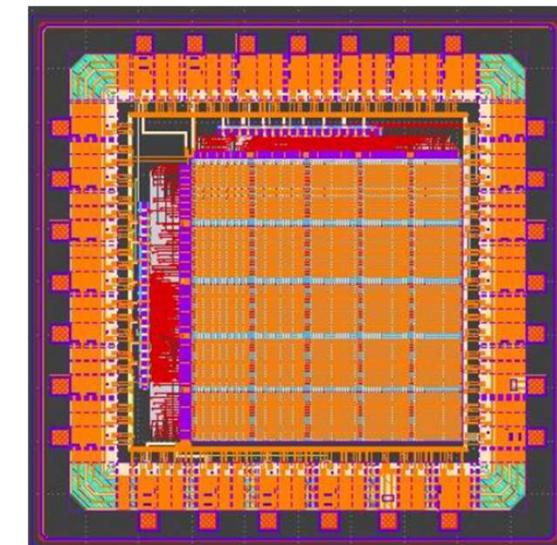
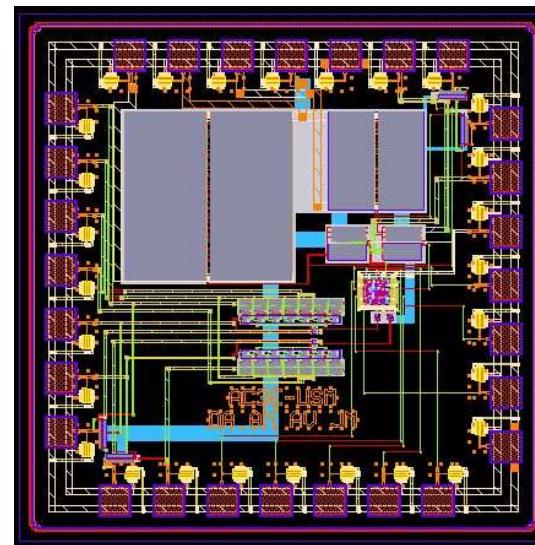
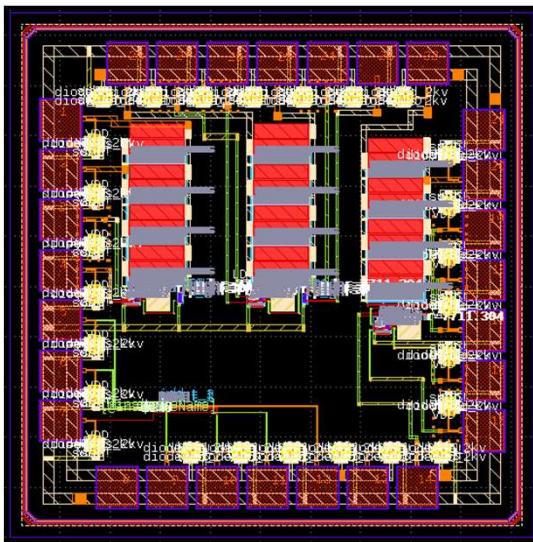
Part II: Hands-on (mini) project

Proposed miniprojects

- Design&layout a 4-bit analog MUX
- Create a layout for the full single-pulse generator
- Design&layout a time-to-digital converter
- Propose your own idea!



Thank you! Questions?



jorge.marin.ndez@gmail.com