

# Open-Source IC Design Workshop

## 3-1 Advanced circuit and layout design

Jorge Marin N., PhD

Research Associate, AC3E-UTFSM

UCU, Montevideo, Uruguay – July 2, 2025

# Agenda

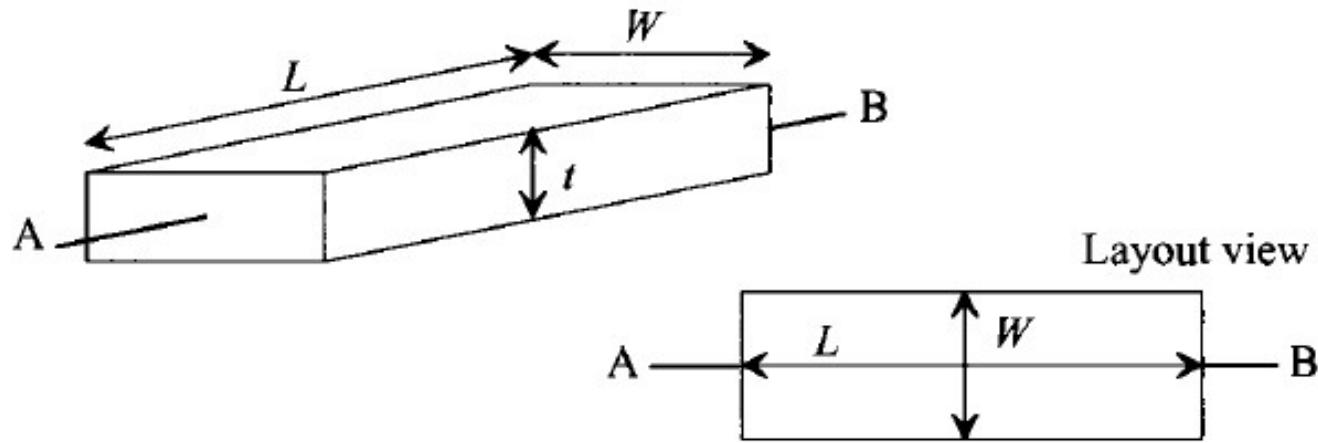
- Introduction: passive devices and layout concepts
- Single-pulse generator simulation
- Single-pulse generator layout
- Task: customized single-pulse generator

# Introduction: passive devices and layout concepts

# Passive devices in IC design

- *Passive* as opposed to *active* devices (MOSFETS and diodes)
- Mainly: resistors, capacitors and inductors (latter are less common)
- This lecture will cover the implementation of such devices in integrated circuits (in particular, standard CMOS)
- Additionally, we will review layout strategies for such devices, some of which can be generalized for active devices and building blocks

# Resistors in CMOS technology



[J. Baker, 2010]

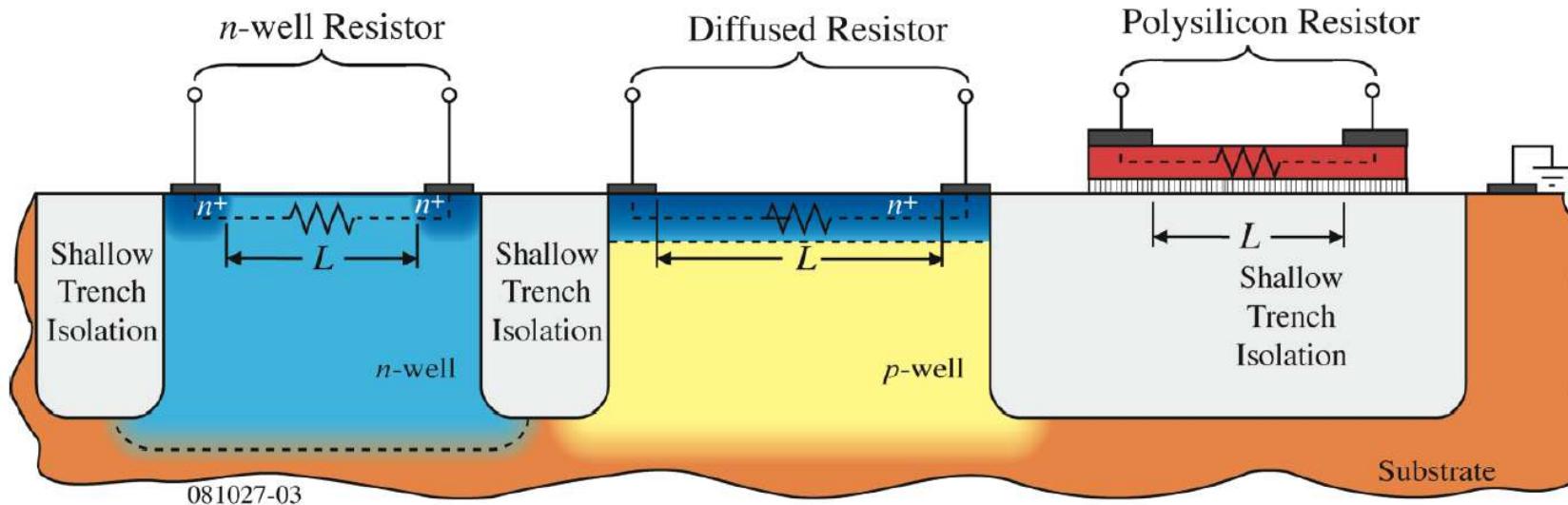
$$R = \frac{\rho}{t} \cdot \frac{L \cdot \text{scale}}{W \cdot \text{scale}} = \frac{\rho}{t} \cdot \frac{L}{W}$$

$$R = R_{\text{square}} \cdot \frac{L}{W} \rightarrow R_{\text{square}} = \frac{\rho}{t}$$

- $\rho$ : material's resistivity
- Remember: we can only define W and L
- $R_{\text{square}}$ : sheet resistance in  $\Omega/\text{square}$

- CMOS is optimized for digital  $\rightarrow$  Efforts focus on REDUCING resistors
- R is normally not used, if used they are needed at edge (e.g. ESD, CLK generator)
- Analog needs LARGE, PREDICTABLE and STABLE resistors

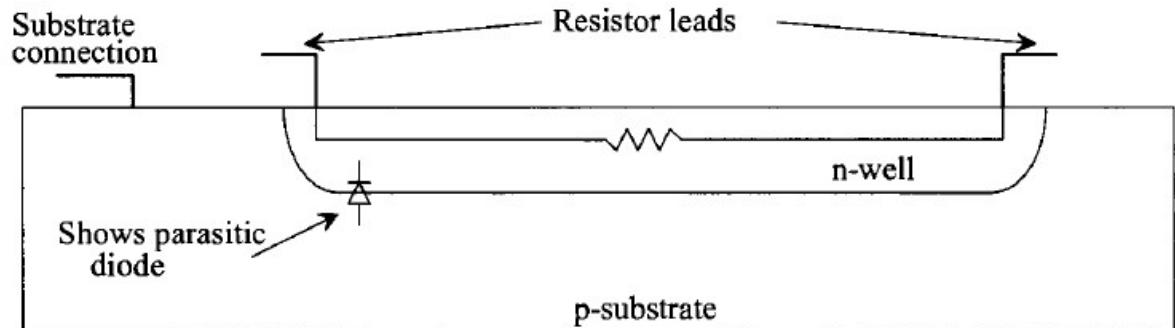
# Types of resistors in CMOS technology



[P. E. Allen's slides, 2016]

- Diffused and/or implanted resistors
- Well resistors
- Polysilicon resistors
- Metal resistors

# Resistors in CMOS technology: the well



- Good when large values of resistance are needed
- Parasitics are large and resistance is voltage dependent
- NL parasitic cap → cross section changes with PN
- Good thermal dissipation

**SKY130 →**

Parameter	NOM	LSL	USL	Units	Description
RSNW	950	550	1350	Ω/□	N-Well sheet resistance

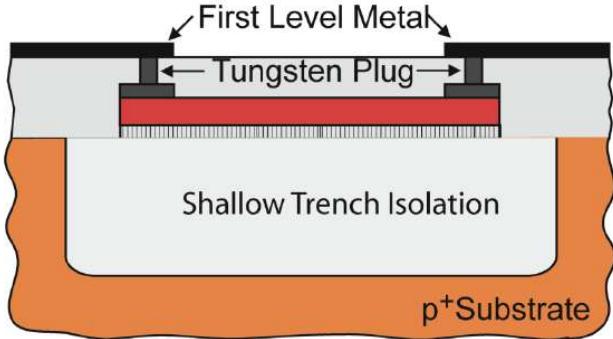
<https://skywater-pdk.readthedocs.io/en/main/rules/device-details.html#generic-resistors>

**GF180MCU →**

PARAMETERS	XTORS	DIMENSIONS / COMMENTS	MIN	TYP	MAX	UNITS
Wide Nwell (unsalicided)		5 um (measured @I=100uA)	800	1000	1200	Ω/sq

[https://gf180mcu-pdk.readthedocs.io/en/latest/analog/spice/elec\\_specs/elec\\_specs\\_5\\_1.html](https://gf180mcu-pdk.readthedocs.io/en/latest/analog/spice/elec_specs/elec_specs_5_1.html)

# Resistors in CMOS technology: polysilicon



- Good general resistor with low parasitics
- Lower resistance density than N-well implementation
- Low TCR, good linearity
- May need extra mask to block silicide (cost!)

Parameter	NOM	LSL	USL	Units	Description
SKY130 →	RP0P35X20SQ	7888	6691	9086	Ω P+ poly resistor, 0.35 μm wide, 20 squares

<https://skywater-pdk.readthedocs.io/en/main/rules/device-details.html#generic-resistors>

PARAMETERS	XTORS	DIMENSIONS / COMMENTS	MIN	TYP	MAX	UNITS
GF180MCU →	Wide N+ Poly (unsalicided)	5 um (measured @I=100uA)	250	310	370	Ω/sq

[https://gf180mcu-pdk.readthedocs.io/en/latest/analog/spice/elec\\_specs/elec\\_specs\\_5\\_1.html](https://gf180mcu-pdk.readthedocs.io/en/latest/analog/spice/elec_specs/elec_specs_5_1.html)

# Resistors in CMOS technology: IHP 130nm

## 2.7. Rsil-Specs

### ! Tip

Rsil utilizes salicided, n-doped gate polysilicon as resistor material.

Parameter	Name	Unit	Min	Target	Max	Meas.Cond.
Sheet Resistance	RSNRSIL	$\Omega$	6.2	7.0	7.8	A.i
Line Width Delta	DWRSIL	nm	-20	10	40	A.i
Temperature Coefficients	TC1NRSIL	ppm/K		3100		A.af
Temperature Coefficients	TC2NRSIL	ppm/K <sup>2</sup>		0.3		A.af
Matching Coefficient	MATRSIL1	nm		6		A.ac
Matching Coefficient	MATRSIL2	nm		1.4		A.ac
Metal-to-Body- Resistance	RCRSIL			4.5		A.ae
Max. Current Density						

# Resistors in CMOS technology: IHP 130nm

## 2.8. Rppd-Specs

### ! Tip

Rppd utilizes unsalicided, p-doped gate polysilicon as resistor material. For realizing precision resistors, a line width of 2 $\mu$ m or higher is recommended.

Parameter	Name	Unit	Min	Target	Max
Sheet Resistance	RSRPPD	$\Omega$	235	260	285
Line Width Delta	DWRPPD	nm	-24	6	36
Temperature Coefficients	TC1NRPPD	ppm/K		170	
Temperature Coefficients	TC2NRPPD	ppm/K <sup>2</sup>		0.4	
Matching Coefficient	MATRPPD	nm		15	
Metal-to-Body- Resistance	RCRPPD	$\Omega \cdot \mu m$		35	
Temperature Coefficient Metal-toBody-Resistance	TC3NRPPD	ppm/K		-950	
Max. Current Density	IMRPPD	mA/ $\mu m$		1.2	

# Resistors in CMOS technology: IHP 130nm

## 2.9. Rhigh-Specs

### ! Tip

Rhigh utilizes unsalicided, partially compensated gate polysilicon as resistor material.

Parameter	Name	Unit	Min	Target	Max	Meas.Cond.
Sheet Resistance	RSRHIGH	$\Omega$	1160	1360	1560	A.i
Line Width Delta	DWRHIGH	nm	-80	-40	0	A.i
Temperature Coefficients	TC1NRHIGH	ppm/K		-2300		A.af
Temperature Coefficients	TC2NRHIGH	ppm/K <sup>2</sup>		2.1		A.af
Matching Coefficient	MATRHIGH	nm		48		A.ac
Metal-to-Body- Resistance	RCRHIGH	$\Omega \cdot \mu\text{m}$		80		A.ae
Max. Current Density	IMRHIGH	mA/ $\mu\text{m}$			0.6	

# Resistors in CMOS technology: IHP 130nm

Parameter	Name	Unit	Min	Target
Substrate Resistivity	RSBLK	Ωcm	37.5	50
Salicidized GatPoly (n+)				
Unsalicidized GatPoly (n+)				
Unsalicidied GatPoly (p+)				
Metal1 Snake Sheet Resistance	SNAKEM1	mΩ	90	115
Unsalicidied nSD-Activ Sheet Resistance	RSNSD0	Ω	55	67
Unsalicidied pSD-Activ Sheet Resistance	RSPSD0	Ω	69	79
Metal2 Snake Sheet Resistance	SNAKEM2	mΩ	70	88
Metal3 Snake Sheet Resistance	SNAKEM3	mΩ	70	88
Metal4 Snake Sheet Resistance	SNAKEM4	mΩ	70	88
Metal5 Snake Sheet Resistance	SNAKEM5	mΩ	70	88
TopMetal1 Snake Sheet Resistance	SNAKETM1	mΩ	14	18
TopMetal2 Snake Sheet Resistance	SNAKETM2	mΩ	7.5	11

# Resistors in CMOS technology: IHP 130nm

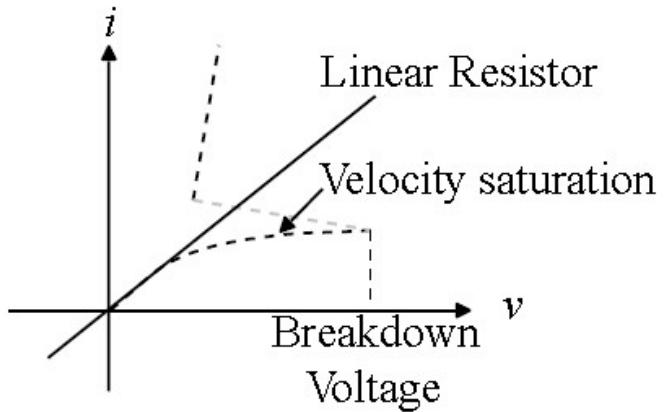
Metal1 Sheet Resistance	RSMET1	mΩ	85	110
Metal2 Sheet Resistance	RSMET2	mΩ	73	88
Metal3 Sheet Resistance	RSMET3	mΩ	73	88
Metal4 Sheet Resistance	RSMET4	mΩ	73	88
Metal5 Sheet Resistance	RSMET5	mΩ	73	88
TopMetal1 Sheet Resistance	RSTM1	mΩ	15	18
TopMetal2 Sheet Resistance	RSTM2	mΩ	7.5	11
Metal1 Line Width Delta	DWMET1	nm	-64	-24
Metal2 Line Width Delta	DWMET2	nm	-56	-16
Metal3 Line Width Delta	DWMET3	nm	-56	-16
Metal4 Line Width Delta	DWMET4	nm	-56	-16
Metal5 Line Width Delta	DWMET5	nm	-50	-20
TopMetal1 Line Width Delta	DWTM1	nm	-300	-100
TopMetal2 Line Width Delta	DWTM2	nm	-340	-140
Metal1 Sheet Resistance Temperature Coefficient	TC1RSMET1	ppm/K		3400
Metal2 Sheet Resistance Temperature Coefficient	TC1RSMET2	ppm/K		3500
Metal3 Sheet Resistance Temperature Coefficient	TC1RSMET3	ppm/K		3500
Metal4 Sheet Resistance Temperature Coefficient	TC1RSMET4	ppm/K		3500
Metal5 Sheet Resistance Temperature Coefficient	TC1RSMET5	ppm/K		3500
TopMetal1 Sheet Resistance Temperature Coefficient	TC1RSTM1	ppm/K		3700
TopMetal2 Sheet Resistance Temperature Coefficient	TC1RSTM2	ppm/K		3800

# CMOS resistors 1

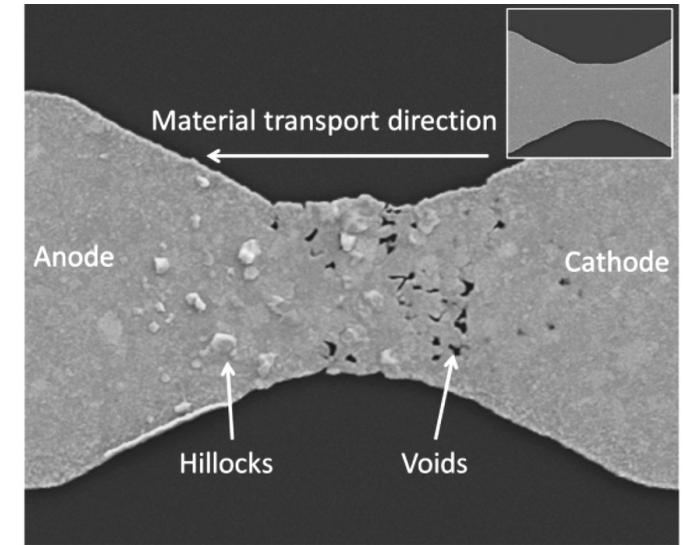
- Absolute value →

$$R = R_{square} \cdot \frac{L}{W}$$

- Linearity →

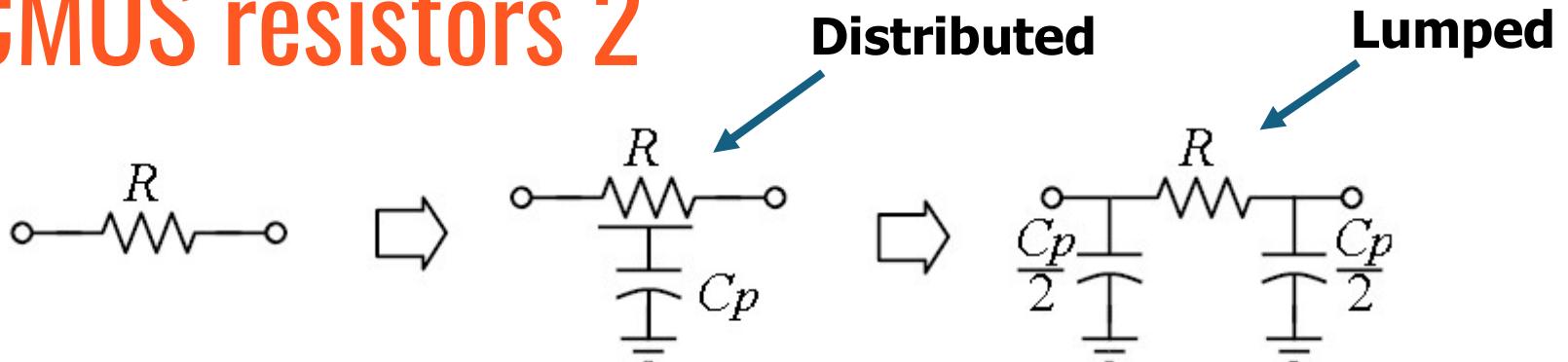


- Electromigration (D. Fernandez' video on LinkedIn) →
  - Too much current move metal atoms → Layer is destroyed
  - MAX CURRENT!
  - Rule of thumb: 1mA/ $\mu m$  → But tech dependent

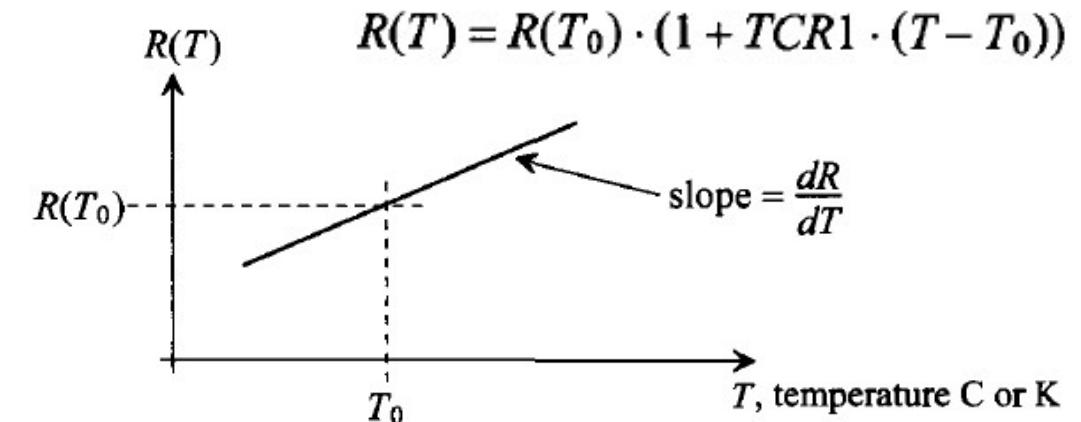
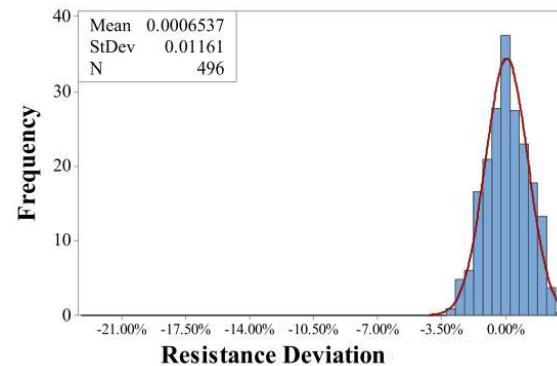


# CMOS resistors 2

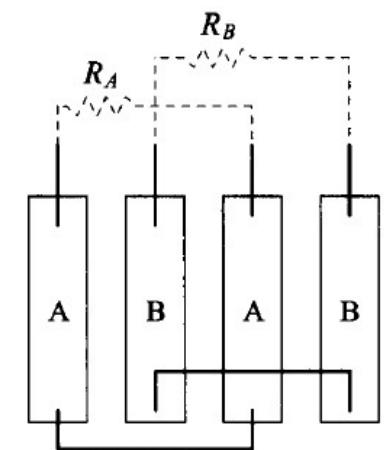
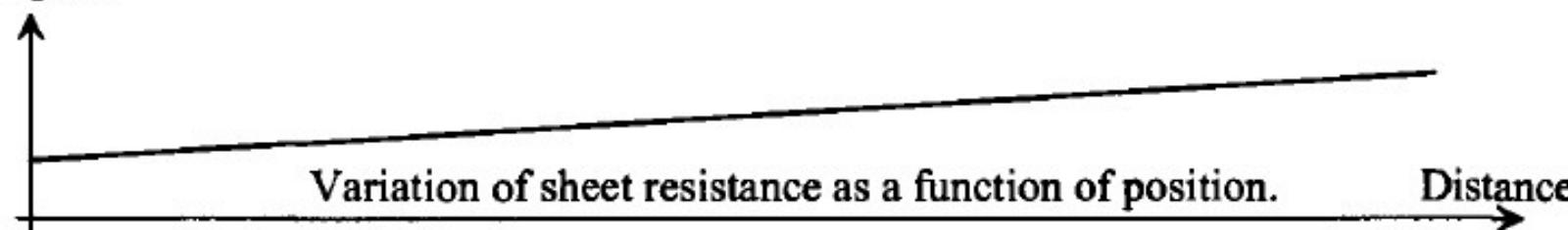
- Parasitics →



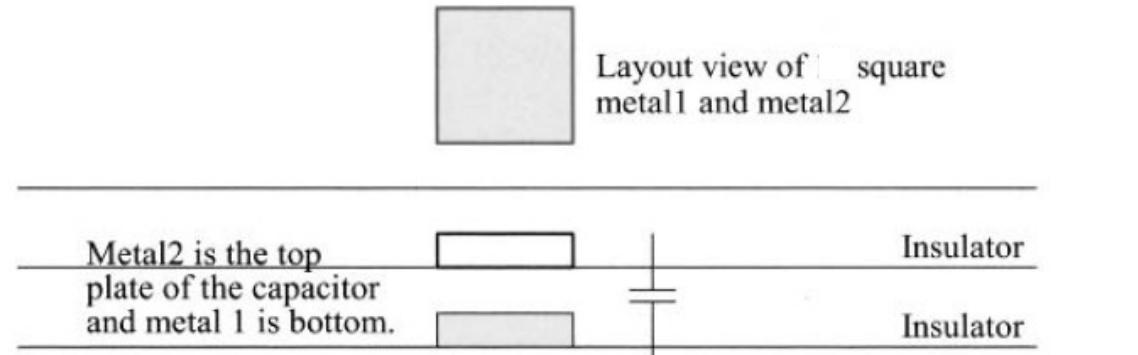
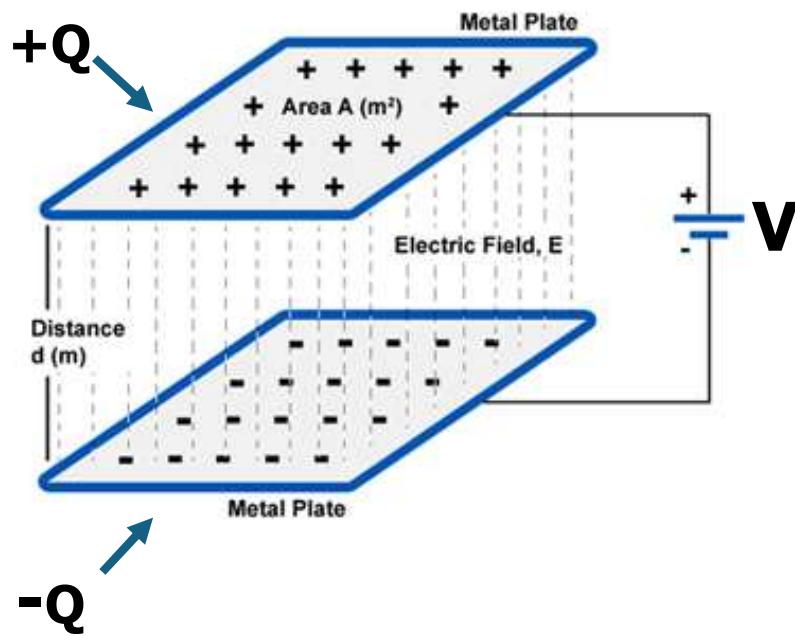
- PVT (process, voltage, temperature) →



- M  $\Omega/\text{square}$



# Capacitors in CMOS technology



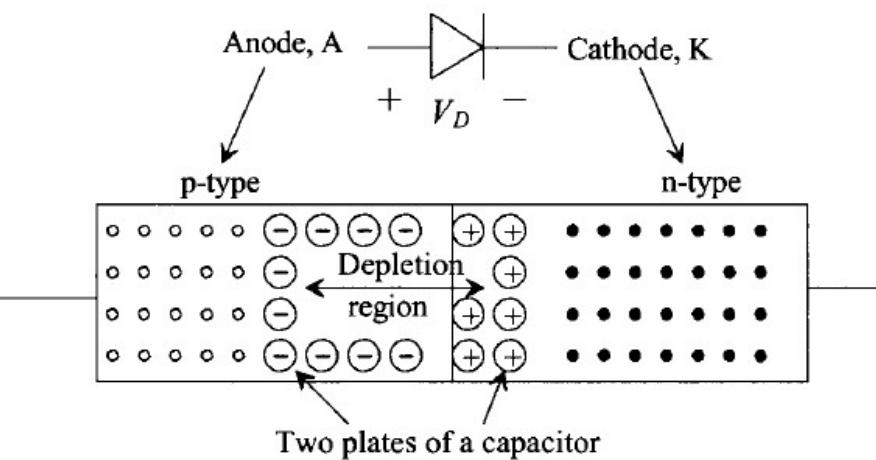
[J. Baker, 2010]

- $C = \epsilon A/d = C_{\text{square}} * A$
- Remember: we can only define W and L
- $R_{\text{square}}$ : sheet resistance in  $\Omega/\text{square}$

- Easiest implementation uses parallel metal plates
- $\epsilon$ : permittivity of insulator
- $C = Q/V \rightarrow I = C \cdot dV/dt$

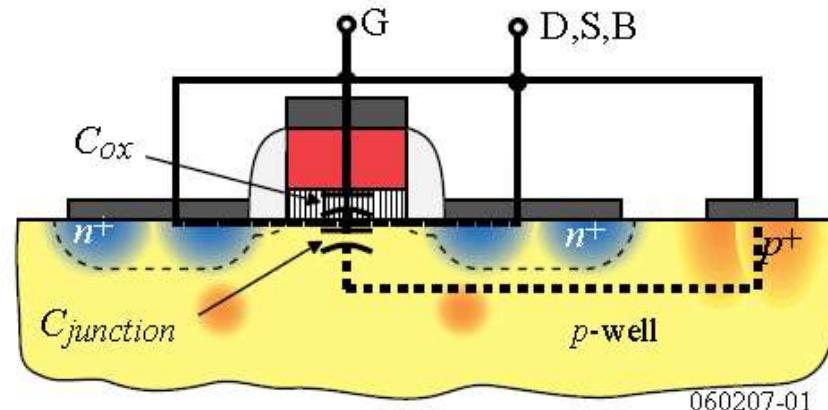
# Types of capacitors in CMOS technology

(1)



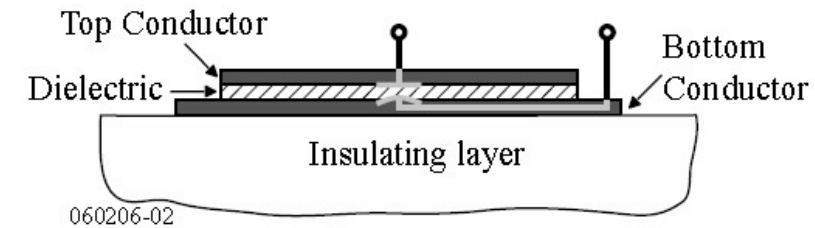
[J. Baker, 2010]

(2)



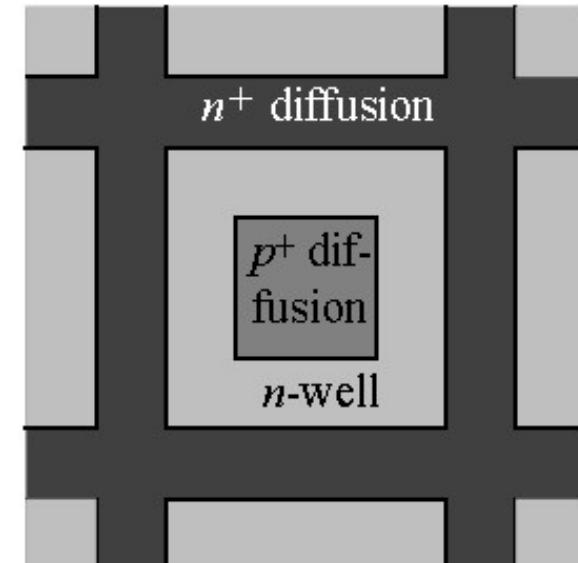
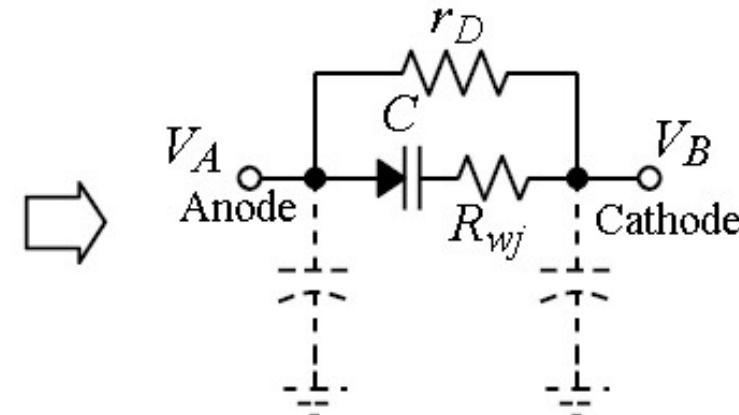
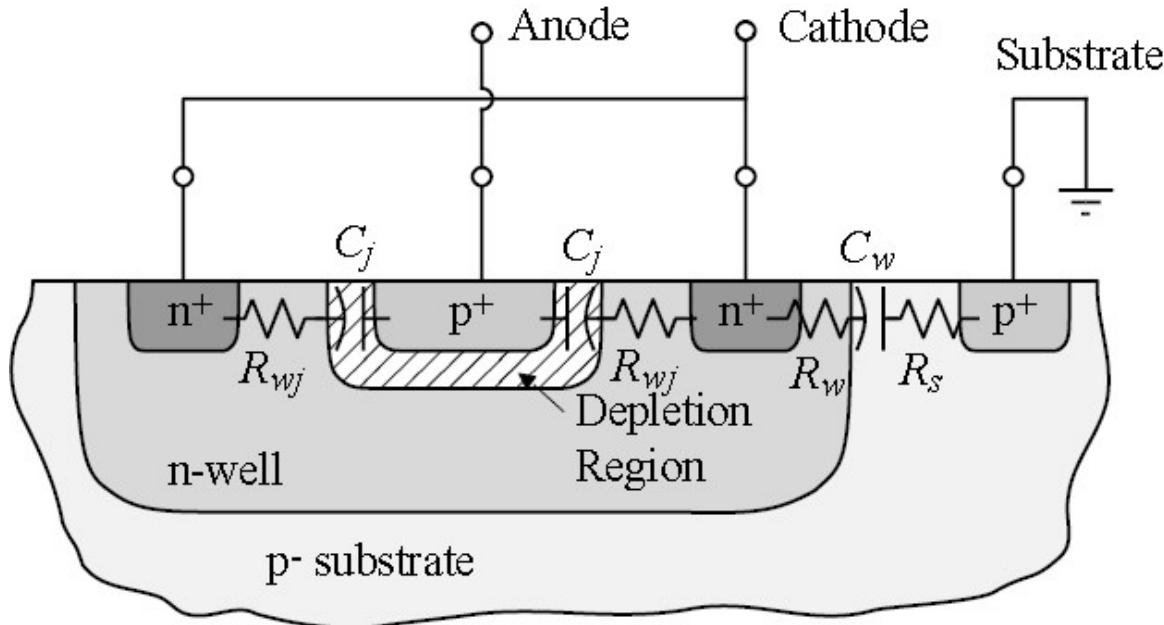
[P. E. Allen's slides, 2016]

(3)



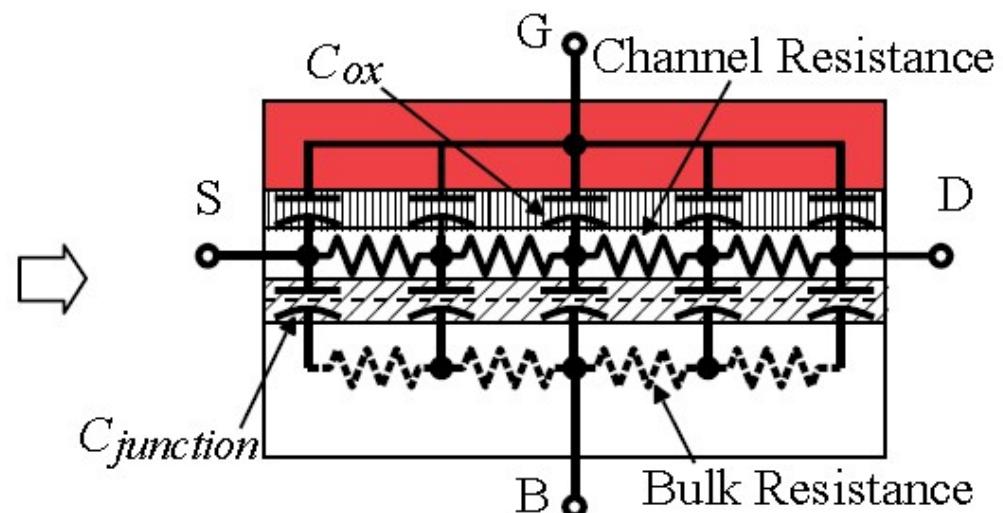
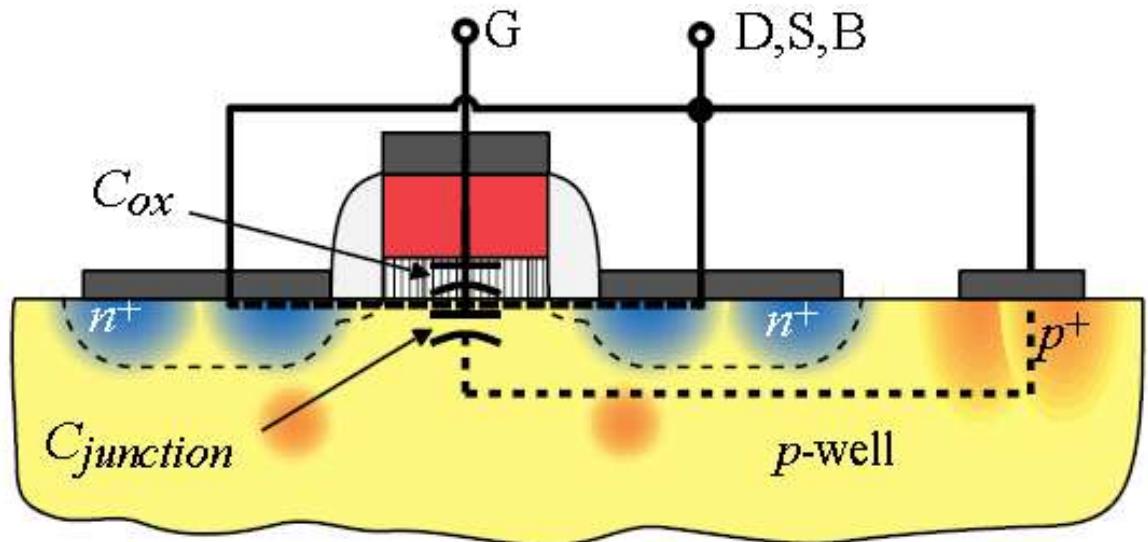
- (1) PN junction in depletion (reverse biasing).
- (2) MOSFET gate capacitor (MOSCAP).
- (3) Metal (poly) – insulator – metal (poly) capacitor (MIM, MOM).

# Capacitors in CMOS technology: PN junction



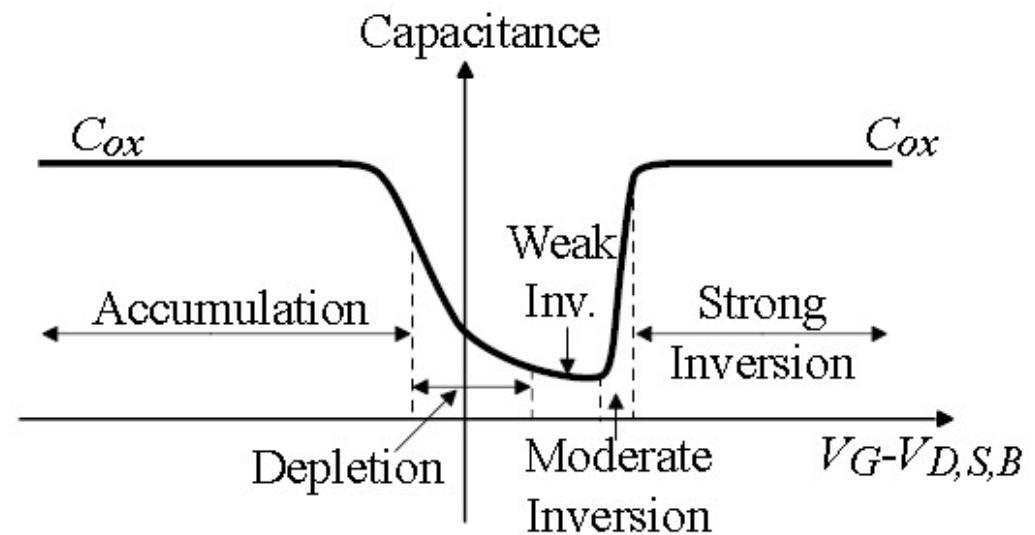
- Nonlinear
- Moderate density
- Could be considered a parasitic element

# Capacitors in CMOS technology: MOSCAP

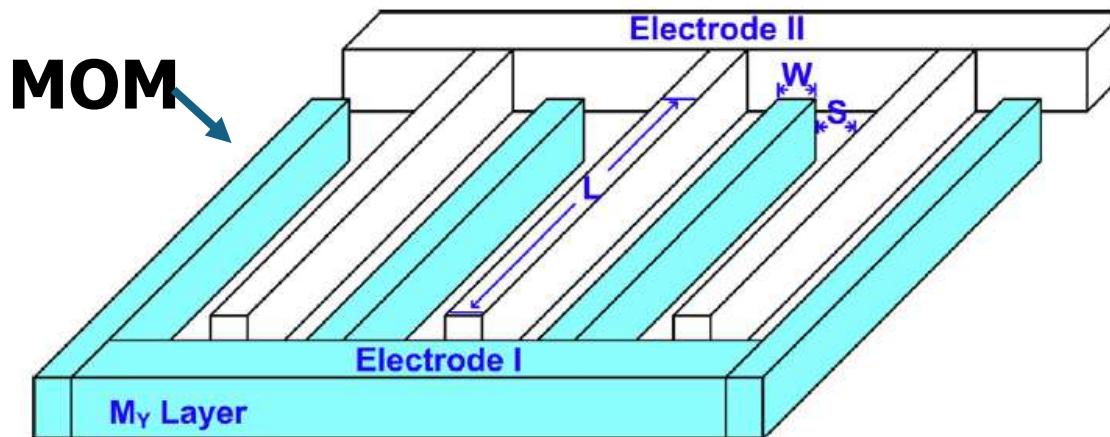
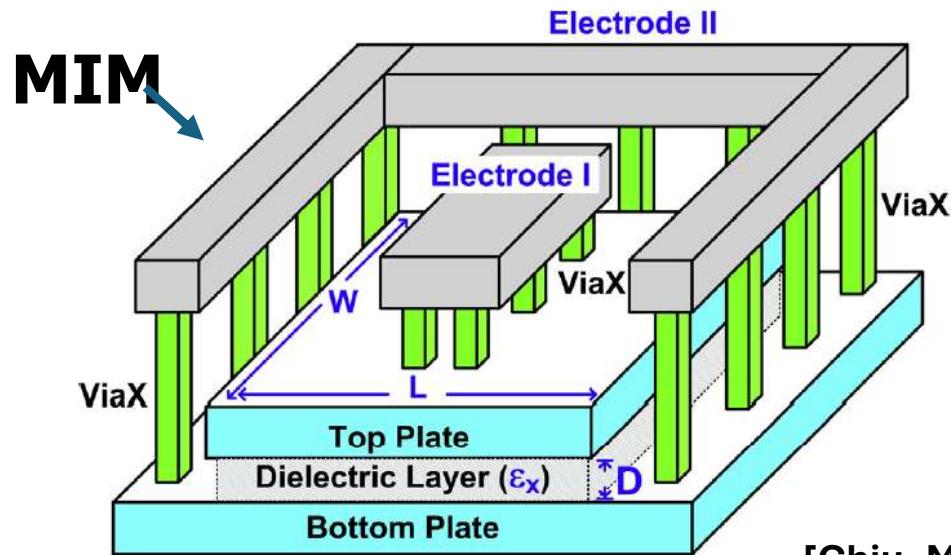


$$C_{gate} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_j}}$$

- Largest
- But very nonlinear →  $C = C(V)$
- sometimes it's not relevant
- Can implement **varactors**



# Capacitors in CMOS technology: MIM & MOM



[Chiu, Micro. Reliability, 2014]

- MOM
  - available "for free"
  - but large distance between plates → optimized for digital!
  - top view controlled by lithography, not deposition → ACCURATE!
- MIM
  - extra masks
  - thin later, hard to manufacture (antenna effect)
  - Both have good linearity and acceptable density → good for high precision analog → COMBINE!

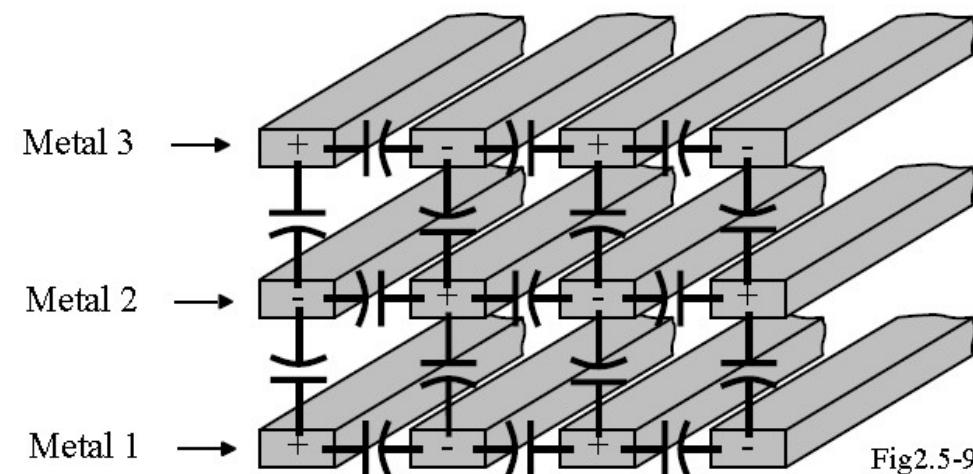
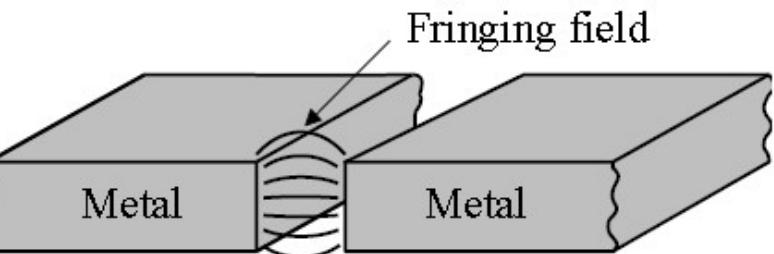


Fig2.5-9

# CMOS capacitors

- Absolute value (capacitor density)  $\rightarrow C_{\text{square}} * A$

- Losses, i.e. Q factor  $\rightarrow$

- $R_s/p$ : series/parallel equivalent resistance

$$Q = \frac{1}{\omega CR_s} = \omega CR_p$$

- Parasitics

- Resistors
  - Capacitors of each plate to ground
    - Top plate parasitic ~0.1% to 1% of desired value
    - Bottom plate parasitic ~5% to 20% of desired value!!!

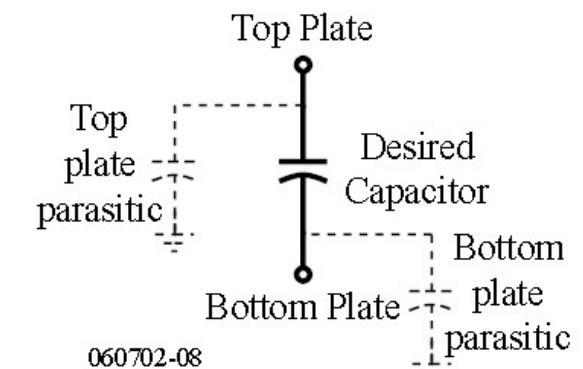
- Accuracy  $\rightarrow$  matching! (see next slides)

- Linearity  $\rightarrow Q = CV$

- Semiconductors  $\rightarrow$  depletion regions and body effects generate nonlinearity

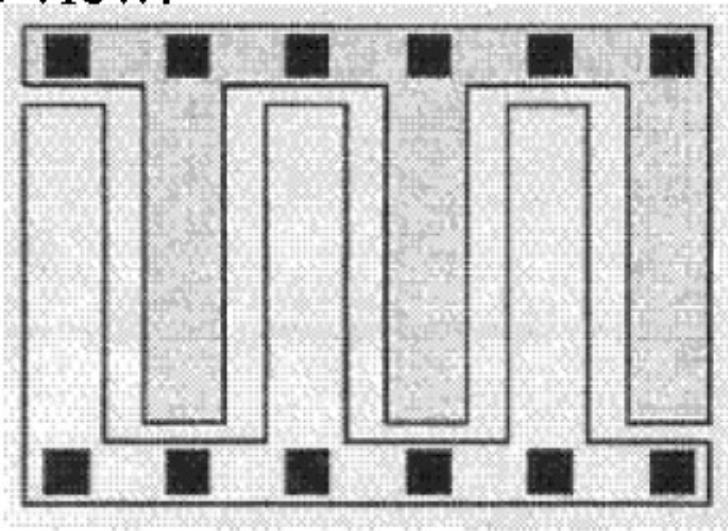
- PVT  $\rightarrow$  absolute accuracies ~10% / TEMPCO ~25 to 40 ppm/C°

- Also voltage coefficient!

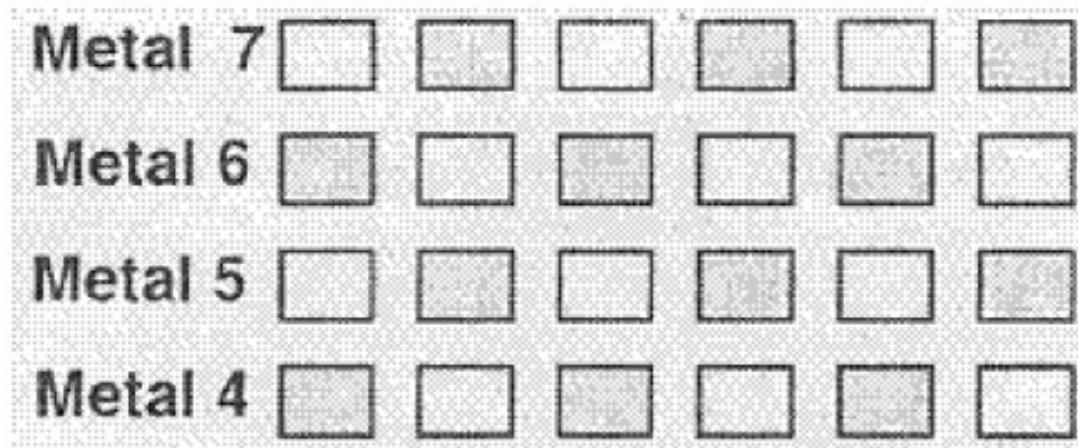


# MOM caps implementation

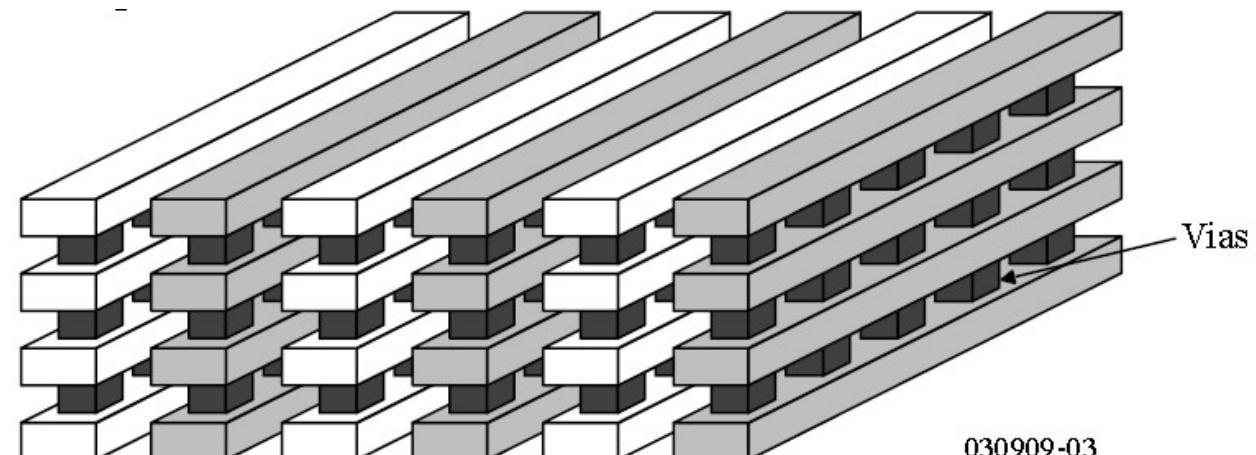
Top view:



Side view:

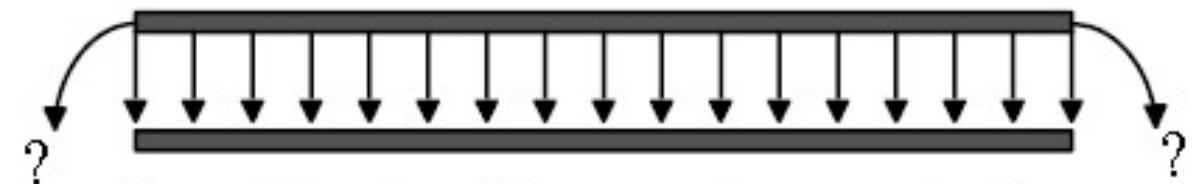
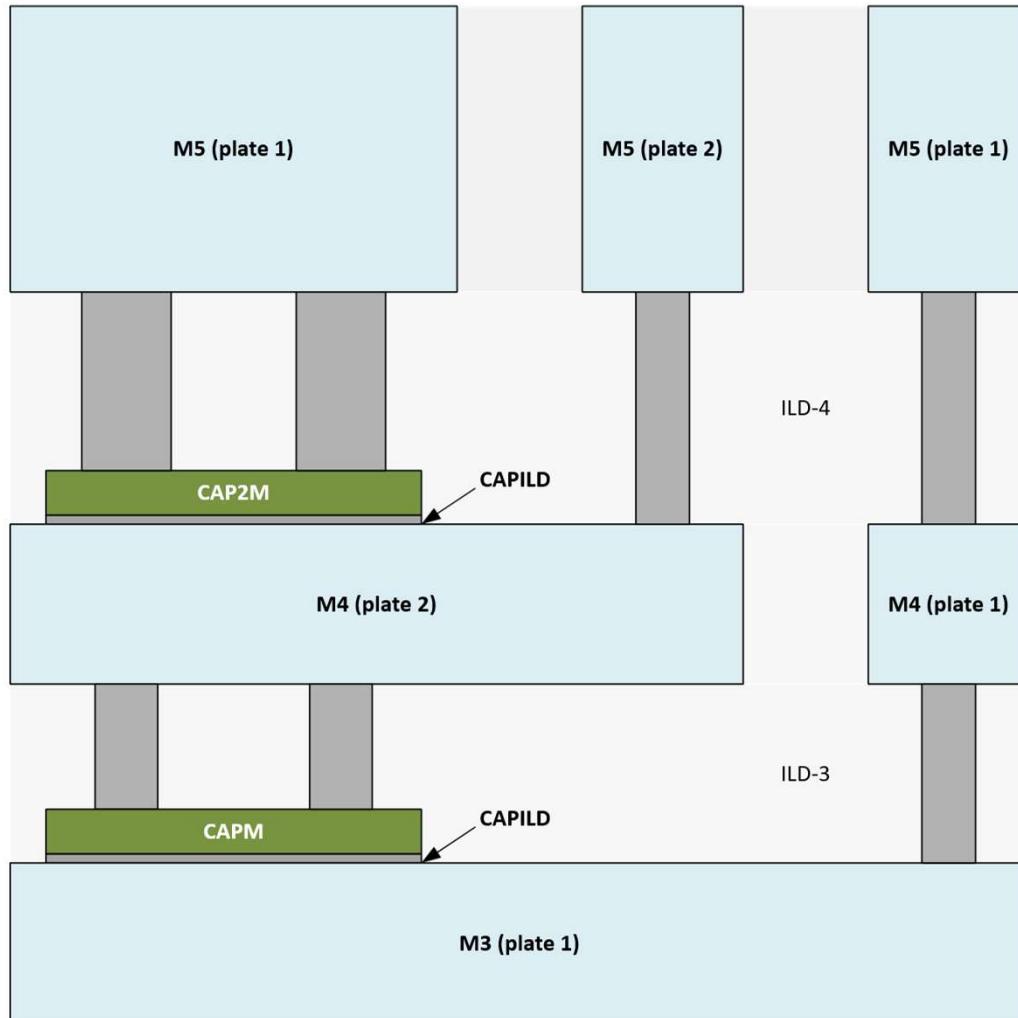


- MOM
- Same parasitic capacitor to substrate in both plates
- Vertical and lateral flux → “fingers”
- + multiple layers
- Also: use vias for extra capacitor lateral area → lithography dependent!

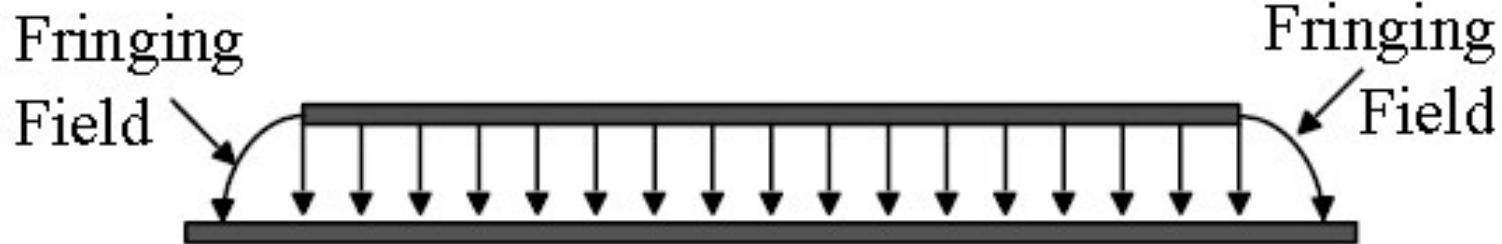


030909-03

# MIM caps implementation



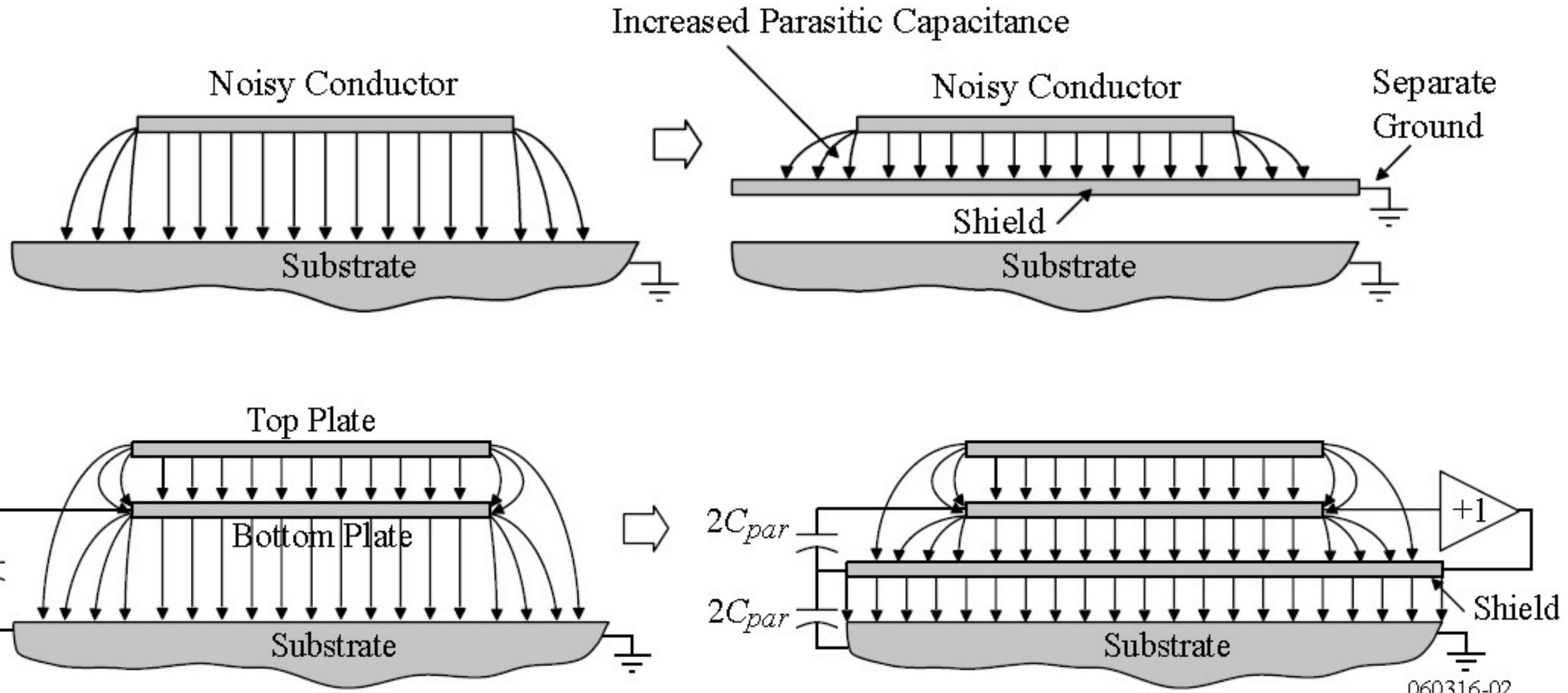
Sensitive to alignment errors in the upper and lower plates and loss of capacitance flux (smaller capacitance).



Insensitive to alignment errors and the flux reaching the bottom plate is larger resulting in large capacitance.

060207-09

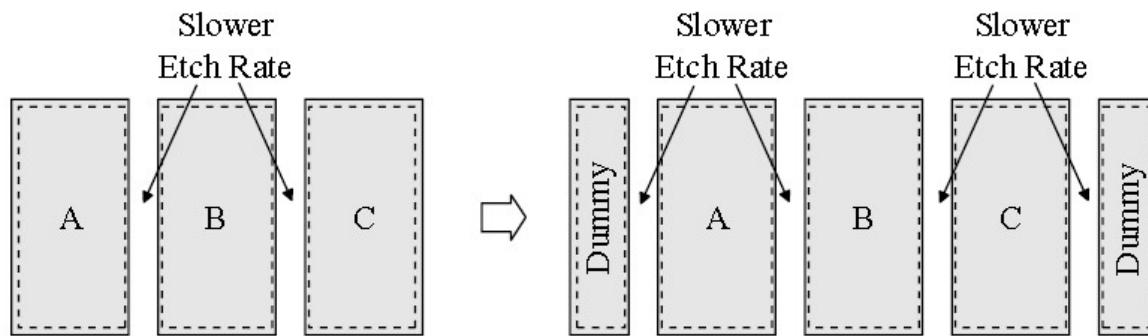
# Shielding



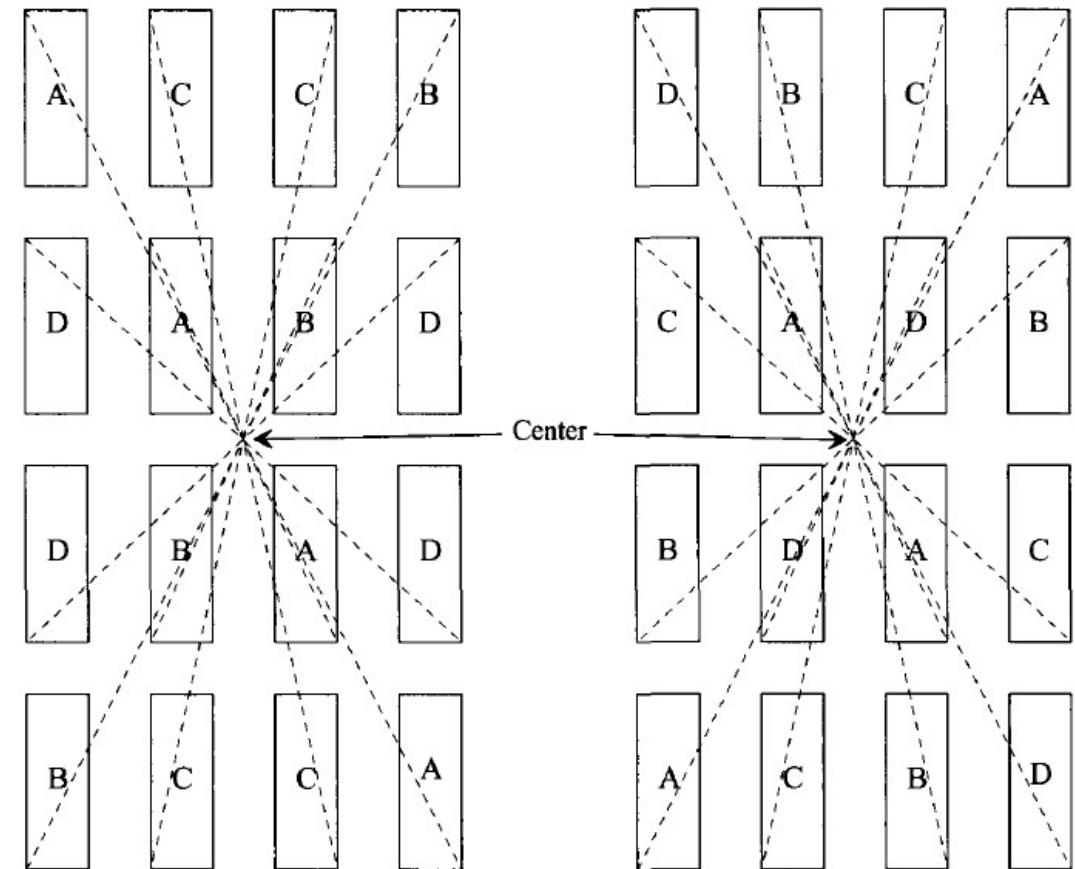
# Layout techniques for matching

## VARIATION

- Process → run-to-run
- Mismatch
  - Systematic → introduced by designers
  - Random
    - Line edge roughness
    - Gradients
    - Etch rate differences



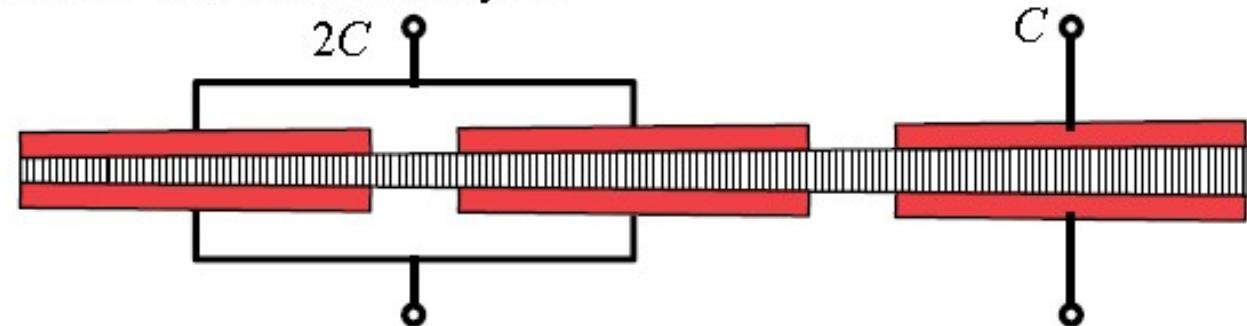
- The size of the area to be etched determines the etch rate
- Smaller areas allow less access to the etchant while larger areas allow more access to the etchant
- → dummy elements reduce this effect!



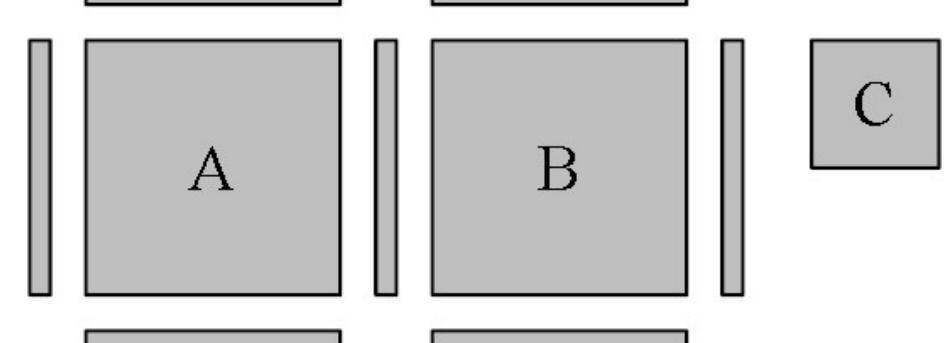
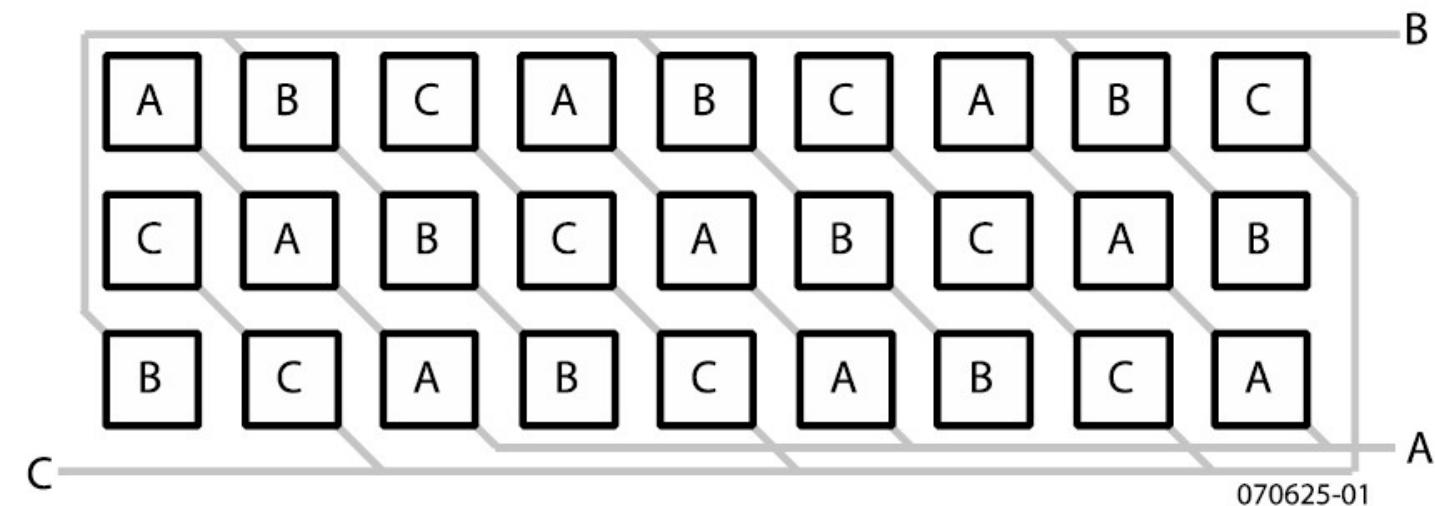
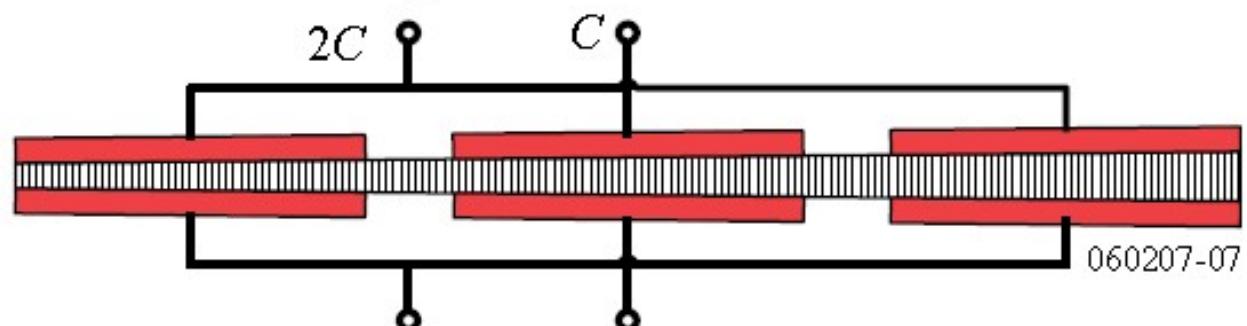
Common-centroid layout of four matched resistors (or capacitors)

# Oxide gradients + edge effects

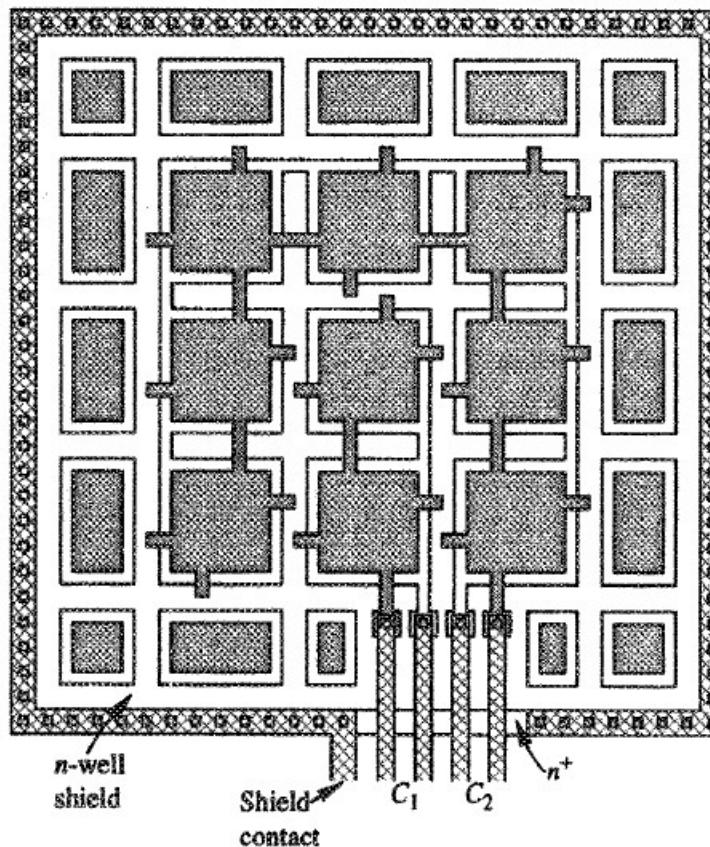
No common centroid layout



Common centroid layout



# Oxide gradients + edge effects

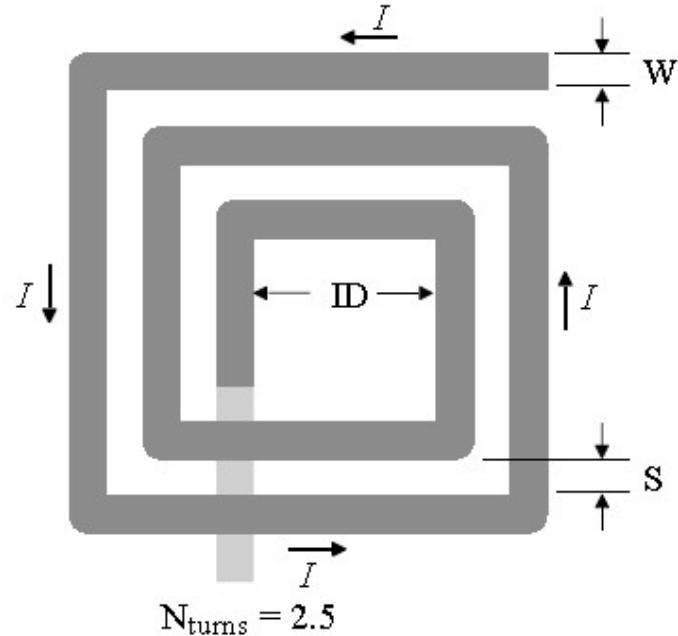


[Tsividis, 2002]

**Figure 6.17** A layout of two capacitors with ratio  $C_2/C_1 = \frac{1}{2}$ , incorporating several of the techniques discussed in the text (adapted from Ref. 23).

MORE INFO: R. Aparicio and A. Hajimiri, "Capacity limits and matching properties of integrated capacitors," in *IEEE Journal of Solid-State Circuits*, vol. 37, no. 3, pp. 384-393, March 2002, doi: 10.1109/4.987091.

# Inductors in CMOS technology



Ideally, the self inductance of an on-chip spiral inductor isolated from a ground plane can be approximated by

$$L = 2l \left\{ \ln \left( \frac{2l}{w+t} \right) + 0.5 + \frac{w+t}{3l} \right\}, \quad (1)$$

where  $L$  is the inductance in nH,  $l$ ,  $w$ , and  $t$  represent the length, width, and thickness of the conductor in cm,

$$\text{Quality factor, } Q = \frac{\omega L}{R}$$

- Planar inductor → self-inductance depends on geometry →  $L = 1-8\text{nH}$ ;  $Q = 3-6$  at 2GHz
- When  $1/f \sim$  dimensions, distributed model needed
- Note: bond wires can also be used as inductor →  $1\text{nH/mm}$  (2 to 5 nH in typical packages)

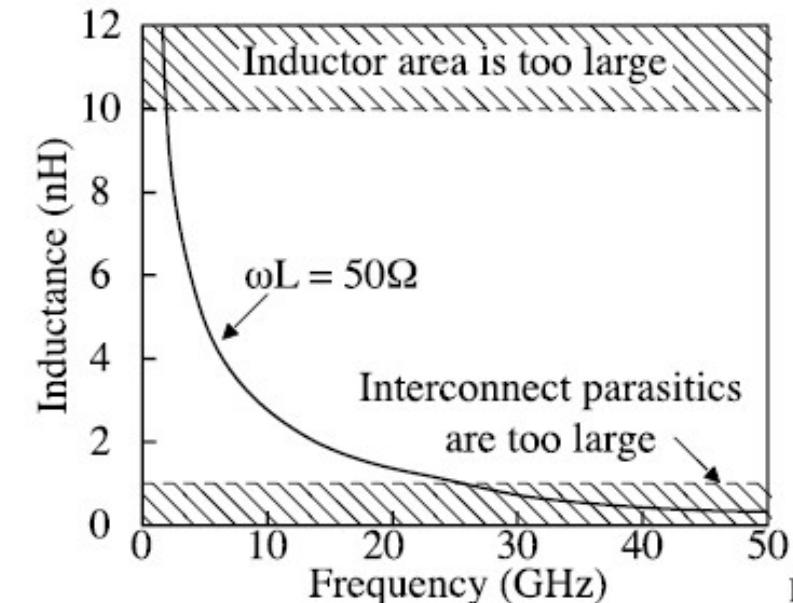
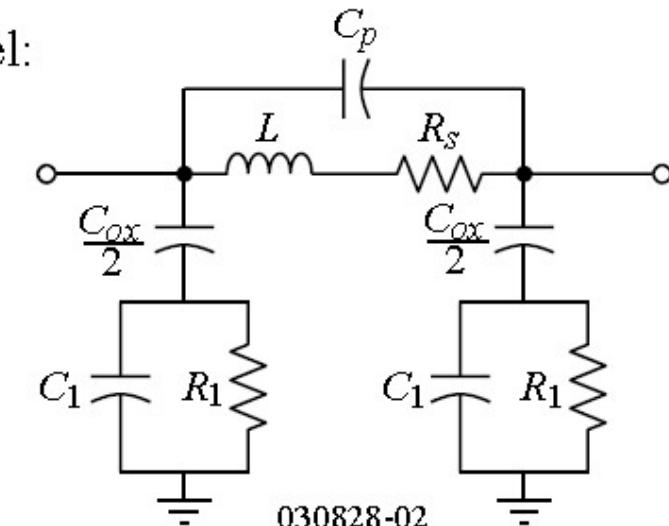


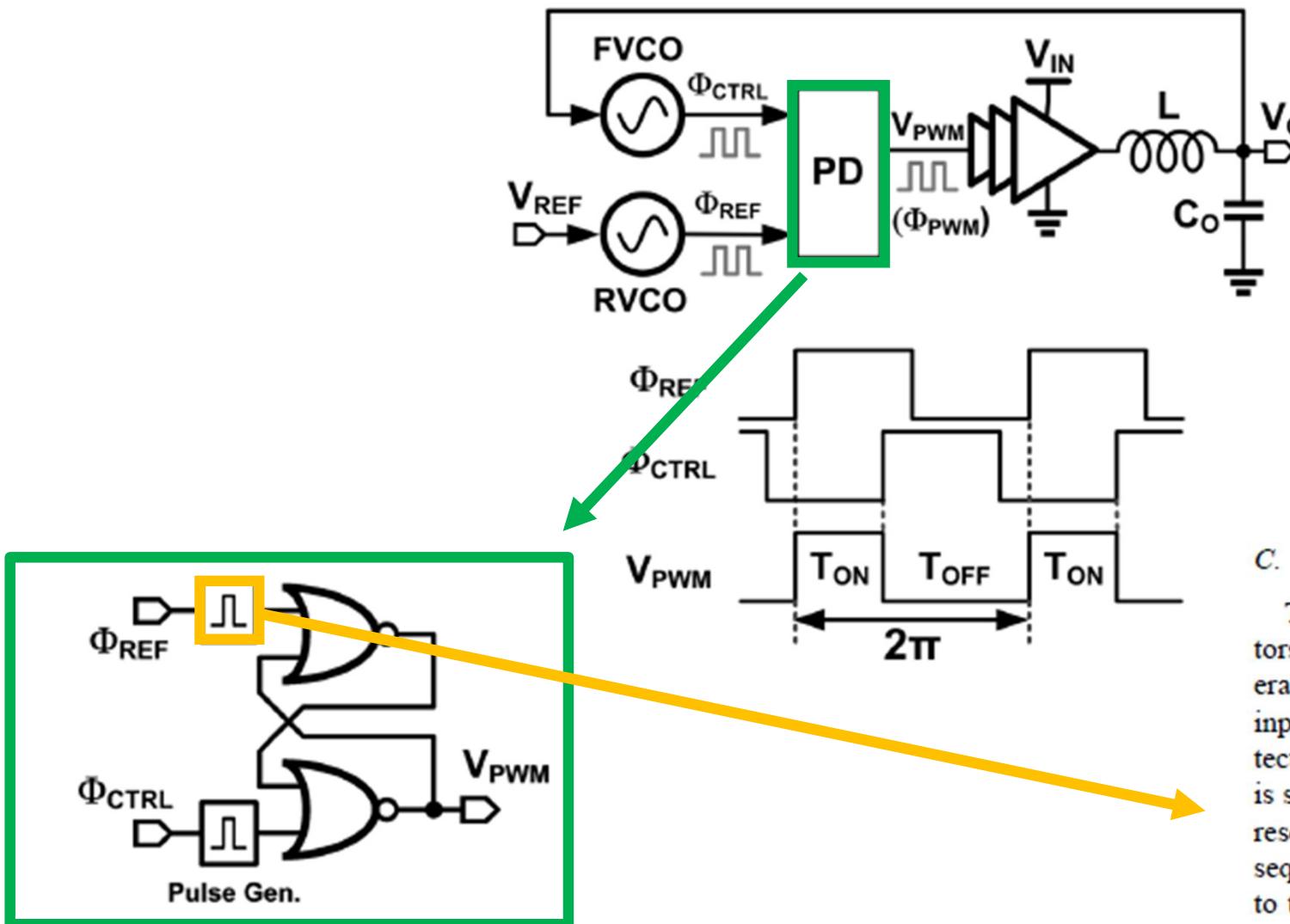
Fig. 6-5

Model:



# Single-pulse generator simulation

# Single-pulse generator in real design

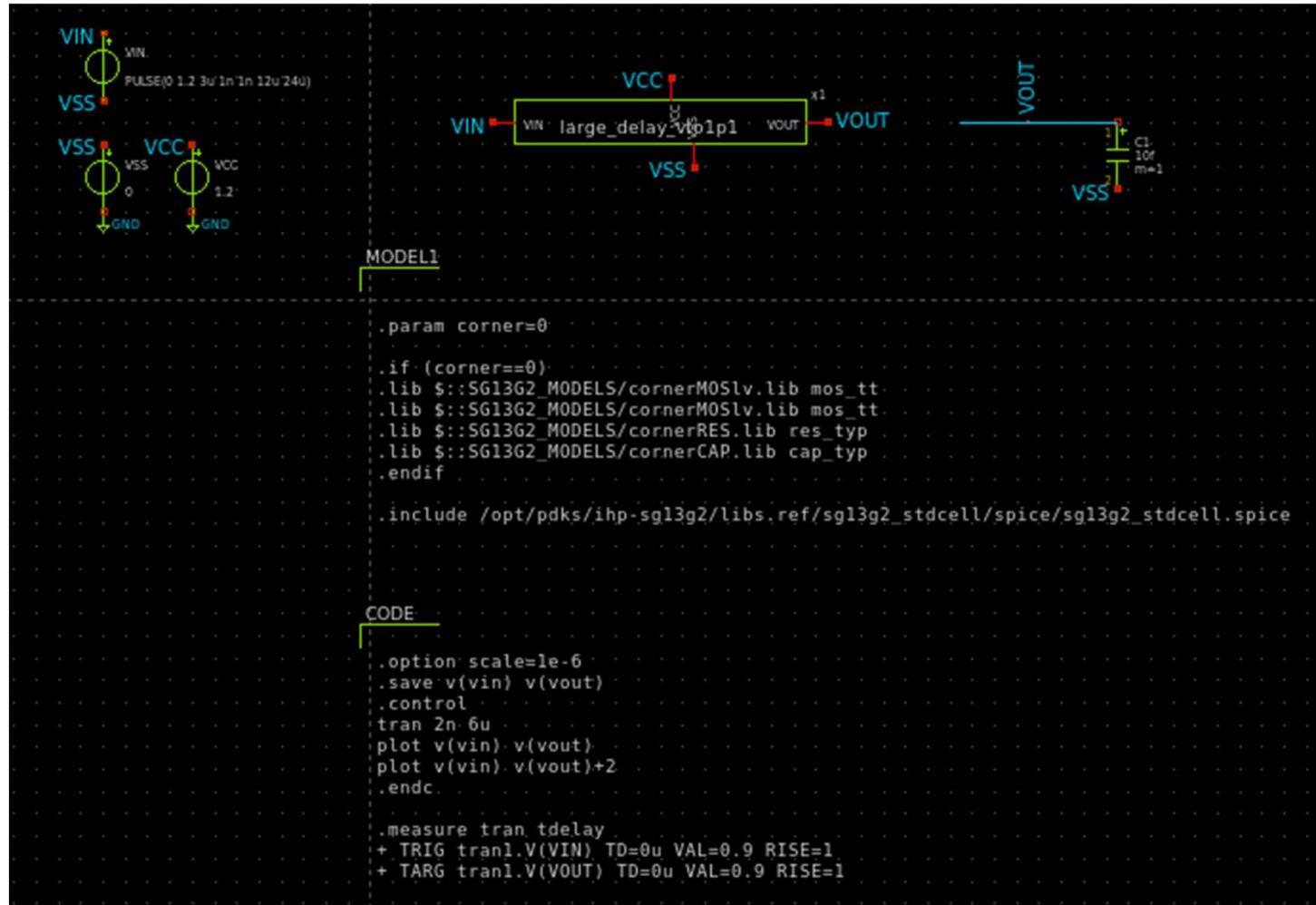


[Kim, JSSC 2015]

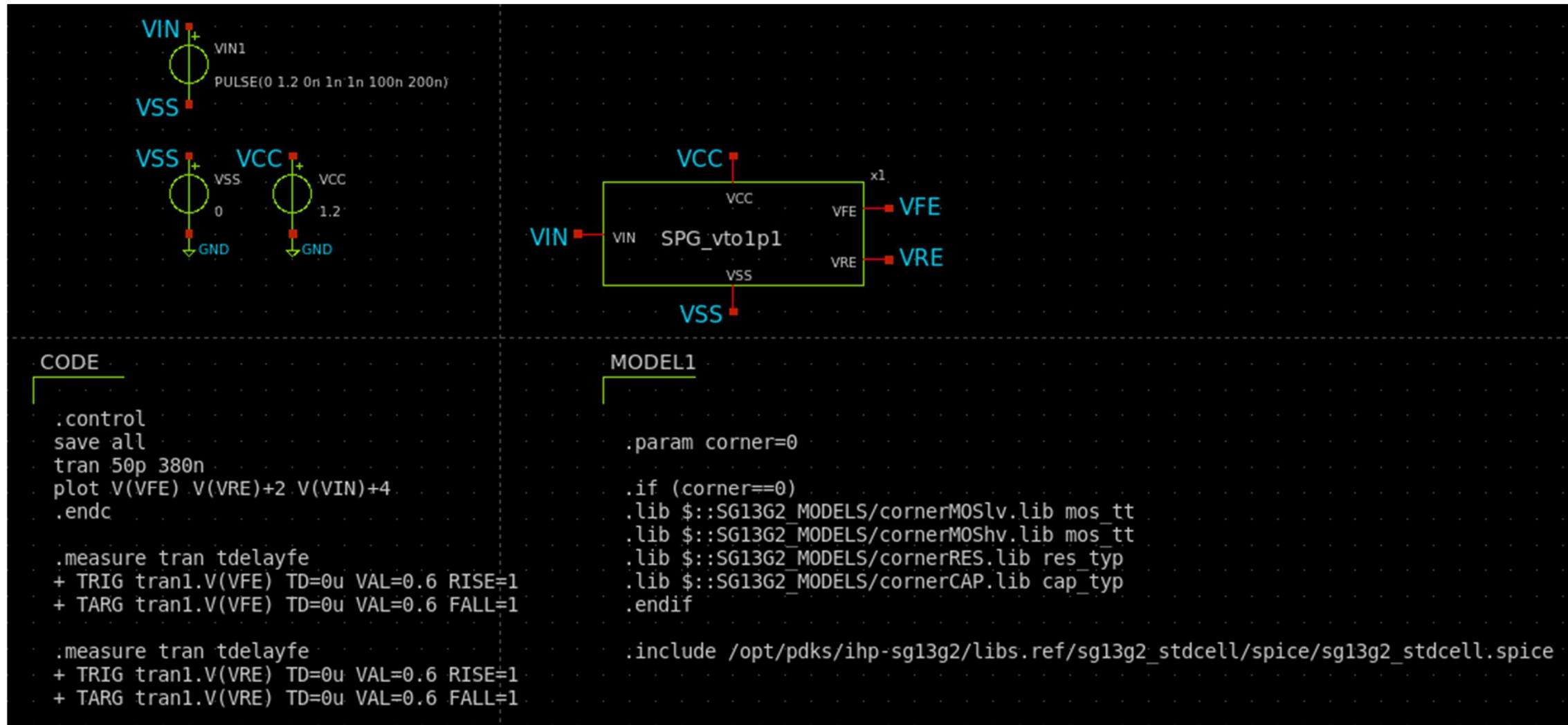
## C. Phase Detector

The phase detector is simply an RS latch with pulse generators at its inputs as shown in Fig. 18. The pulse generators generate narrow pulses on every positive edge transition of their inputs, resulting in RS flip-flop like behavior for the phase detector. The duty cycle of pulse width modulated signal,  $V_{PWM}$  is set at every positive edge of the reference phase,  $\Phi_{REF}$  and reset at every positive edge of the control phase,  $\Phi_{CTRL}$ . Consequently, the duty cycle of  $V_{PWM}$  waveform is proportional to the difference of two control phases. As mentioned before, this implementation of phase detector avoids use of an explicit PWM as the output of the phase detector is a digital waveform with CMOS levels carrying the necessary duty cycle information provided by control input phases.

# Testbench: large delay



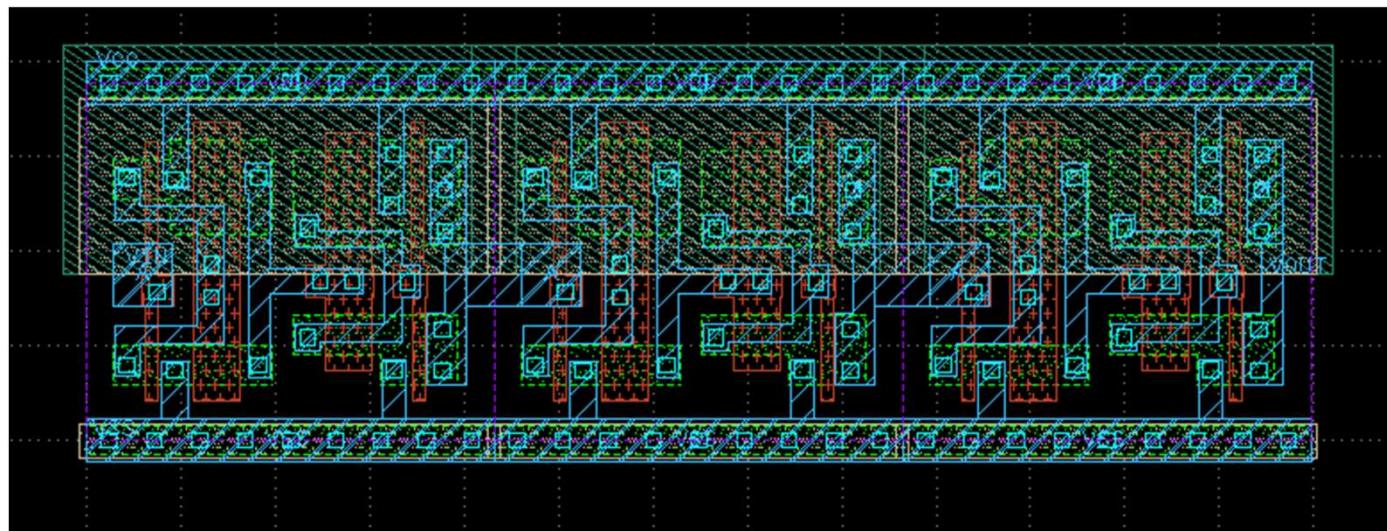
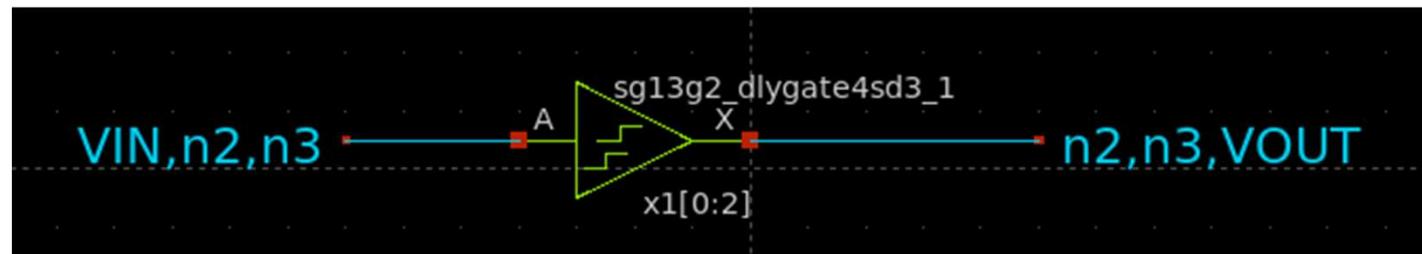
# Testbench: SPG



# Large delay layout

# Python-generated layout

- Macros → Macros development
- Import “add\_dly.py” & run
- Add connections and labels



# Modifications to schematic netlist

Open

large\_delay\_vtolp1.spice  
~/shared/OS\_AnalogIC\_UCU\_July2025/Day3/large\_delay/simulations

```
1 ** sch_path: /home/designer/shared/OS_AnalogIC_UCU_July2025/Day3/large_delay/large_delay_vtolp1.sch
2 .subckt large_delay_vtolp1 VCC VSS VIN VOUT
3 *.PININFO VIN:B VOUT:B VCC:B VSS:B
4 x1[0] VIN VCC VSS n2 sg13g2_dlygate4sd3_1
5 x1[1] n2 VCC VSS n3 sg13g2_dlygate4sd3_1
6 x1[2] n3 VCC VSS VOUT sg13g2_dlygate4sd3_1
7 .ends
8
9 * Library name: sg13g2_stdcell
10 * Cell name: sg13g2_dlygate4sd3_1
11 * View name: schematic
12 * Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
13 * pspice dspf
14 .subckt sg13g2_dlygate4sd3_1 A VDD VSS X
15 MP3 X net3 VDD VDD sg13_lv_pmos w=1.12u l=130.00n ng=1 ad=0 as=0 pd=0 ps=0 m=1
16 MP2 net3 net2 VDD VDD sg13_lv_pmos w=1.000u l=500.0n ng=1 ad=0 as=0 pd=0 ps=0 m=1
17 MP1 net2 net1 VDD VDD sg13_lv_pmos w=1.000u l=500.0n ng=1 ad=0 as=0 pd=0 ps=0 m=1
18 MP0 net1 A VDD VDD sg13_lv_pmos w=420.00n l=130.00n ng=1 ad=0 as=0 pd=0 ps=0 m=1
19 MN3 X net3 VSS VSS sg13_lv_nmos w=740.00n l=130.00n ng=1 ad=0 as=0 pd=0 ps=0 m=1
20 MN2 net3 net2 VSS VSS sg13_lv_nmos w=420.00n l=500.0n ng=1 ad=0 as=0 pd=0 ps=0 m=1
21 MN1 net2 net1 VSS VSS sg13_lv_nmos w=420.00n l=500.0n ng=1 ad=0 as=0 pd=0 ps=0 m=1
22 MN0 net1 A VSS VSS sg13_lv_nmos w=420.00n l=130.00n ng=1 ad=0 as=0 pd=0 ps=0 m=1
23 .ends
24 * End of subcircuit definition.|
```

gedit /opt/pdks/ihp-sg13g2/libs.ref/sg13g2\_stdcell/spice/sg13g2\_stdcell.spice &  
→ Find needed cell and copy .subckt definition

Task: customized single-pulse  
generator

# Task

- Modify the large\_delay cell to obtain pulses with width > 2ns
- Create a DRC+LVS passing layout for this circuit
- [extra] Create a layout for the full SPG

**Thank you!  
Questions?**