

# Open-Source IC Design Workshop

## 1.1 Introduction to open-source integrated circuit design

Jorge Marin N., PhD

Research Associate, AC3E-UTFSM

UCU, Montevideo, Uruguay – June 30, 2025

# Jorge Marin N.

## ➤ Academic Degrees

- Ph.D. in Electrical Engineering. KU Leuven, Belgium, 2018.
  - KU Leuven Doctoral fellowship + IWT-Flanders research project grant
- MsC degree in Electrical Engineering. KU Leuven, Belgium, 2012.
- BsC/MsC in Electrical Engineering. Universidad de Chile, Santiago, Chile, 2010.

## ➤ Work Experience

- Research Associate at Advanced Center for Electrical and Electronic Engineering (AC3E), USM, Valparaíso.
- Postdoctoral Research Fellow at AC3E-USM, Valparaíso, Chile, 2022-2023.
- Analog Designer Sony Depthsensing Solutions 2020 – 2021.
- Analog Designer ICsense (TDK) 2018 – 2020.
- Engineer Intern/ Engineer Synopsys R&D Center Santiago, Chile 2006 - 2009.
- Lecturer and TA, 2008 - 2025
  - Universidad de Chile, Universidad de los Andes (Chile), KU Leuven, USM
  - Digital Systems, Analog Integrated Circuit Design, Analog IC Design Lab

## ➤ Other roles

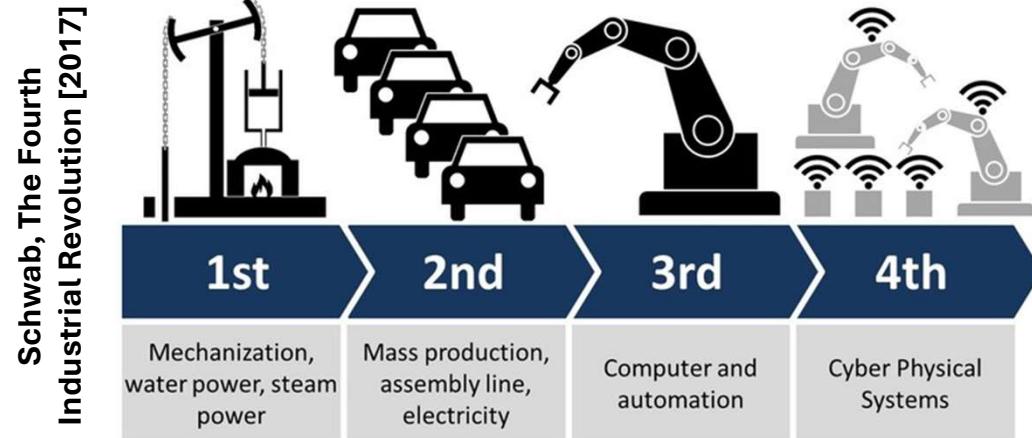
- IEEE CASS/SSCS/EDS joint chapter chair
- IEEE CICC TPC member
- UNIC-CASS educational program team lead



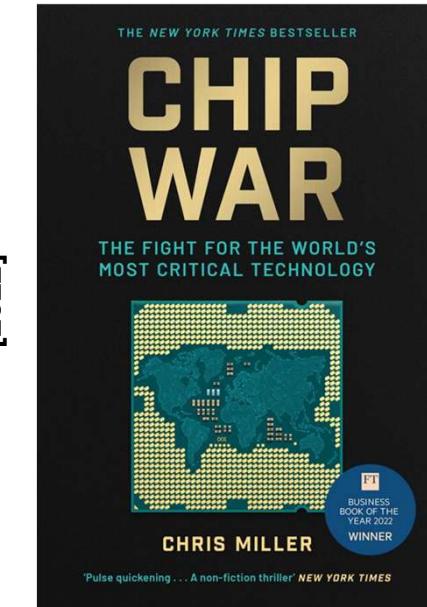
# Introduction

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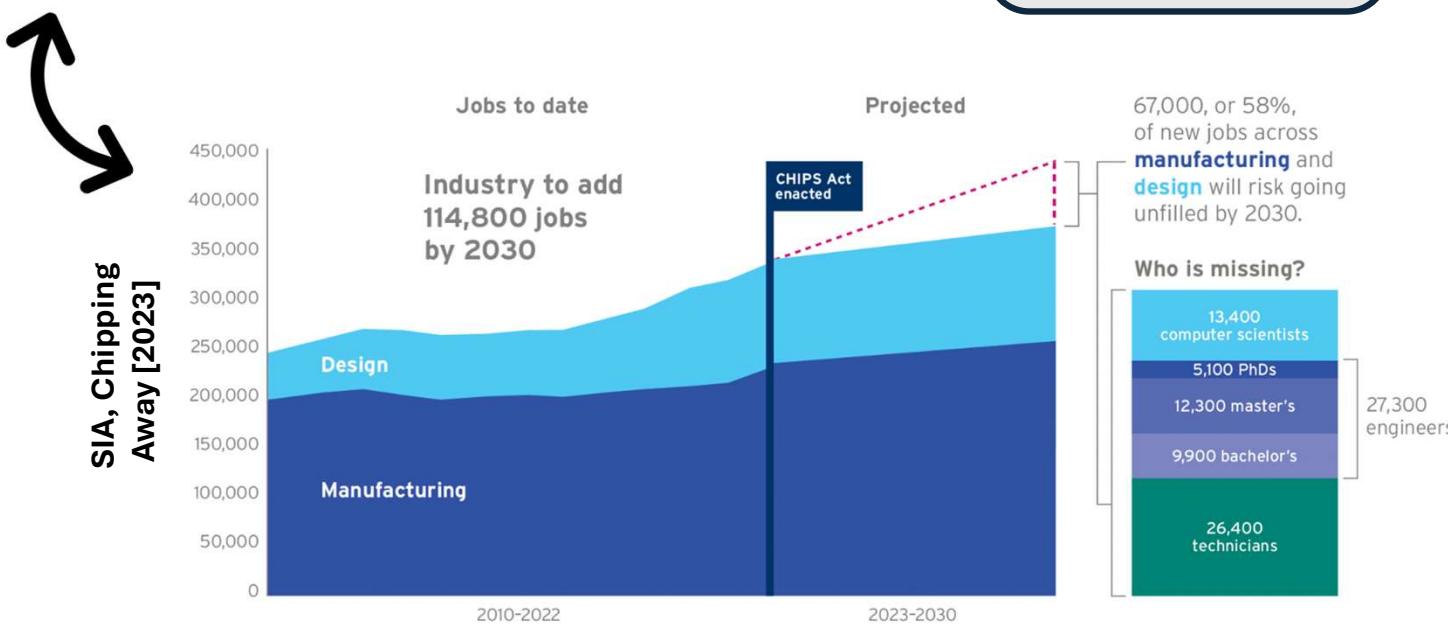
## Why chips matter today?



High demand for complex chips  
→ exponential technologies



Geopolitical context → chips are the new oil!



Workforce crisis  
→ CS is (way) more interesting than EE

# Introduction

“Harder/better/faster/stronger”

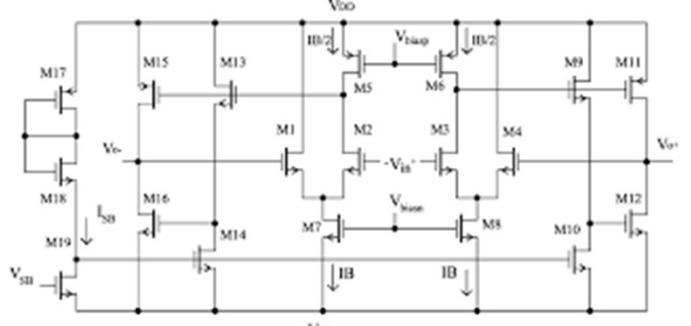
→ We need to

- Design more chips
- Make them more complex, reliable and robust
- Do this with less engineers

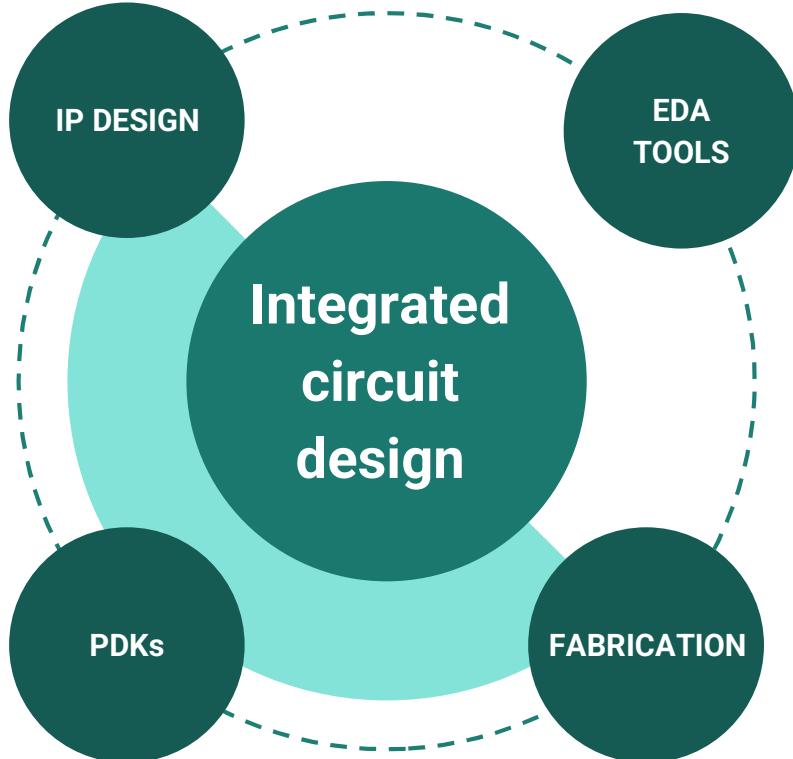
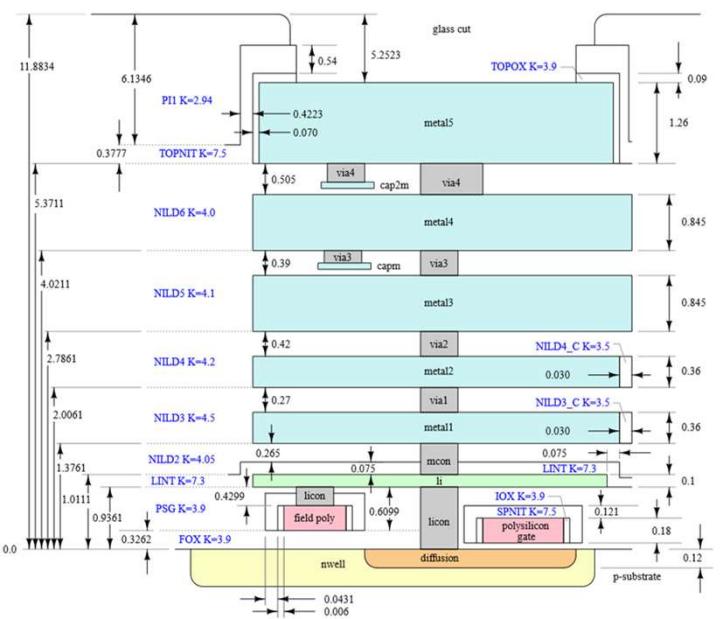
**The current IC design ecosystem is not keeping the pace!**

# Introduction

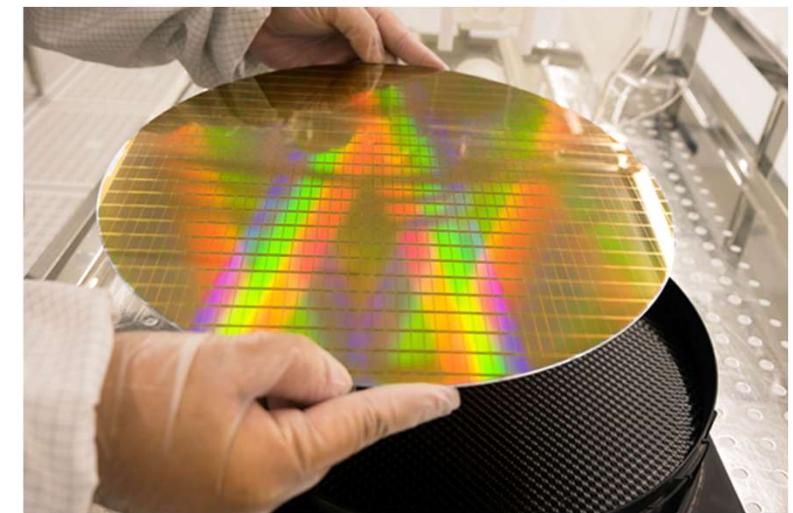
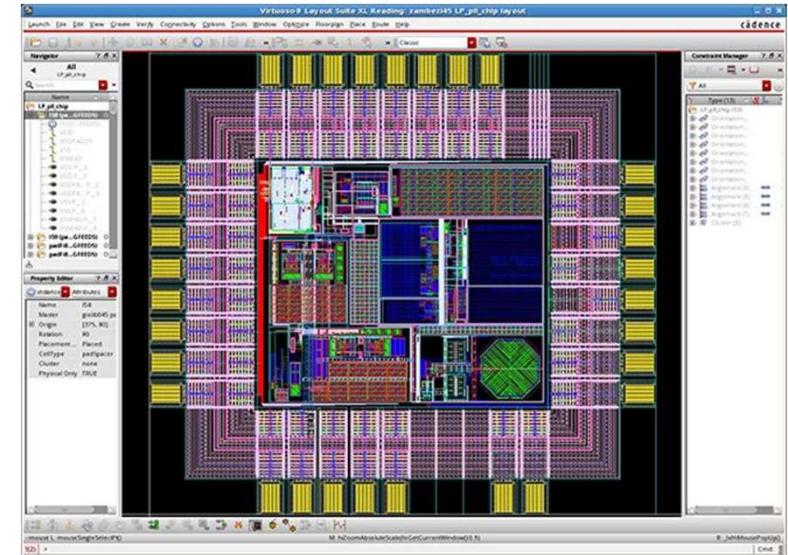
## Why Open-Source IC design?



(Diagram not to scale!)

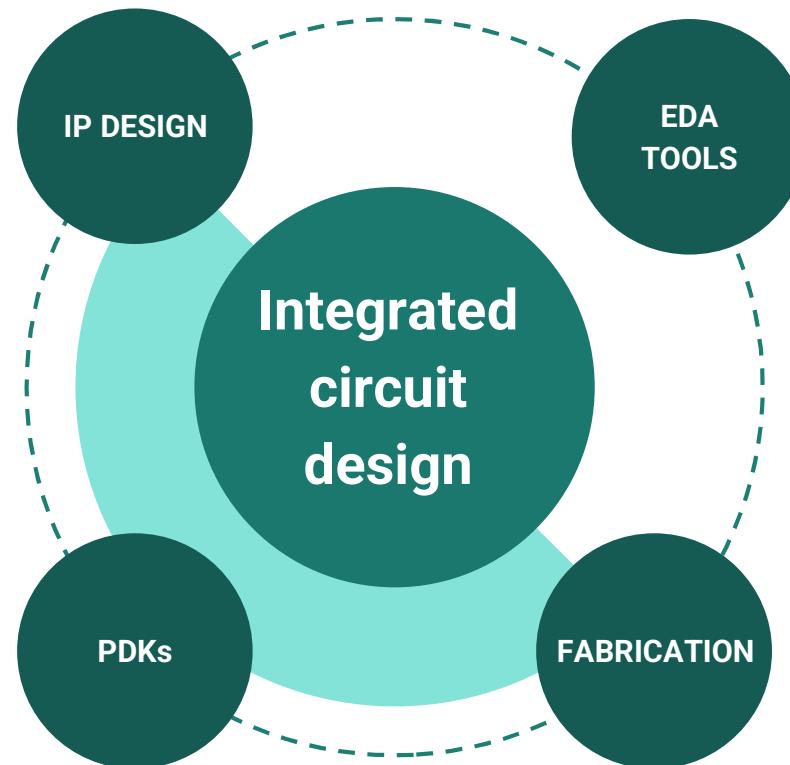
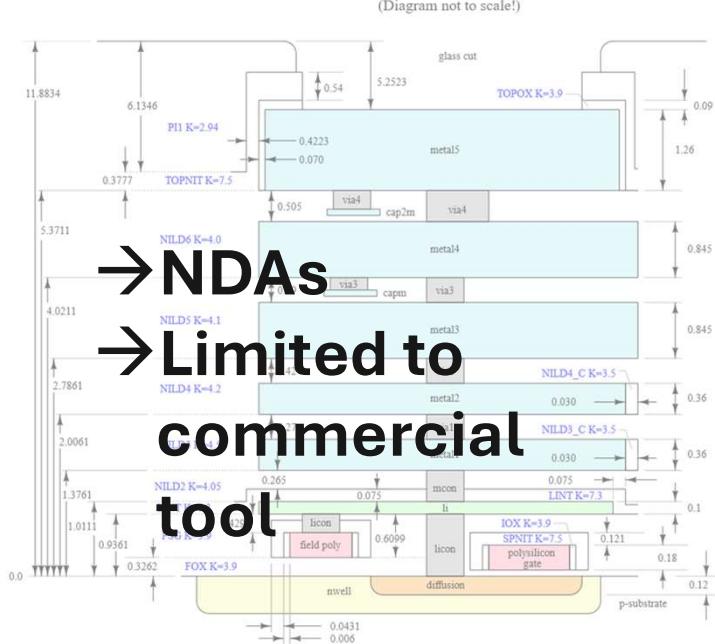
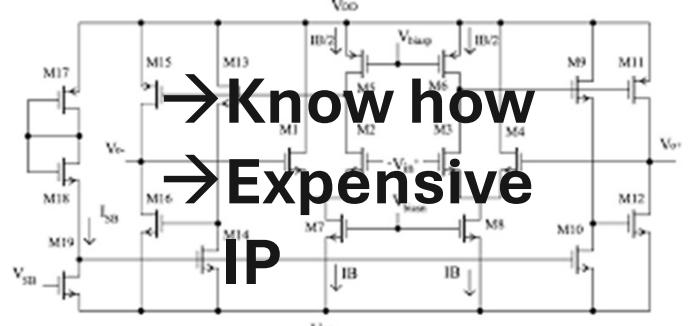


[Tim Ansell, FOSSI Dial-Up2020]

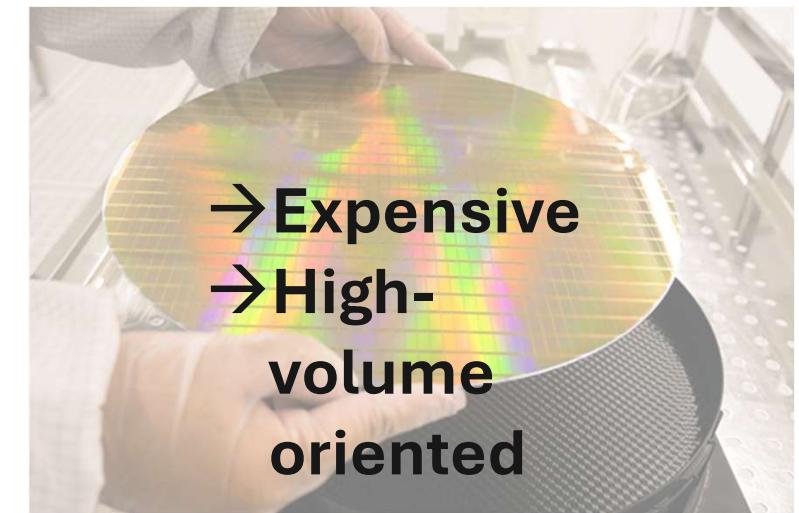
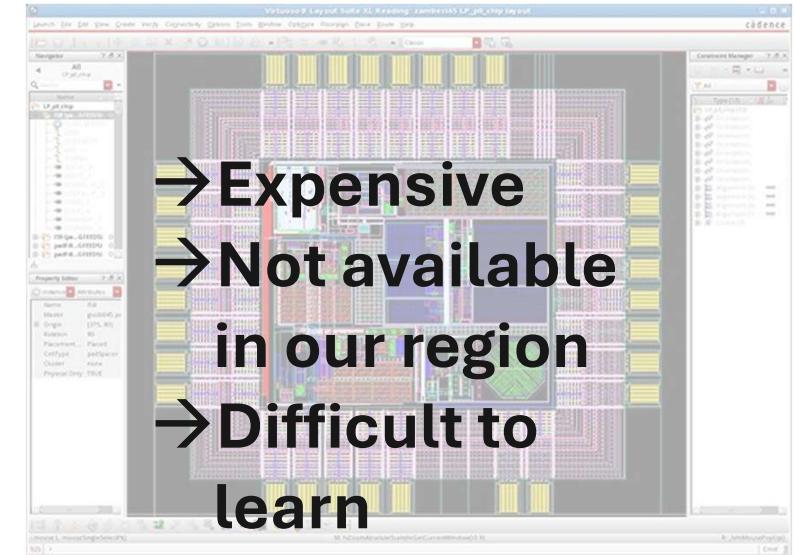


# Introduction

## Why Open-Source IC design?



[Tim Ansell, FOSSi Dial-Up2020]



# Introduction

## Concern and Chips Acts

The New York Times

### America's Semiconductor Boom Faces a Challenge: Not Enough Workers

Strengthened by billions of federal dollars, semiconductor companies plan to create thousands of jobs. But officials say there might not be enough people to fill them.

Le Monde

« Une partie des candidats qu'on cherche n'existent pas » : une entreprise face aux difficultés de recrutement

Les difficultés d'embauche du fabricant de semi-conducteurs X-Fab révèle combien la question est complexe.

EE Times  
EUROPE

News Analysis

Focus ▾

Opinion

Education ▾

Magazine ▾

Company

News Analysis Trends

### Europe's Semiconductor Talent Gap Widens

# Introduction

## Concern and Chips Acts

### Exploring the 2022 CHIPS and Science Act

Ensuring increased U.S.-based production  
and improved supply chain resiliency of  
semiconductor technology

**\$52.7 Billion in New  
Funding for Semiconductors**

**U.S. Chips and  
Science Act**



### EU Chips Act

*The EU chips act aims to:*

- ensure **large-scale capacity building** and **innovation** within the EU
- ensure that the EU is **self-supplying** to a much greater extent
- ensure that the EU can **react quickly** in the event of supply crises



In total, more than €43 billion of policy-driven investment will support the Chips Act until 2030, which will be broadly matched by long-term private investment.

# Introduction

## Concern and Chips Acts? (2025 update)

### Trump renegotiating Biden-era Chips Act grants, Lutnick says

By Reuters

June 4, 2025 11:39 PM GMT-4 · Updated June 4, 2025

Economy | Technology

### Trump tells US chip design software makers to halt China sales: Report

*US electronic design automation software makers were told via letters to stop supplies to China, the FT reported.*



### The European Chips Act has no clothes

Opinion | May 3, 2025

By Peter Clarke

EUROPEAN CHIPS ACT

ANALOG

ARTIFICIAL INTELLIGENCE

SEMICONDUCTOR

AUTOMOTIVE

# Introduction

## Concern and Chips Acts? (2025 update)

B B C

### The secretive US factory that lays bare the contradiction in Trump's America First plan

18 May 2025

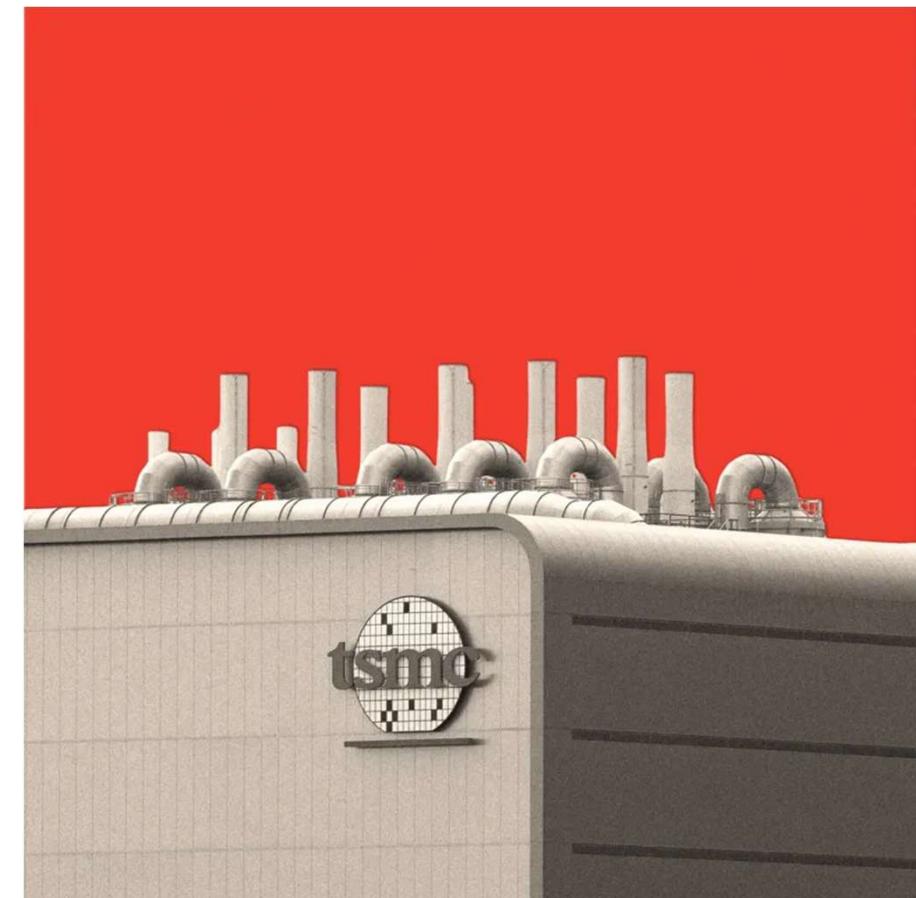


Faisal Islam

Economics editor • [@faisalislam](#)

Reporting from Arizona

Share Save

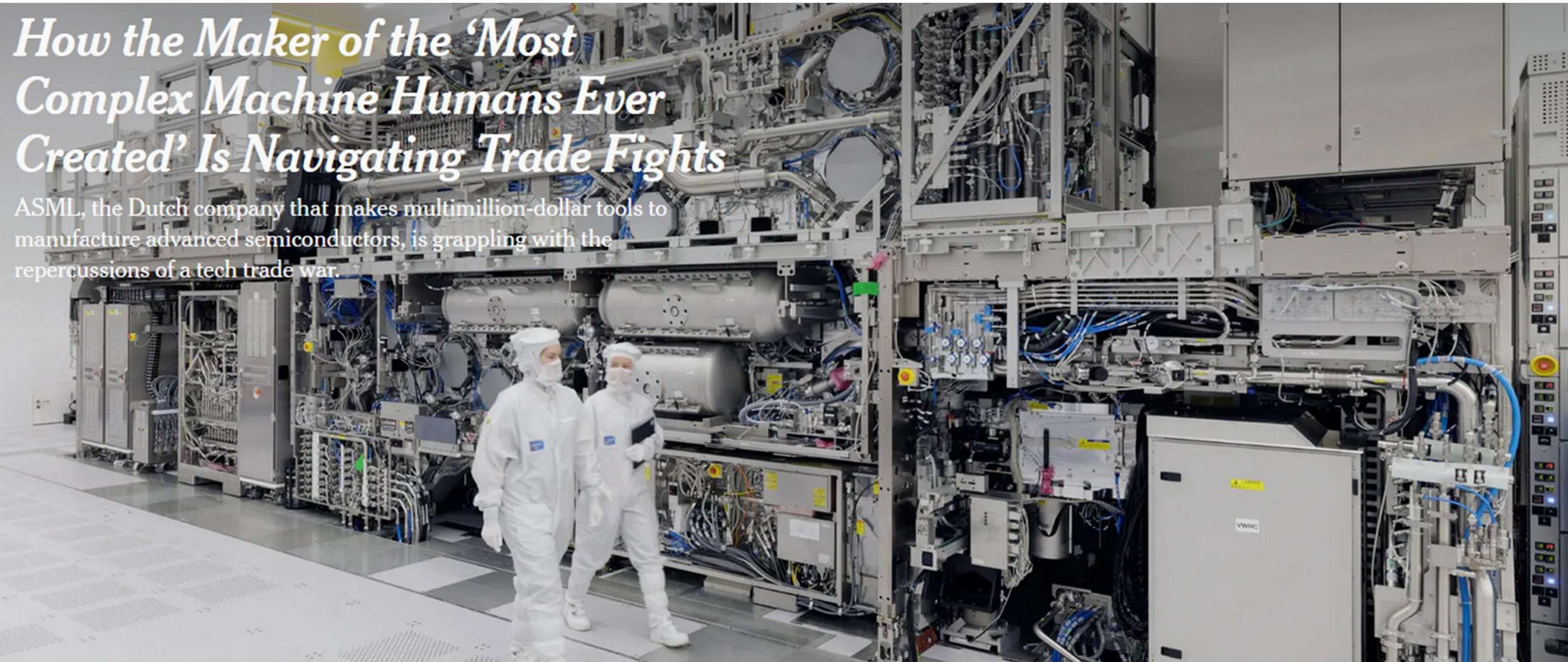


# Introduction

## Concern and Chips Acts? (2025 update)

*How the Maker of the ‘Most Complex Machine Humans Ever Created’ Is Navigating Trade Fights*

ASML, the Dutch company that makes multimillion-dollar tools to manufacture advanced semiconductors, is grappling with the repercussions of a tech trade war.



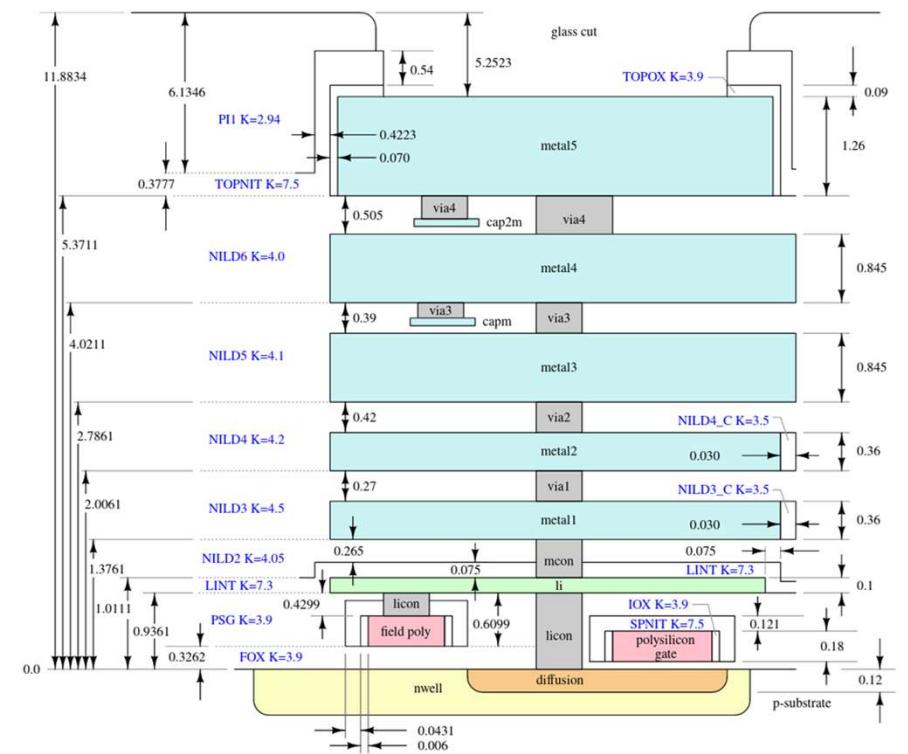
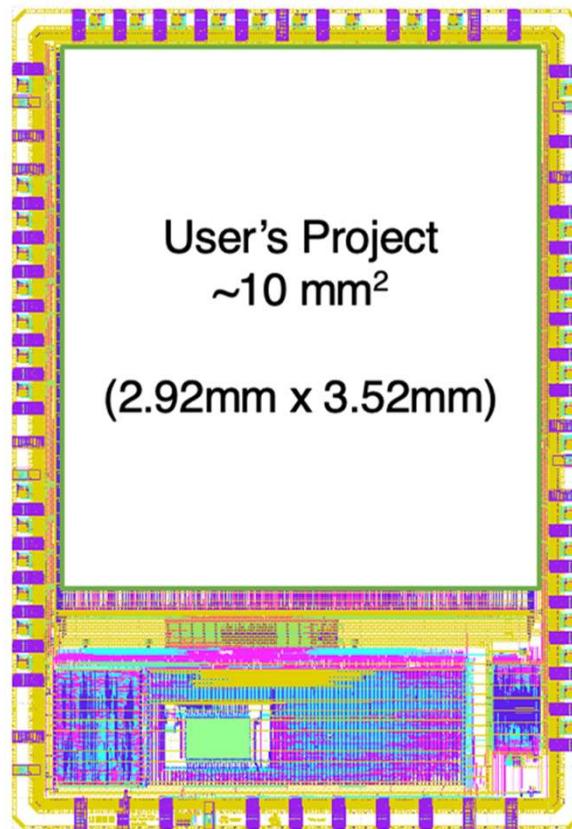
# Open-Source Silicon Approach

# Open-Source Silicon Approach

# The OS approach: open SKY130 PDK (2020)

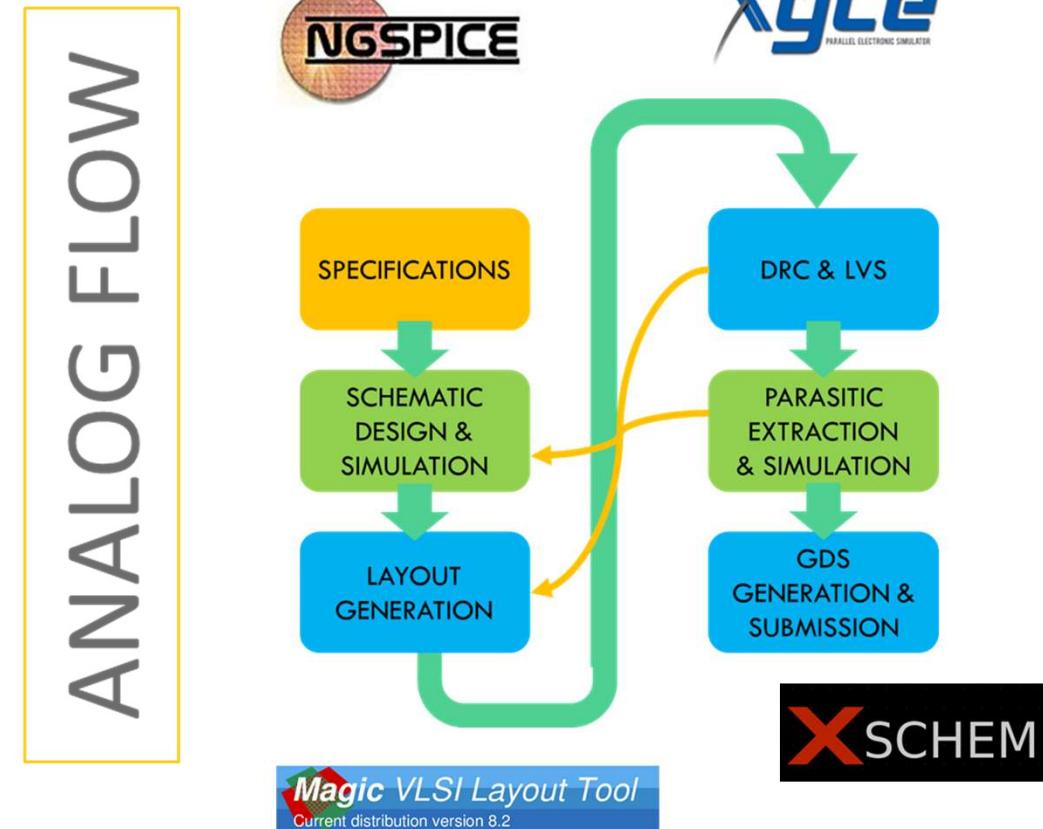
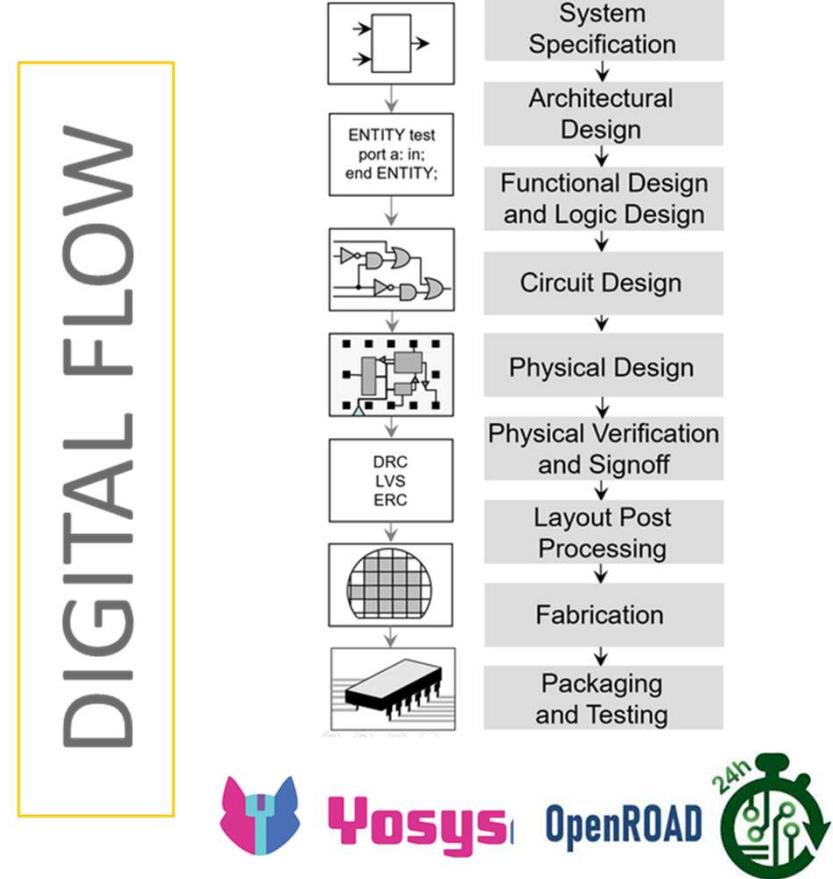


# **Caravel/ Caravan chip harness**



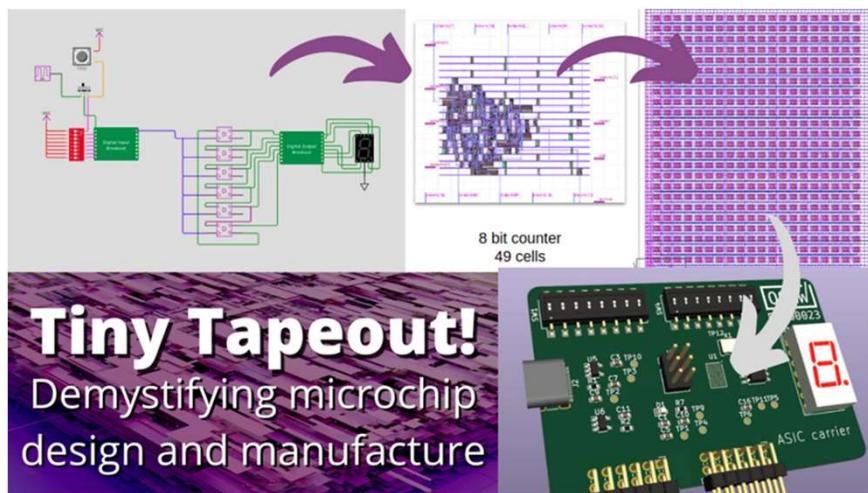
# Open-Source Silicon Approach

The OS approach: opensource EDA/CAD software



# Open-Source Silicon Approach

## The OS approach: affordable silicon



### Welcome to IHP-Open-DesignLib documentation!

IHP-Open-DesignLib is repository, which contains open source IC designs using IHP SG13G2 BiCMOS processs. It is also a central point for design fabrication under the concept of IHP Free MPW runs funded by a public German project [FMD-QNC \(16ME083\)](#). Project funds can be used exclusively to produce chip designs for non-commercial activities, such as university education, research projects, and others. In the project, a continuation for the provision of free area for the open source community is to be worked out.

11 Nov 2024	22 Nov 2024	07 Apr 2025	09 May 2025	18 Jul 2025	15 Sep 2025
SG13CMOS 220	SG13G2 20	SG13G2 140	SG13G2 30	SG13G2 30	SG13CMOS 220



Chip Design, Fabrication and Bring-up for  
Product Companies, Startups and  
university programs

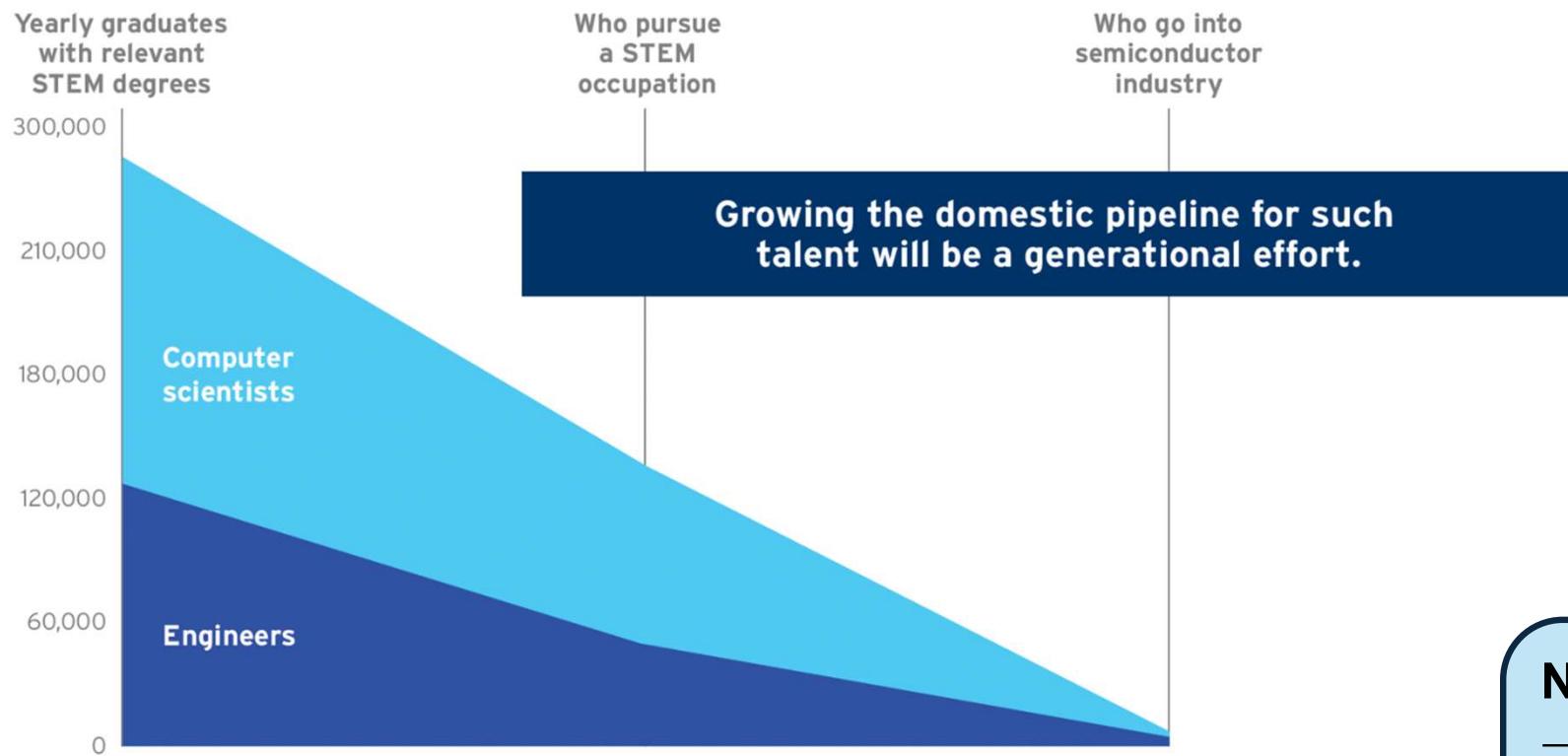
**\$14,950** per tapeout

The ChipCreate offering includes:

- Pre-built SoC design with RISC-V subsystem and peripherals
- Up to 15mm<sup>2</sup> of die space with a standard I/O ring
- 38 fully -configurable I/Os supporting both digital and analog signaling
- Option of 100 QFN-packaged parts or Bare Die
- Plug and play development board with software support
- Complete RTL-to-GDSII Open Source design flow

# Open-Source Silicon Approach

## The OS approach: low barriers for new designers



**USA career choice**  
CS → 830.000  
EE → 70.000

**Nearterm solution**  
→ Attract international talent

**New skills in designers:**  
→ Analog + digital background  
→ AI/ML knowledge  
→ Programmatic/systematic design skills

Source: <https://www.semiconductors.org/chipping-away-assessing-and-addressing-the-labor-market-gap-facing-the-u-s-semiconductor-industry/>

# Open-Source Silicon Approach

The OS approach: low barriers for new designers

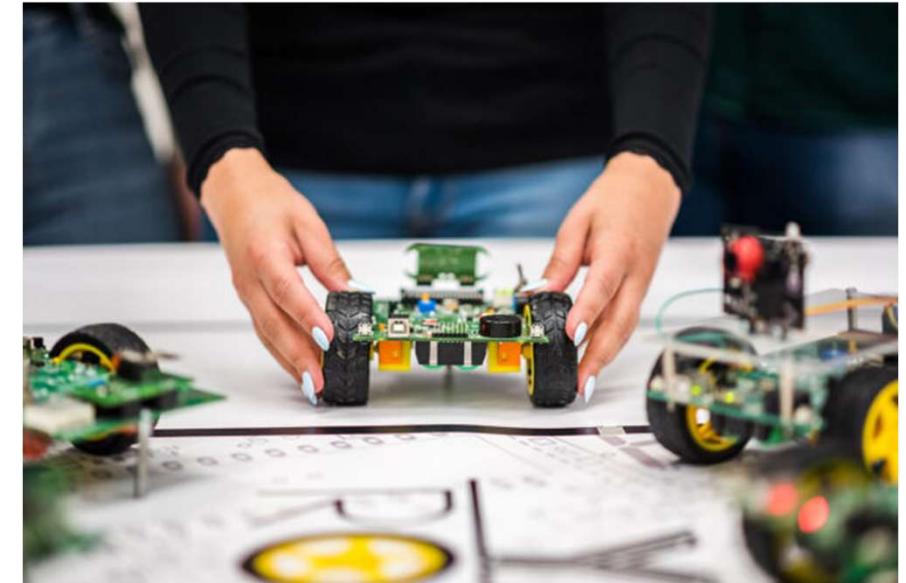


# Open-Source Silicon Approach

The OS approach: low barriers for new designers



Makers' philosophy: do it yourself



The IC design workflow is  
conservative  
→ need for openness and  
collaboration!



# Open-Source Silicon Approach

Industrial initiatives for OS silicon education



SUMMERSCHOOL 2023  
18-22 SEPTEMBER

## AnaGen

Next level  
chip design!



Certificate Course: Analog Design with IHP SG13G2  
Open-Source PDK

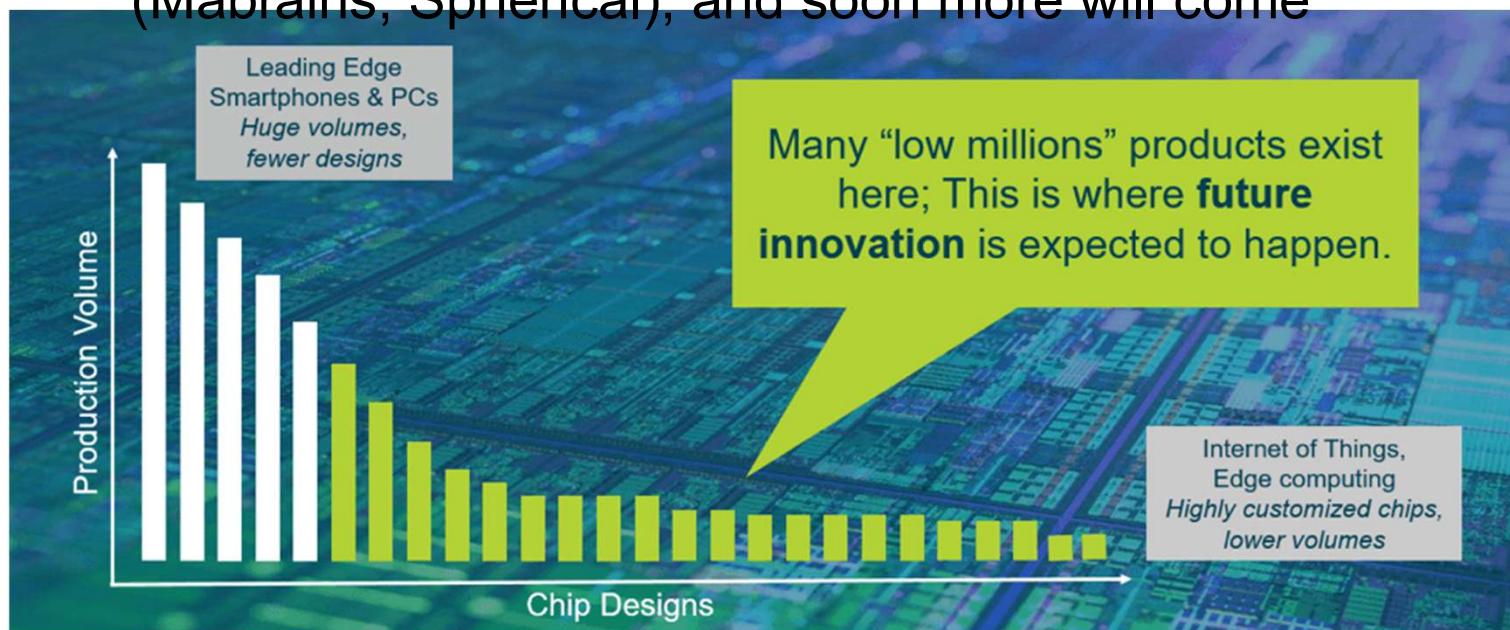
# cadence®

Cadence and SkyWater: Fostering  
the Next Generation of Innovators

# Open-Source Silicon Approach

## Industry: why to care about opensource?

- Some pioneer companies are starting to build their business models around open source silicon movement
- Mostly focused on education, OS EDA and enabling chip design for low-volume projects
- But some of them are already working on design (Mabrain, Spherical), and soon more will come



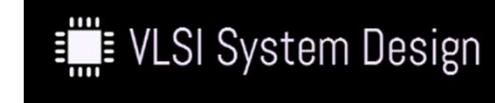
Source: <https://www.skywatertechnology.com/sky130-open-source-pdk/>



Zero to ASIC



Tiny Tapeout



Mabrain



# Research in OSIC design

# Research in OSIC design

New capabilities are enabled by OS silicon

- No restriction to expose PDK parameters
- No restriction in the number of EDA tool licenses
- EDA tools can be customized
- Open data
  - Replicability/reusability
  - AI-based generators

# Previous research: analog/mixed signal IC design

Jorge Marin

Compact and robust time-based CMOS sensor interface



**KU LEUVEN**

ARENBERG DOCTORAL SCHOOL  
Faculty of Engineering Science

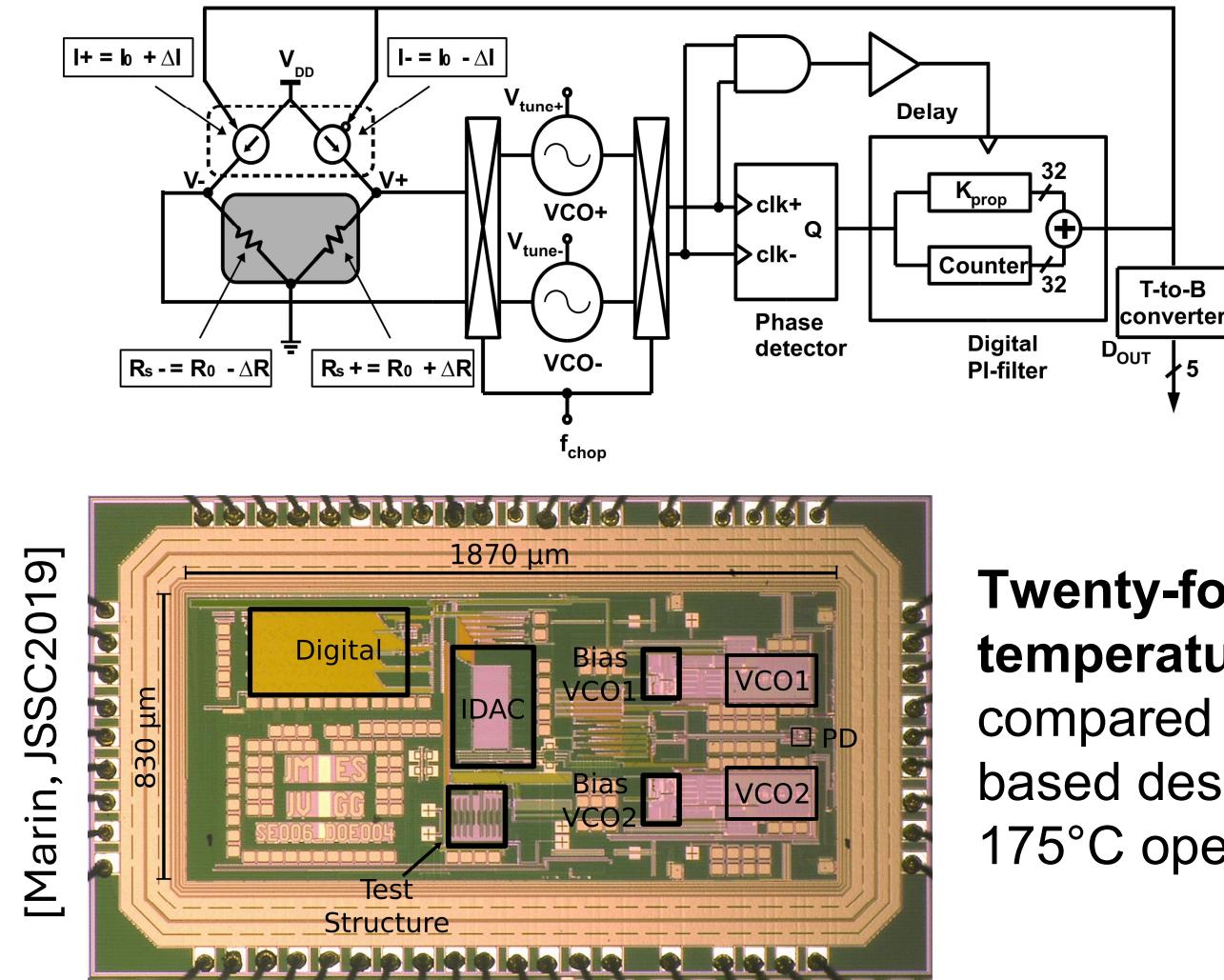
Time-Based Techniques for  
the Design of Area-Efficient  
and Robust CMOS Sensor  
Interface Circuits

Jorge Marin

Supervisors:  
Prof. dr. ir. G. Gielen  
Prof. dr. ir. W. Dehaene

Dissertation presented in partial fulfillment of the requirements for the degree of Doctor of Engineering Science (PhD): Electrical Engineering

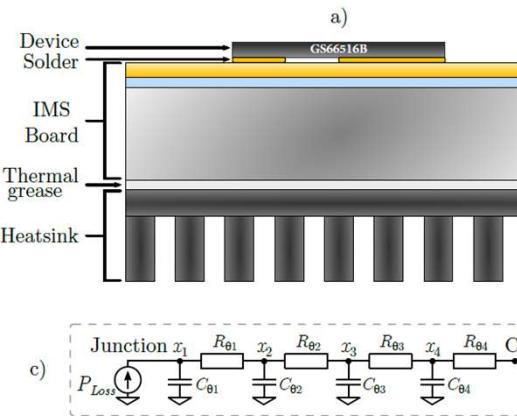
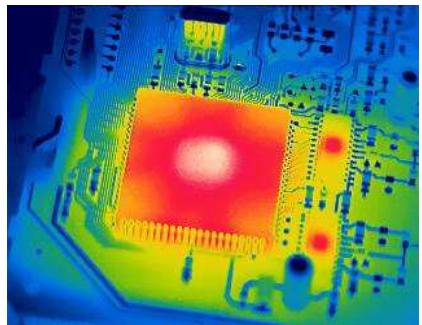
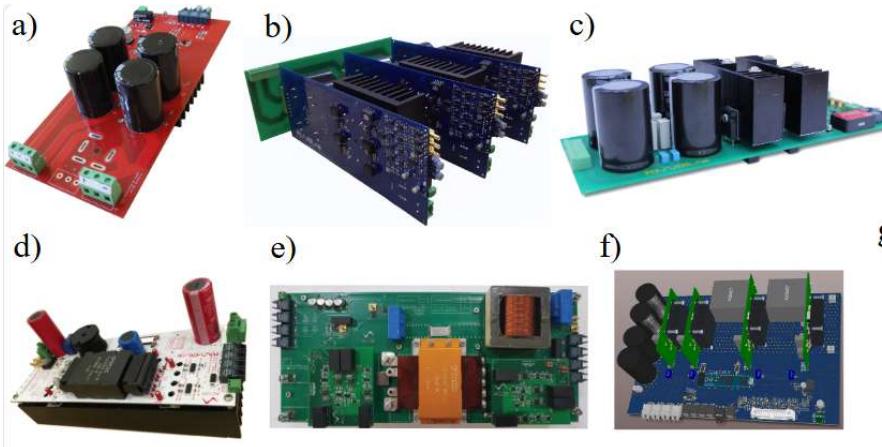
September 2019



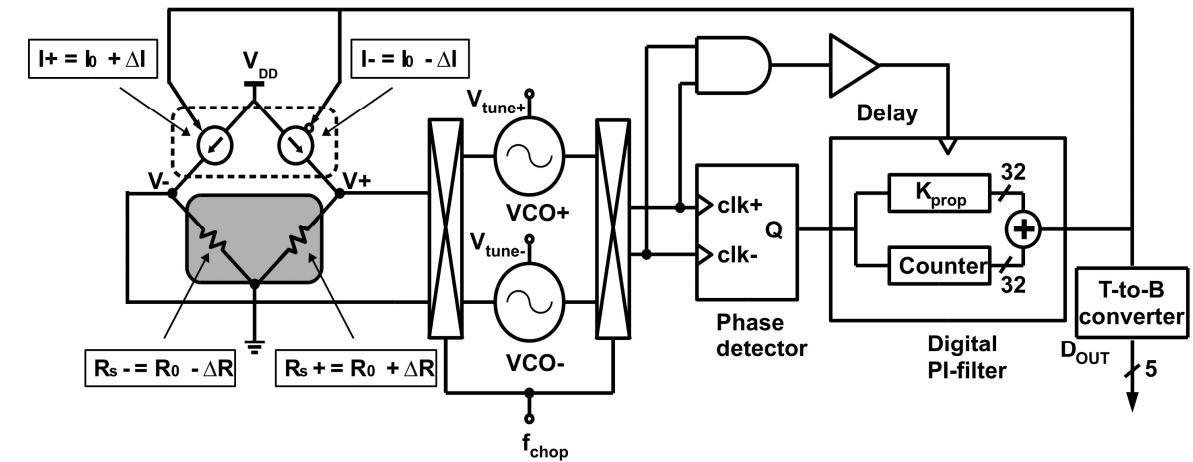
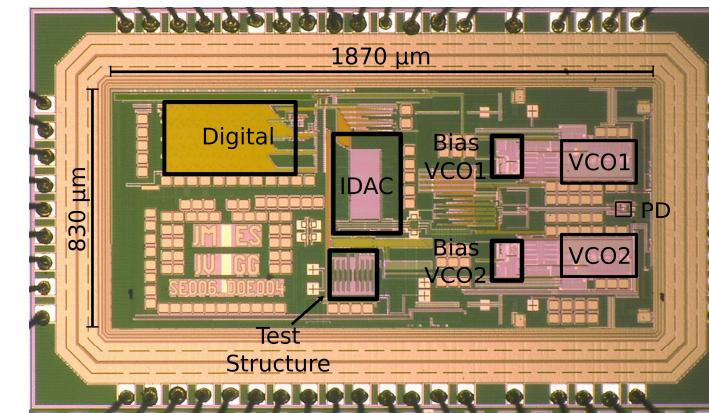
**Twenty-fold higher temperature drift resilience** compared to previous time-based designs in the -40°C to 175°C operating range.

# IC Design meets Power Electronics

Power electronics meet integrated circuits

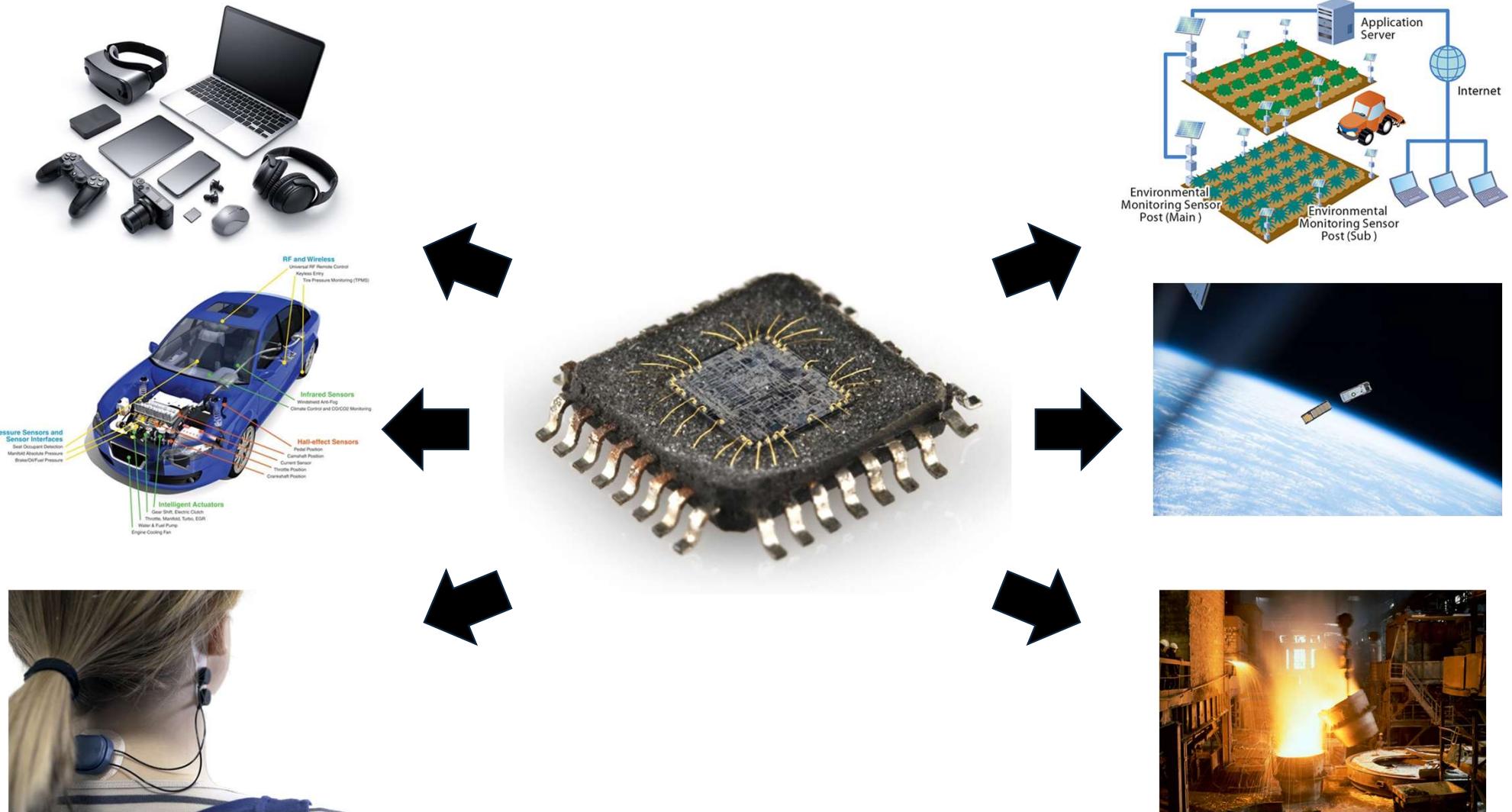


[Rojas et al.,  
IECON2021]



[Marin et al.,  
JSSC2019]

# IC Design meets Power Electronics

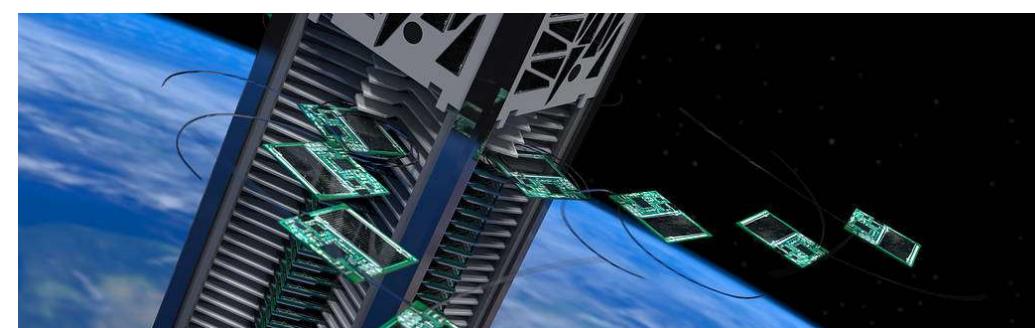
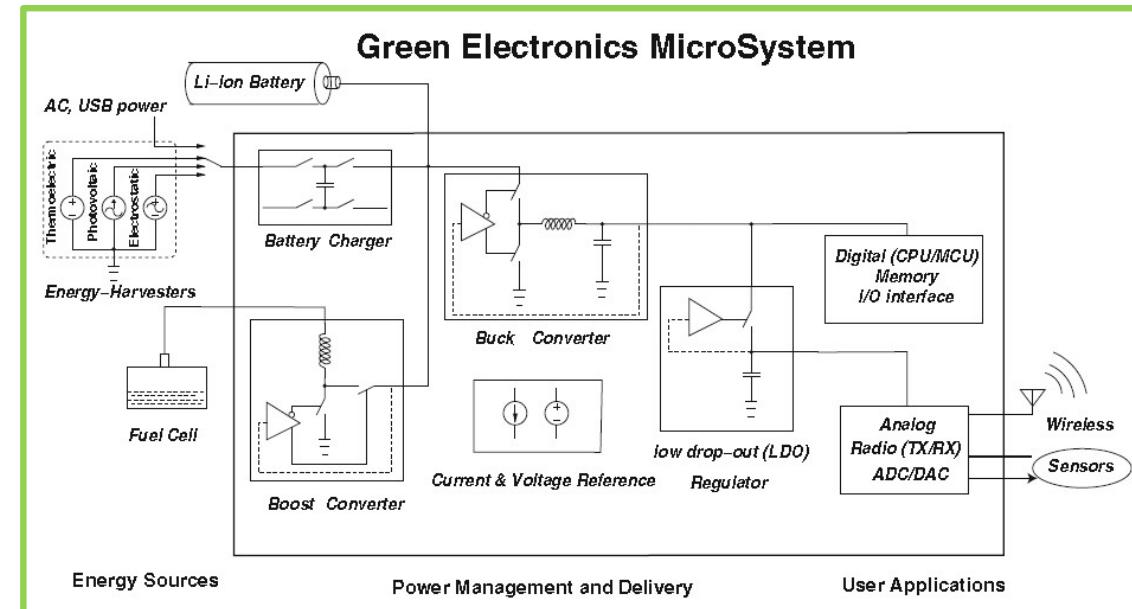
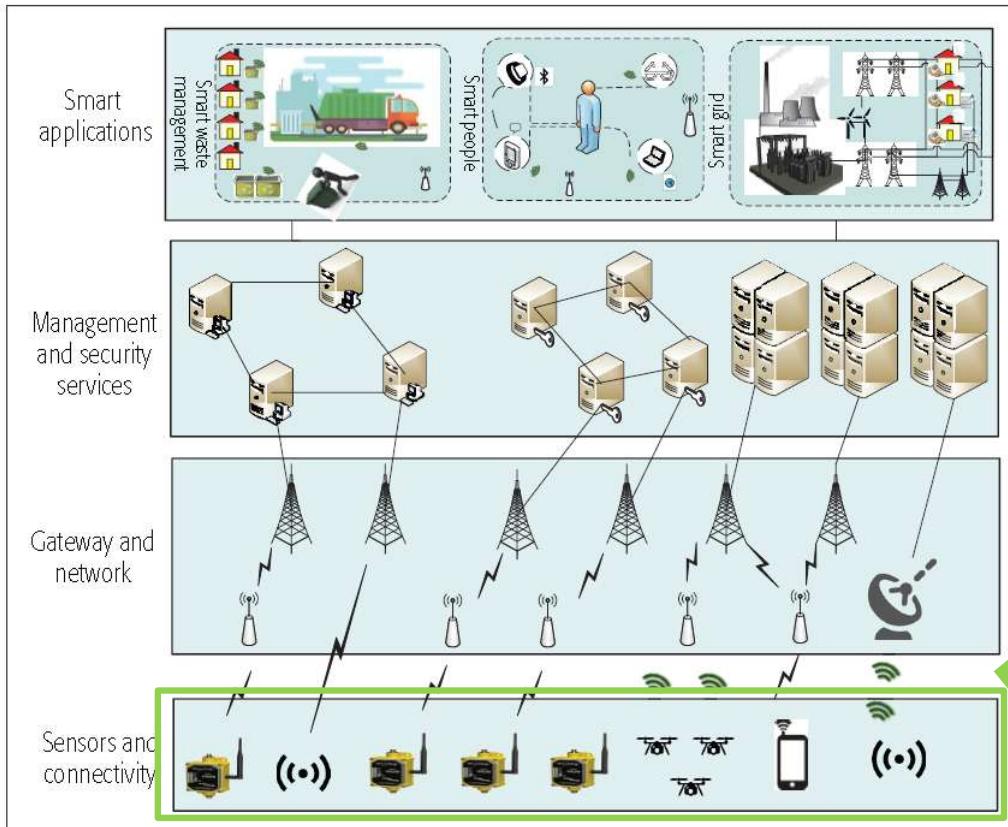


Need for high-performance, efficient and robust ICs



# IC Design meets Power Electronics

## IoT needs for analog design



Example: KickSat project, NASA

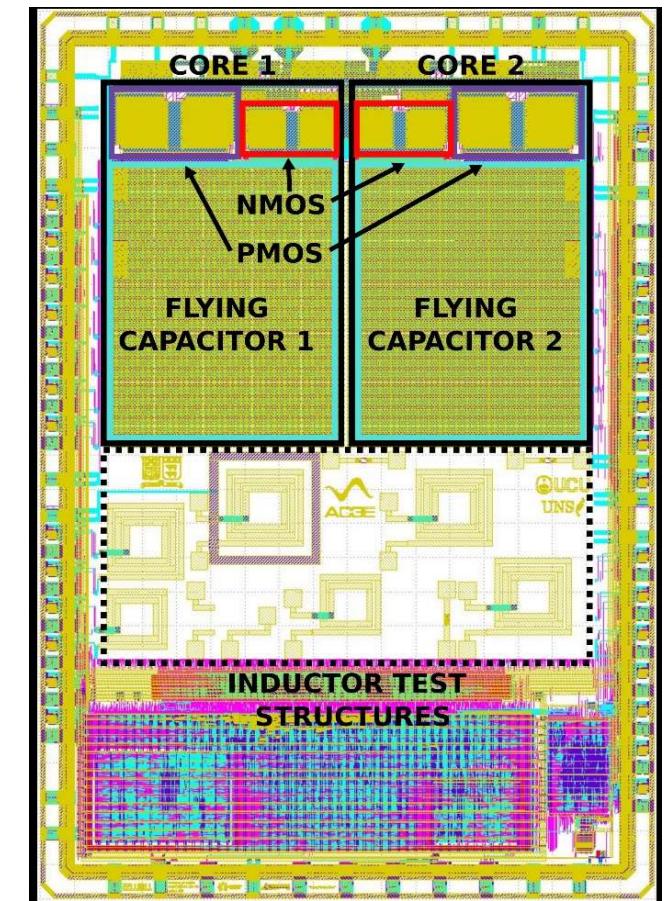
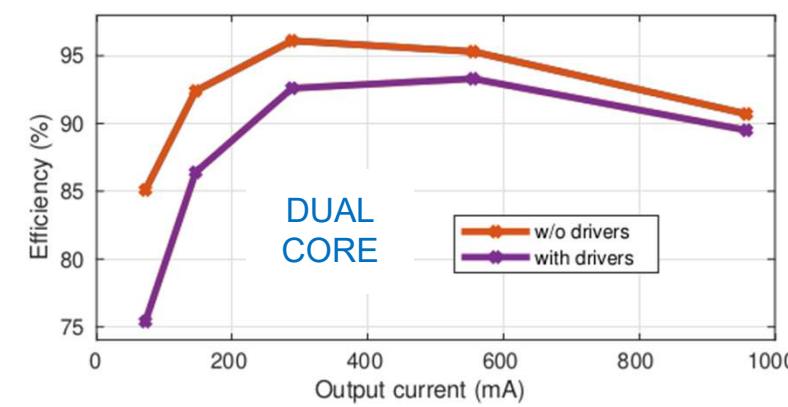
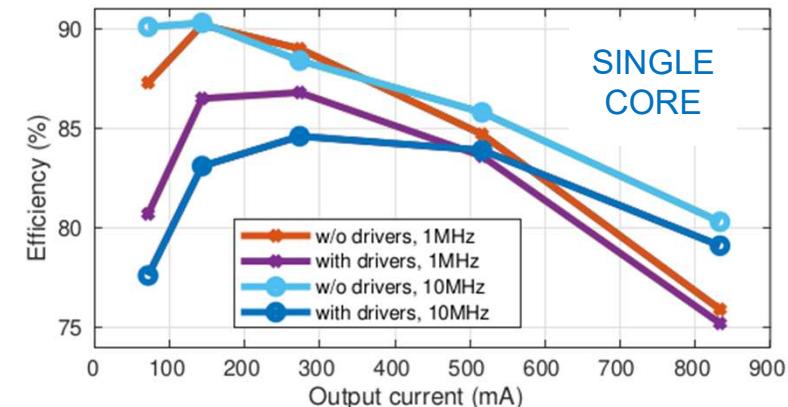
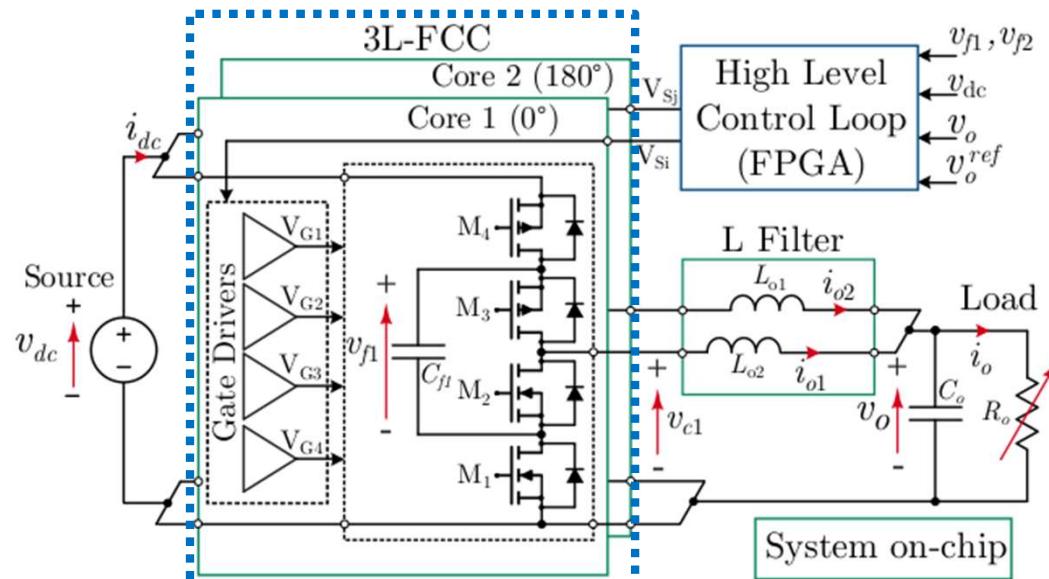


Edge devices performance strongly depends on energy management

# Current research at AC3E-USM: OSIC design and testing

## 3-level flying capacitor DC-DC converter

- Simulations: Efficiency analysis under different conditions
- Implementation: Modular approach → testable subcircuits
- Tapeout: December 2022 → chip delivery: November 2023

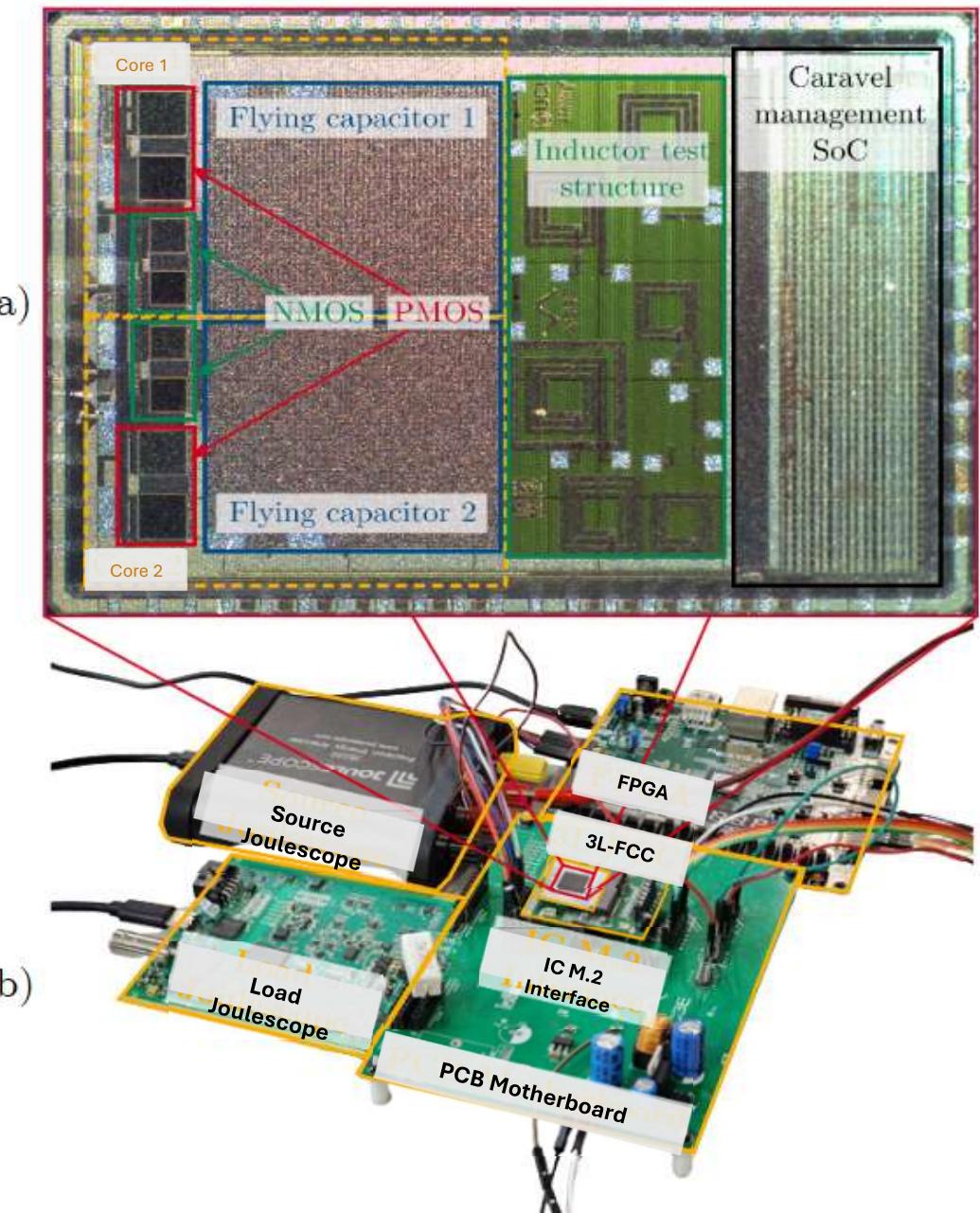


[MARIN, CAE2023]

# Current research at AC3E-USM: OSIC design and testing

## Test setup

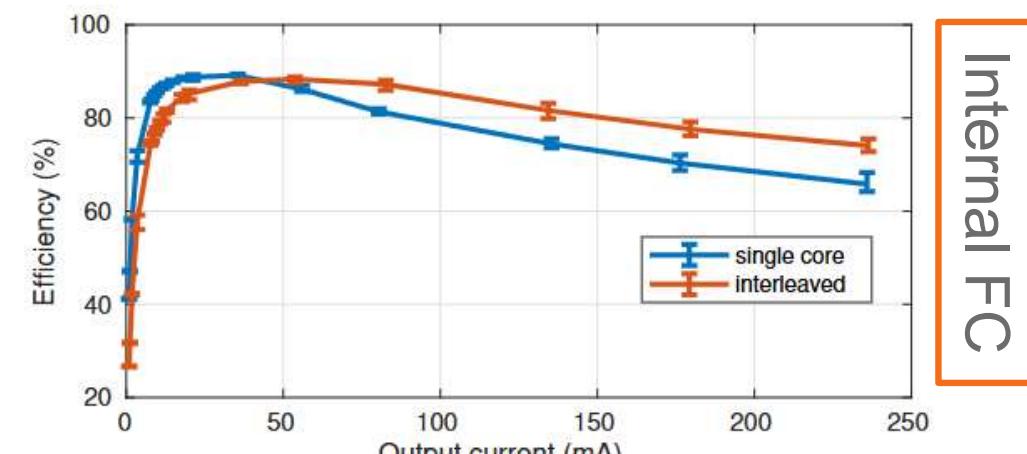
- QFN packages soldered to M2 boards
- Adaptation board for the M2 boards
- Open loop control
  - DC-DC modulator was implemented using a Nexys A7 FPGA
  - 16ns minimum dead time
- Efficiency as main figure of merit for now
  - Internal vs external flying caps
  - Joulescopes
- Other generic equipment: oscilloscope, active probes, power supplies



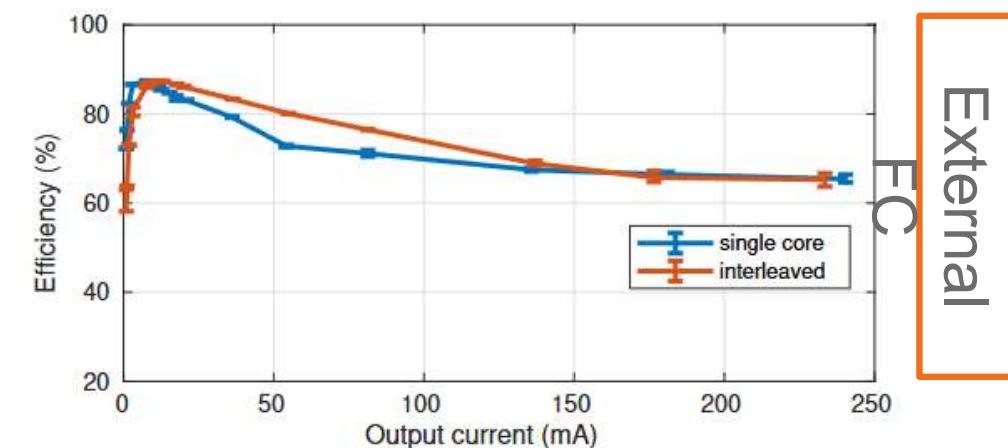
# Current research at AC3E-USM: OSIC design and testing

## Preliminary efficiency measurement results of 3 samples

- 3 samples were fully characterized
  - moderate measurement error
- Internal FC:
  - 89,3% for 21 mA, 1 core
  - 88,9% for 37 mA, 2 cores
- External FC:
  - 87.5% for 8 mA , 1 core
  - 87.4% for 12 mA , 2 cores



(a)



(b)

Internal FC

External FC

# Current research at AC3E-USM: OSIC design and testing

## Code-a-chip automated power IC specs-to-GDS flow

[Rutenbar, 2010]

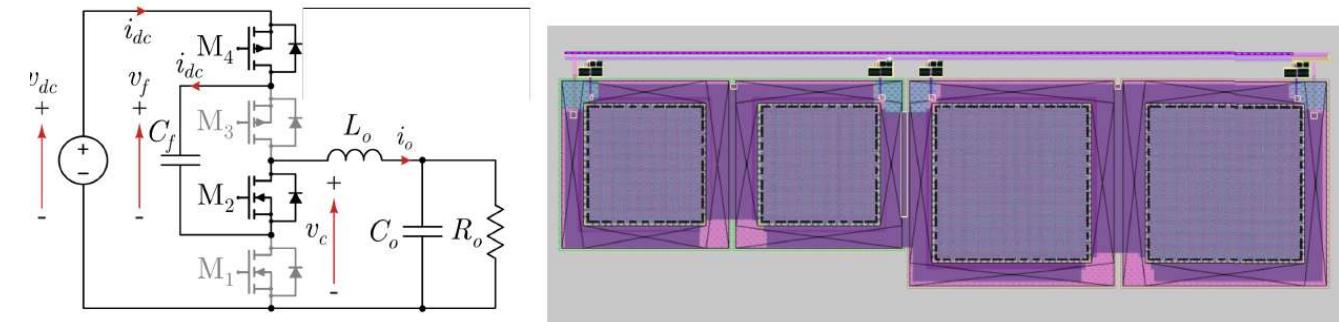
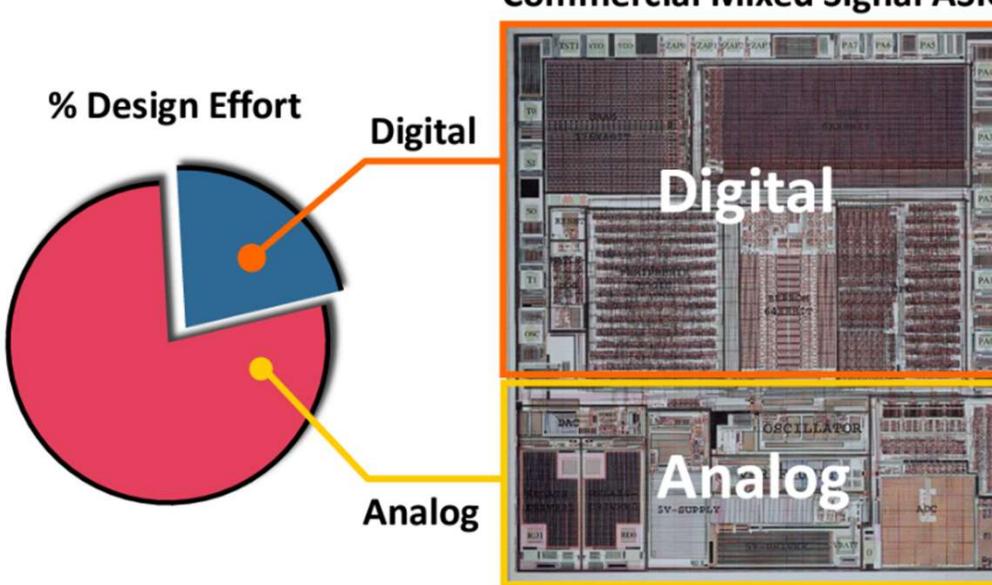
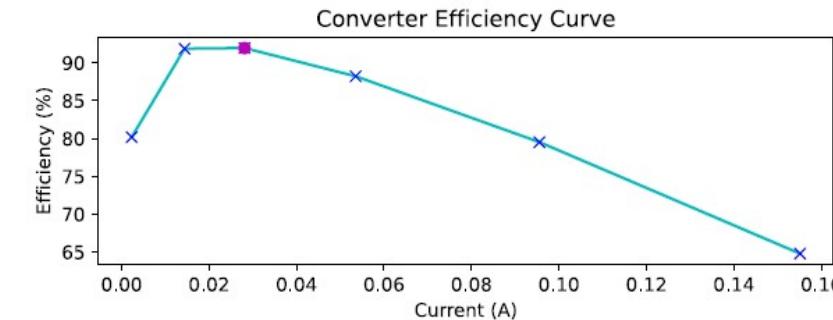


Figure 3: 3LFC Converter schematic (left) and layout (right)



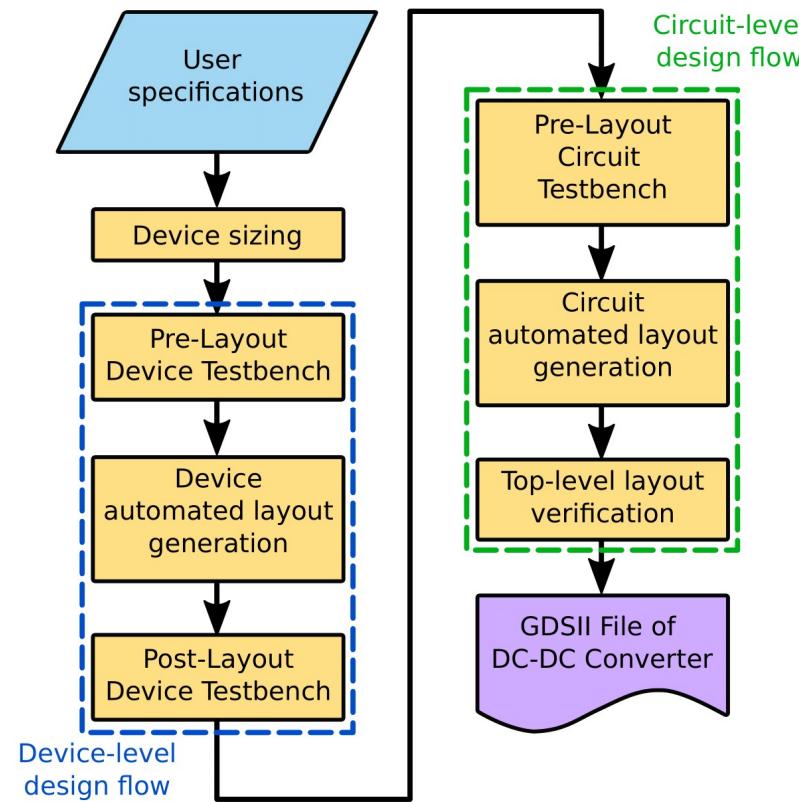
Automated design  
and evaluation?

# Current research at AC3E-USM: OSIC design and testing

## Code-a-chip automated power IC specs-to-GDS flow

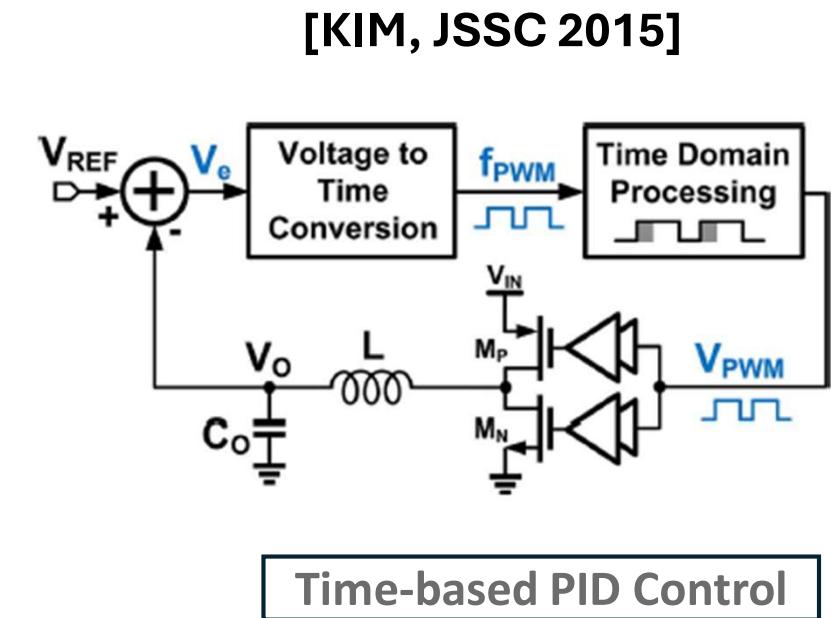
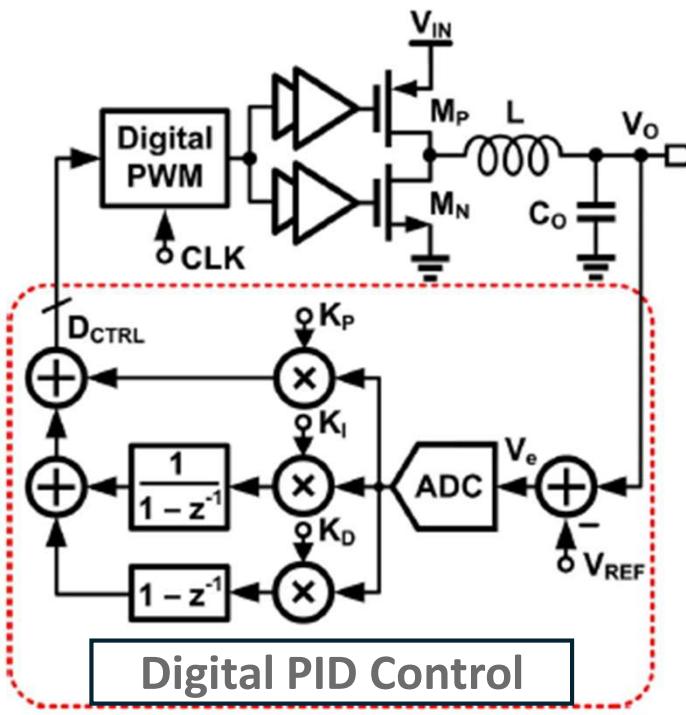
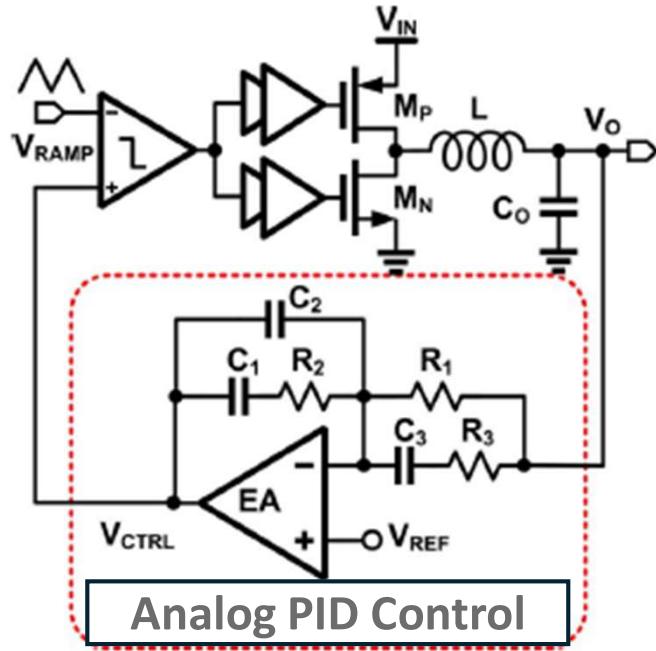
- Full Python-based automated flow using opensource toolkit
- From current, voltage, area and frequency specs to manufacturable layout (GDS file)
- Presented at VLSI Symp. Kyoto 2023

[OSORIO, CAE 2025]



# Current research at AC3E-USM: OSIC design and testing

## Closing the loop: control strategies using the time domain



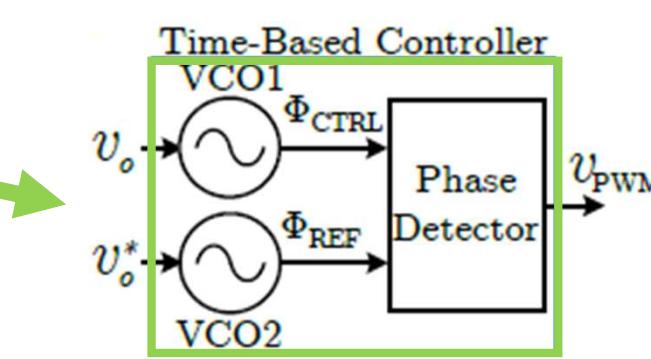
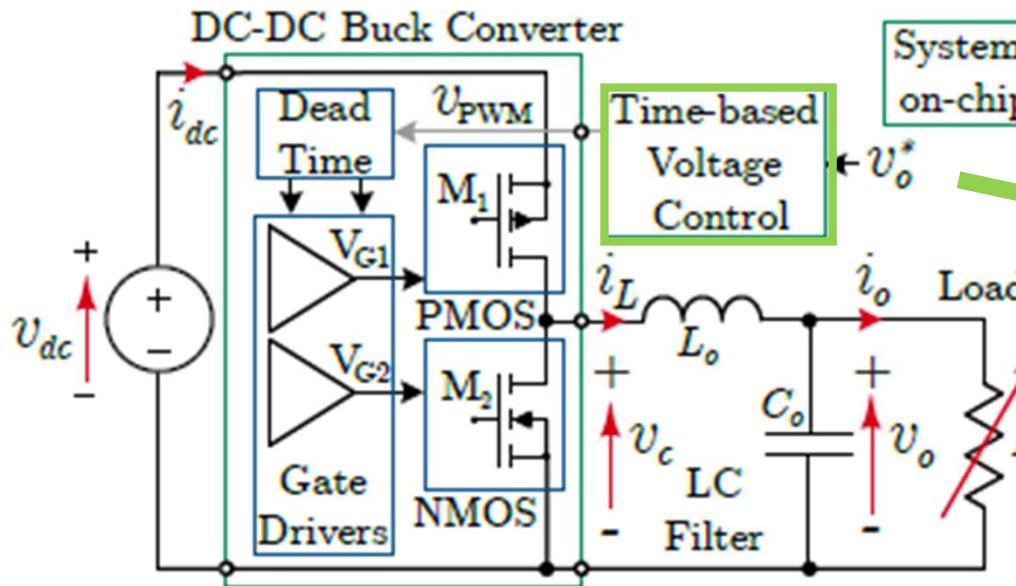
- Well-known implementation
- Not compatible with tech. and voltage scaling
- High power consumption at high frequencies (EA)

- Compatible with advanced nodes
- Requires ADC conversion
- Frequency-limited

- High speed
- Highly digital, so compatible with advanced nodes, low power and area
- New architecture and building blocks

# Current research at AC3E-USM: OSIC design and testing

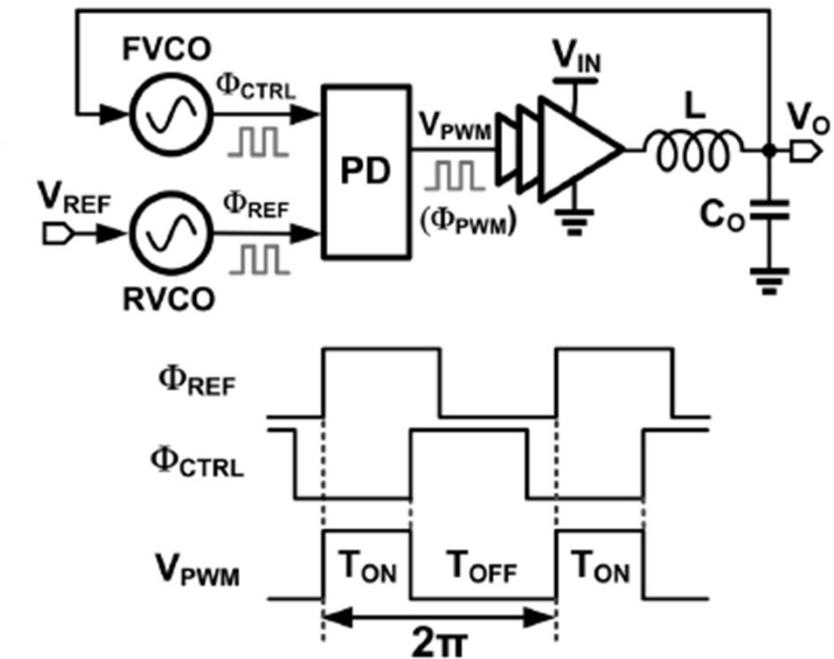
## DC-DC buck converter emerging requirements



[MARIN, LASCAS 2025]

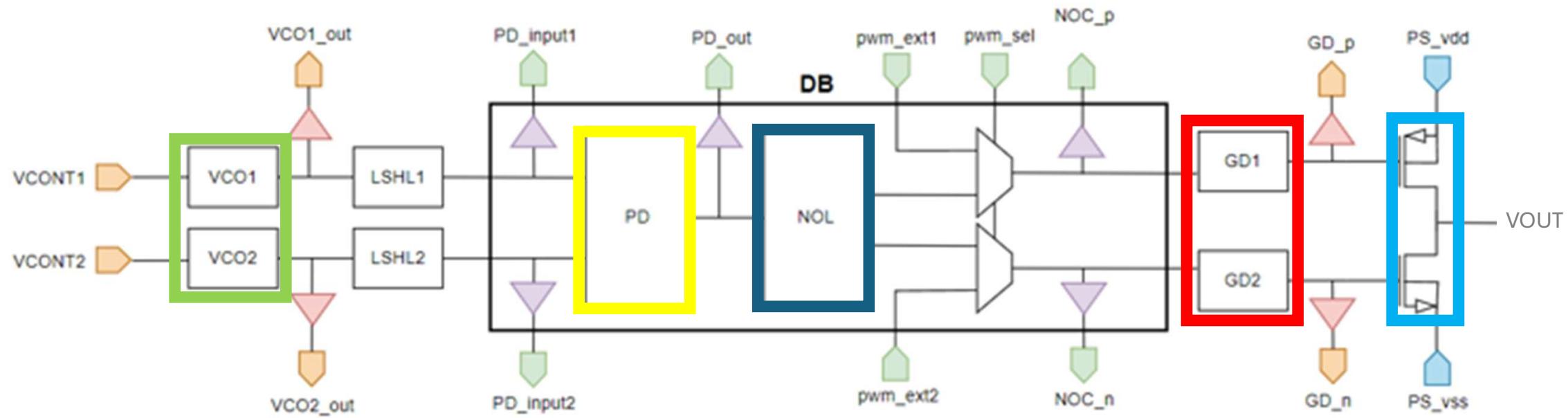
- High-freq. switching
  - Fast transient response and less control loop latency
  - Smaller passive components
- Compatibility with advanced nodes (monolithic integration of PMU) and low power
  - Reduced control circuit area and power consumption
- Robustness
  - Differential cancelling of common mode effects

[KIM, JSSC 2015]



# Current research at AC3E-USM: OSIC design and testing

## Time-based-controlled DC-DC buck converter block diagram



Voltage-controlled oscillators

Phase detector

Non-overlap circuit

PMOS and NMOS power devices

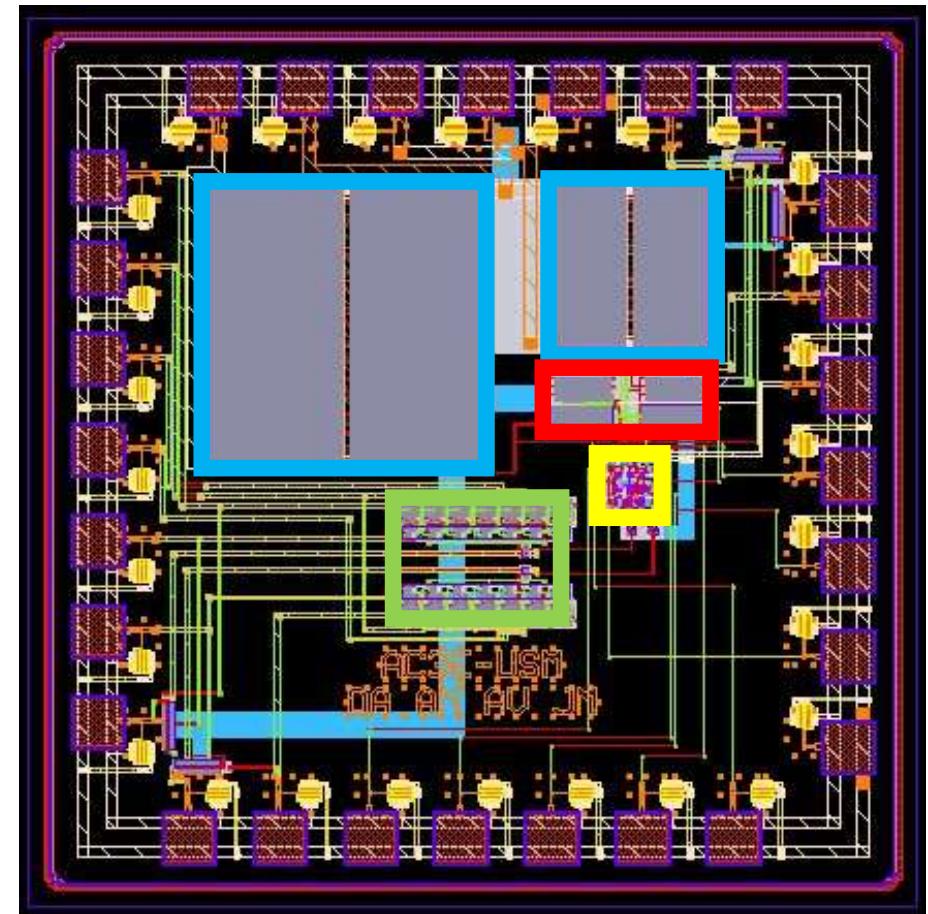
Gate drivers

[MARIN, LASCAS 2025]

# Current research at AC3E-USM: OSIC design and testing

## Time-based-controlled DC-DC buck converter in IHP 130nm CMOS

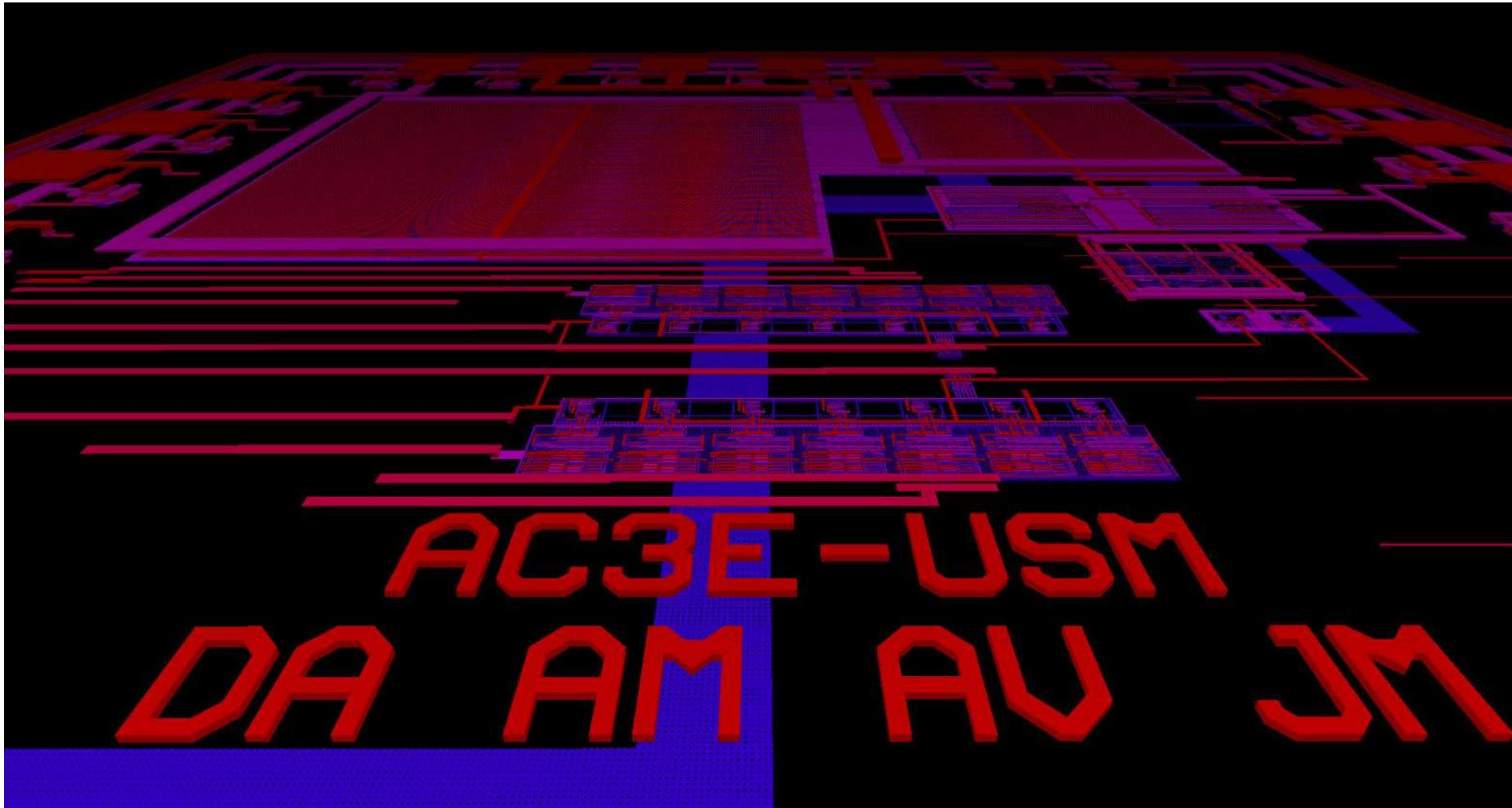
- Chip area: 2mm<sup>2</sup>
- Building blocks
  - PMOS and NMOS power devices
  - Gate drivers
  - Digital block (pase detector + non-overlap)
  - VCOs
- Layout methodologies
  - Analog blocks: exploration of Glayout + manual design
  - Digital block: using digital flow



[MARIN, LASCAS 2025]

# Current research at AC3E-USM: OSIC design and testing

Time-based-controlled DC-DC buck converter in IHP 130nm CMOS



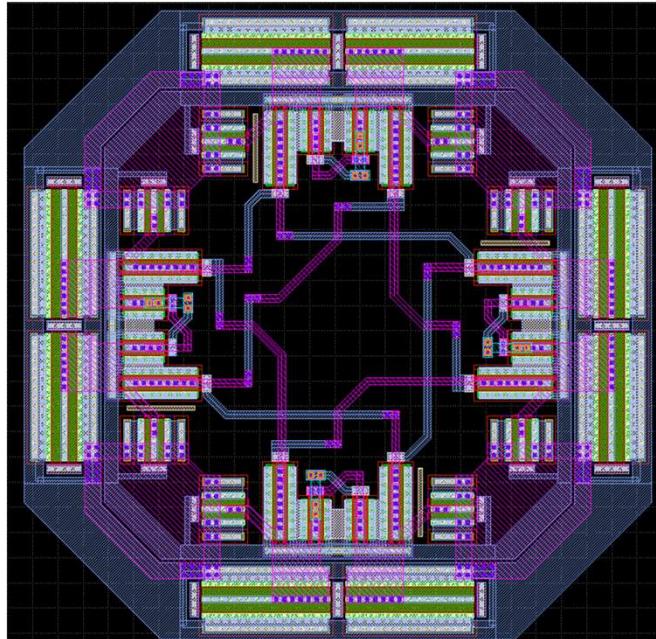
# Other team's R&D in OSIC design

## OPENSOURCE DESIGNS/IP

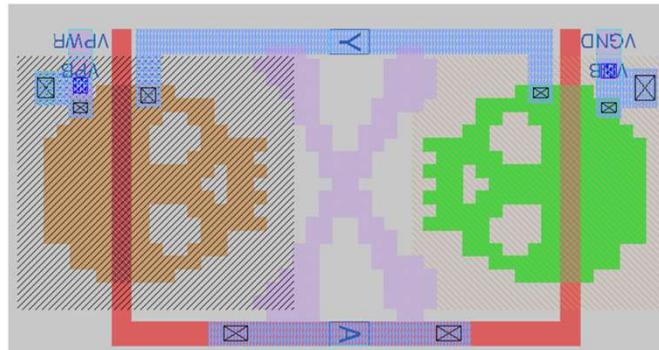
SAR ADC



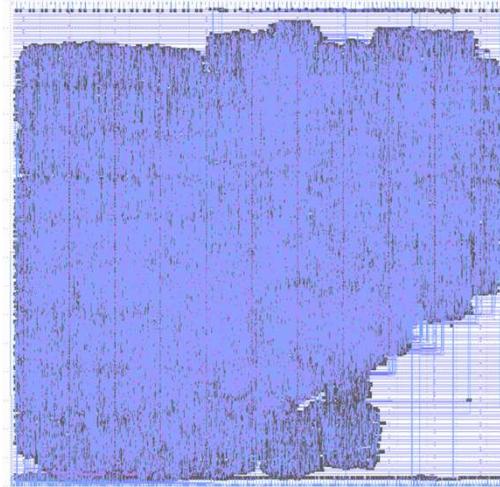
Satellite transceiver



Logic inverter



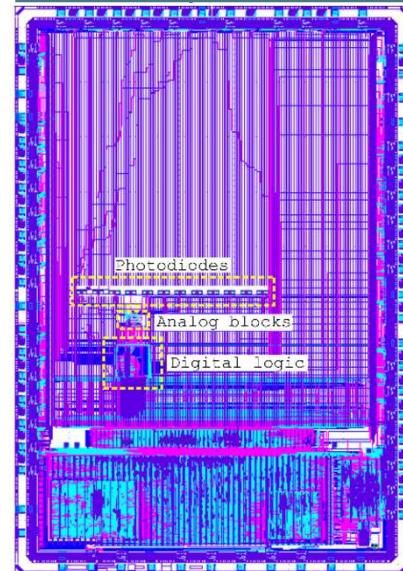
Sudoku Accelerator



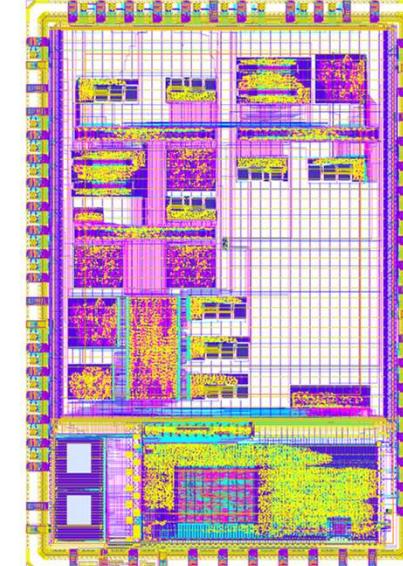
OpenFPGA



MixPix (U. Biobio)



Time to Data Converter



# Opensource designs → re-use and get inspired

- Analog IP components and specifications in Sky130A for Efabless next-generation Caravel (Chipalooza):

<https://docs.google.com/spreadsheets/d/132YkMiYaM0iHML5feT1yWLQIvP-pCM0lCArM9f1LxhM/edit?gid=0#gid=0>

The screenshot shows a Google Sheets spreadsheet with the following data:

Analog IP components and specifications in Sky130A for Efabless next-generation Caravel			
Analog components specified for Chipalooza challenge (see additional sheets)			
IP block	Rank Criticality	Required for ML SoC	URL of Chipalooza challenge submission(s)
Ultra low-power comparator	2	✓	<a href="https://github.com/JYSquare2/sky130_icrg_ip_uipcomp">https://github.com/JYSquare2/sky130_icrg_ip_uipcomp</a> <a href="https://github.com/3x10e8/sky130_rhythmic_ip_dynamic_comparator">https://github.com/3x10e8/sky130_rhythmic_ip_dynamic_comparator</a>
Comparator	2	✓	<a href="https://github.com/Create5517/sky130_pmc_ip_cmp.git">https://github.com/Create5517/sky130_pmc_ip_cmp.git</a>
1.8V Precision bandgap	3	✓	<a href="https://github.com/adankvitschal/sky130_at_ip_cmos_vref">https://github.com/adankvitschal/sky130_at_ip_cmos_vref</a> <a href="https://github.com/dcde10893/sky130_deser_ip_lowpowerLDO">https://github.com/dcde10893/sky130_deser_ip_lowpowerLDO</a>
Low-power 1.8V LDO	3	✓	<a href="https://github.com/AlexMenu/sky130_am_ip_ldo_01v8">https://github.com/AlexMenu/sky130_am_ip_ldo_01v8</a>
Current reference bias generator	2	✓	<a href="https://github.com/tatzelbrumm/sky130_cm_ip_biasgen">https://github.com/tatzelbrumm/sky130_cm_ip_biasgen</a>
16-bit capacitive DAC	1	✓	
12-bit resistive DAC	2	✓	

- IHP opensource designs (per tapeout), e.g.:  
[https://github.com/IHP-GmbH/TO\\_Nov2024](https://github.com/IHP-GmbH/TO_Nov2024)

**Thank you!  
Questions?**