

Open-Source IC Design Workshop

1.3 Open-source analog design tools

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UNIVERSIDAD TECNICA
FEDERICO SANTA MARIA



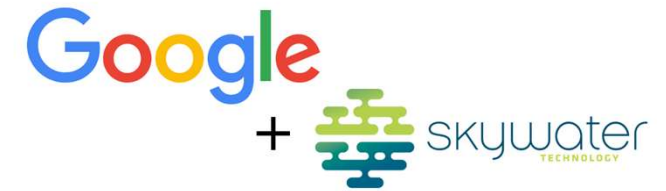
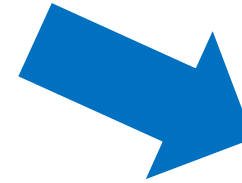
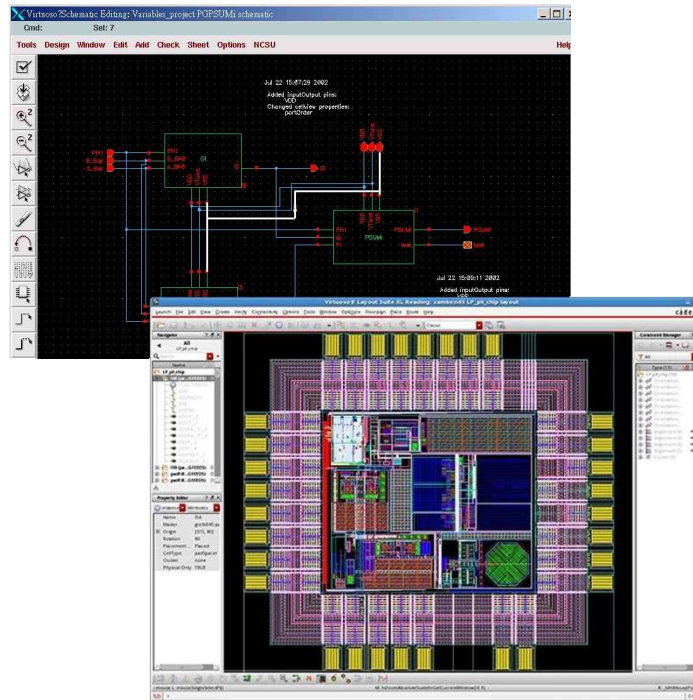
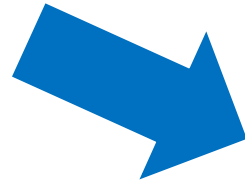
Agenda

- Introduction
- Open-source analog design tools
- Simulation examples

Introduction

Introduction

IC design: from manual to automated



FOSS 130nm Production PDK
github.com/google/skywater-pdk

IHP-GmbH/IHP-Open-PDK-docs

Documentation for IHP 130nm BiCMOS Open Source PDK



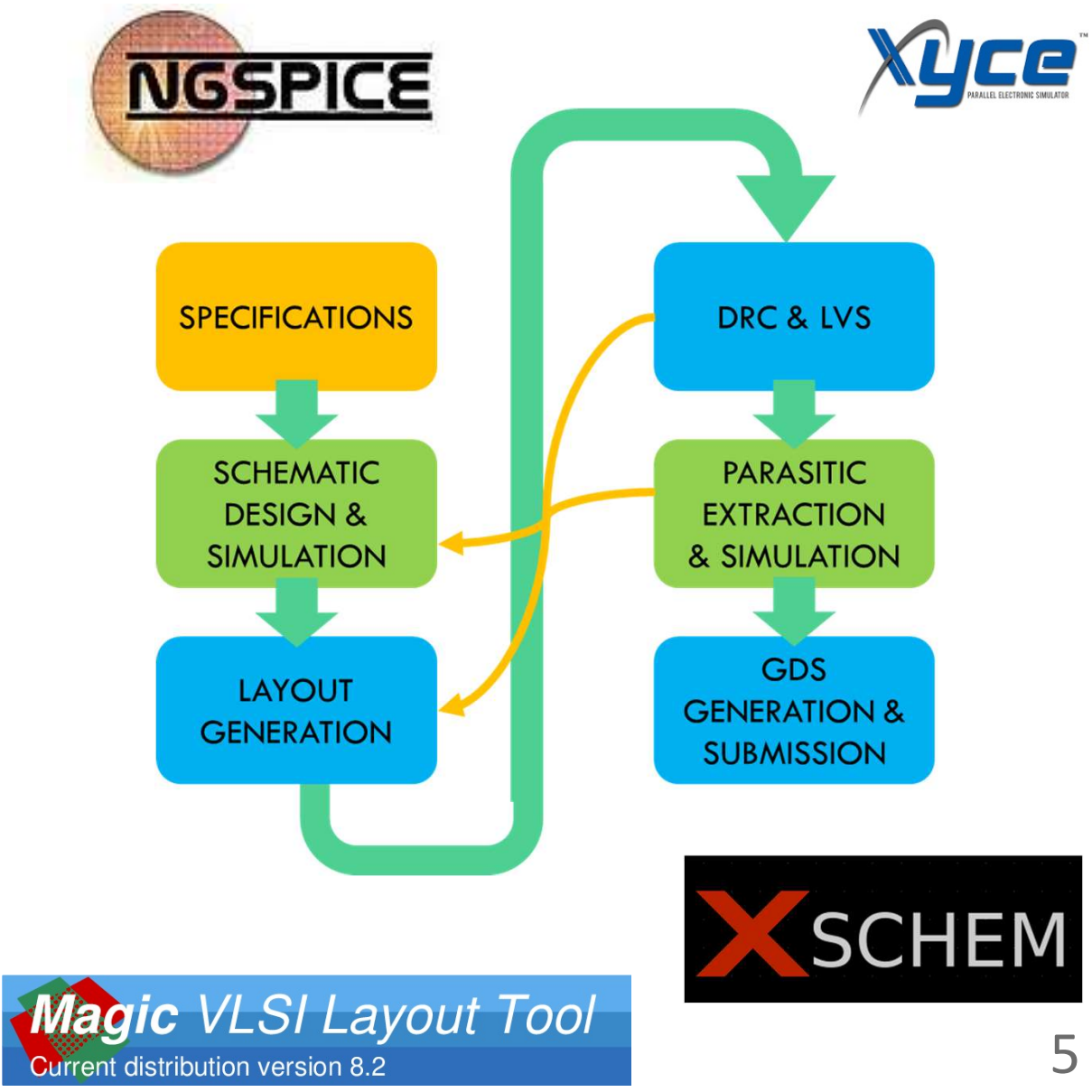
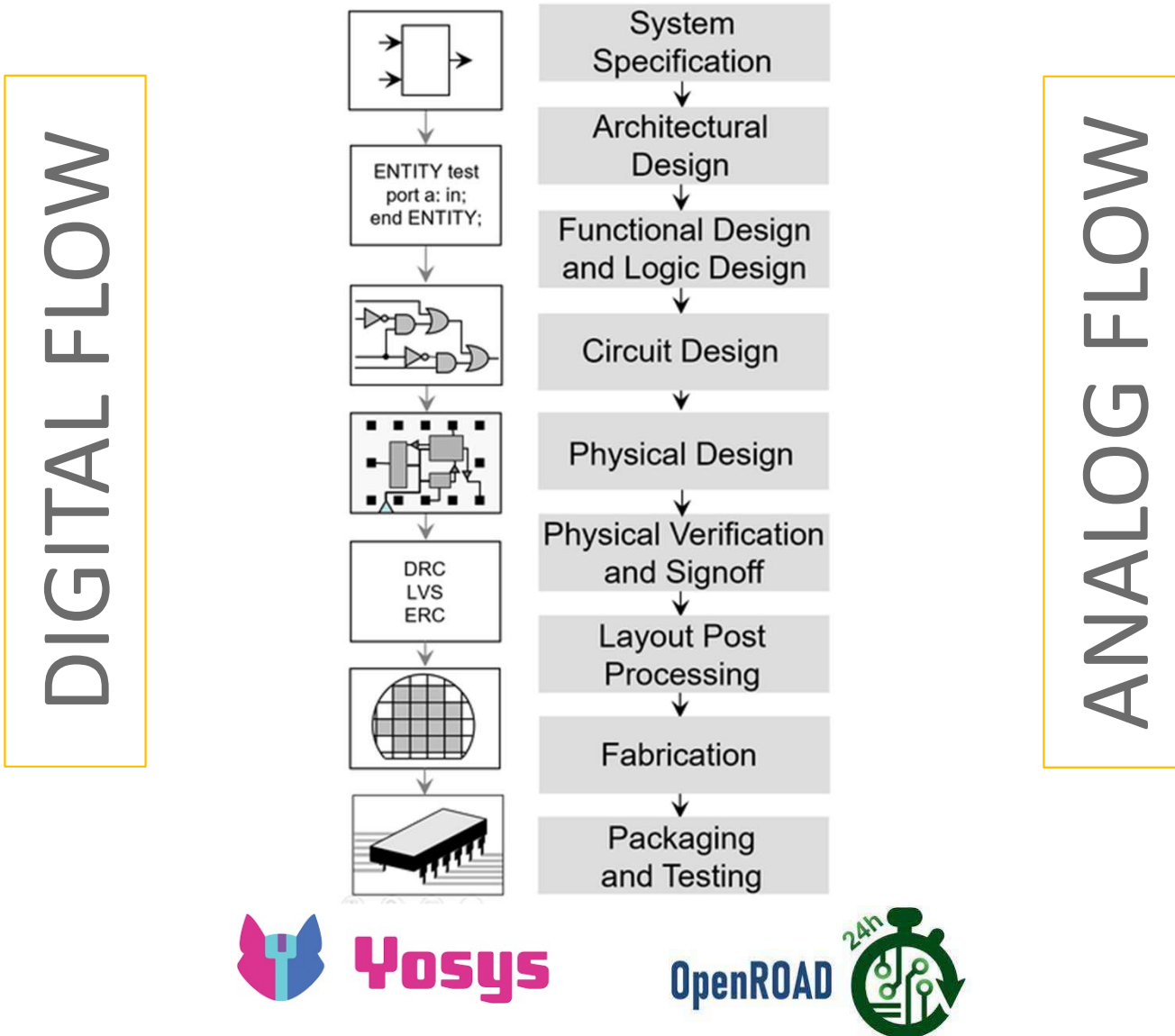
> 2020 → Opensource EDA tools and PDKs

< 1990s → fully manual chip design!

> 1990s → EDA tools

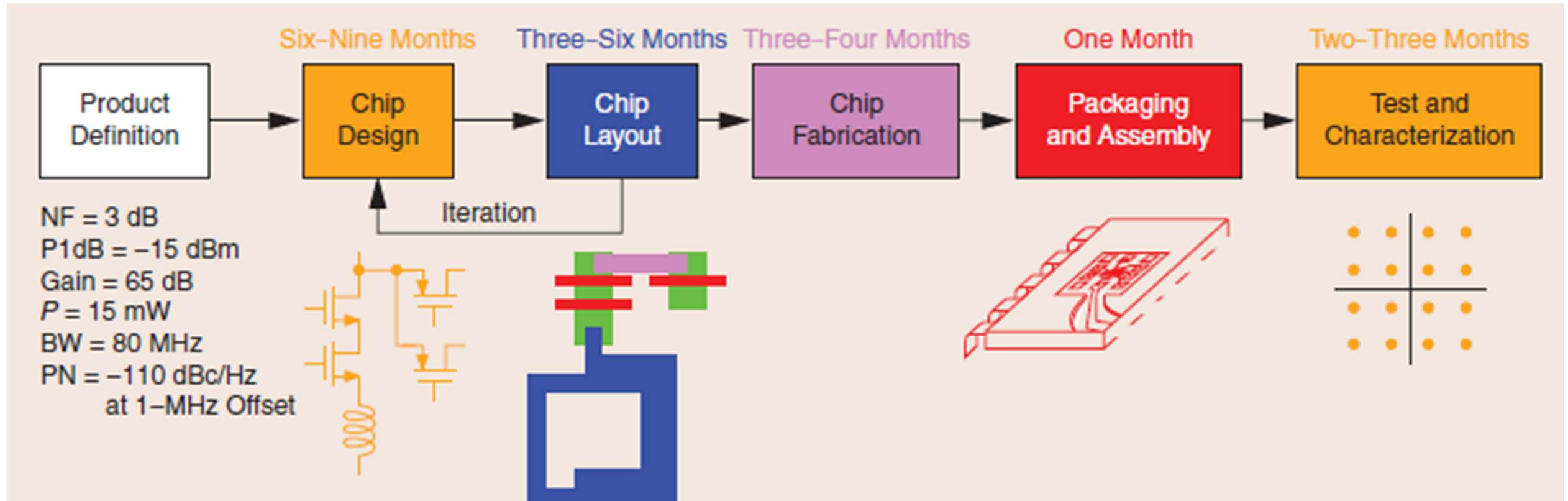
Analog vs digital design flows

IC design flow: digital versus analog



Introduction

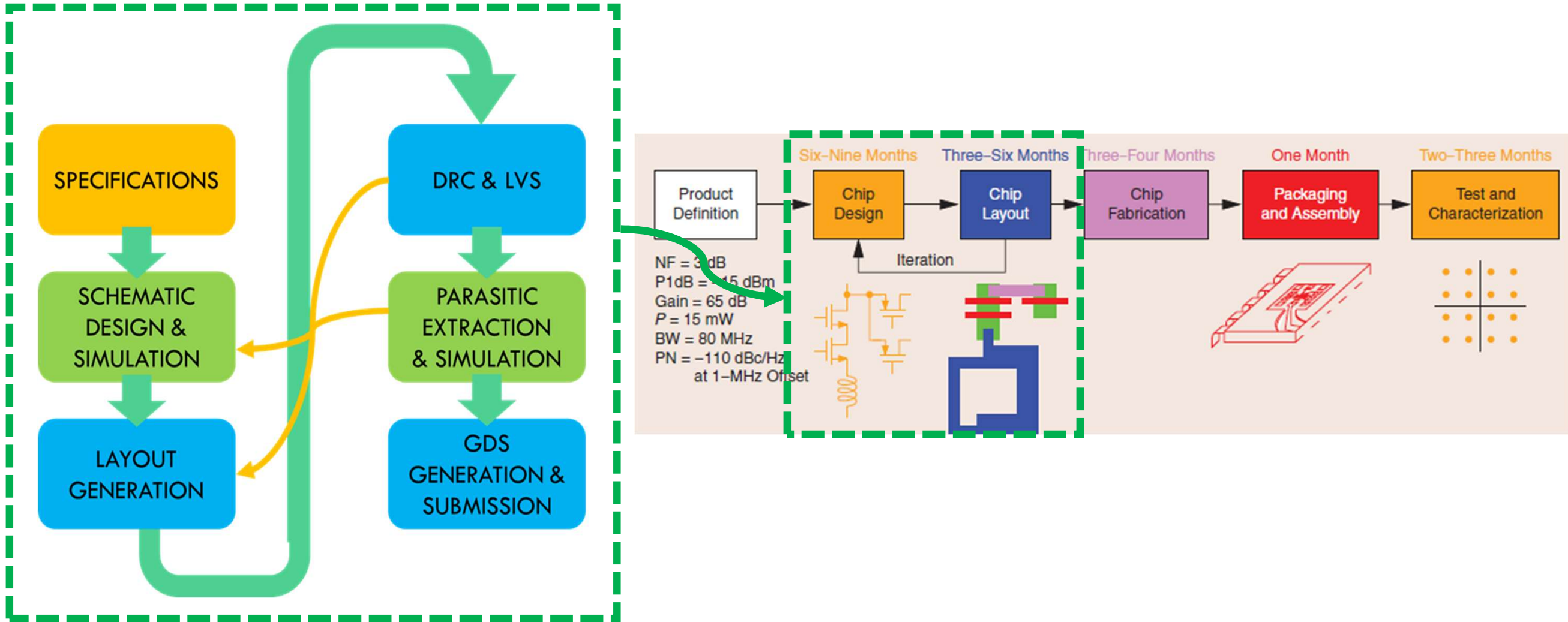
Silicon-proven analog IC design



**[RAZAVI, IEEE SSCMAG
2024]**

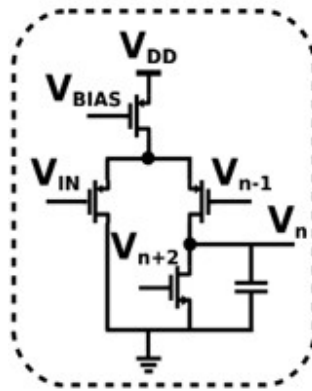
Introduction

Silicon-proven analog IC design

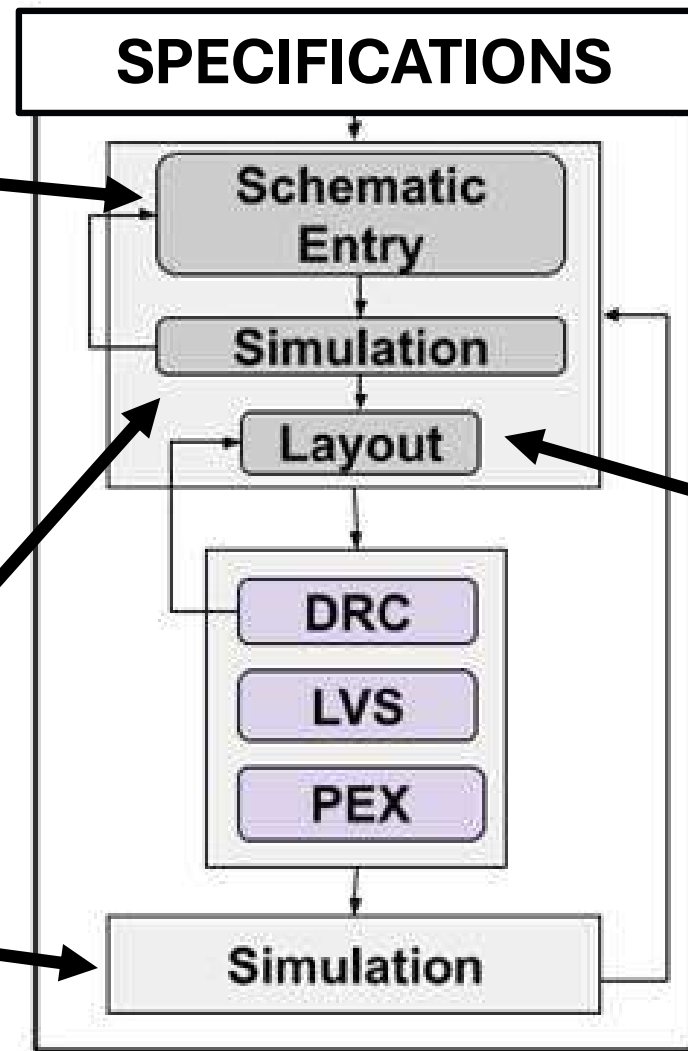
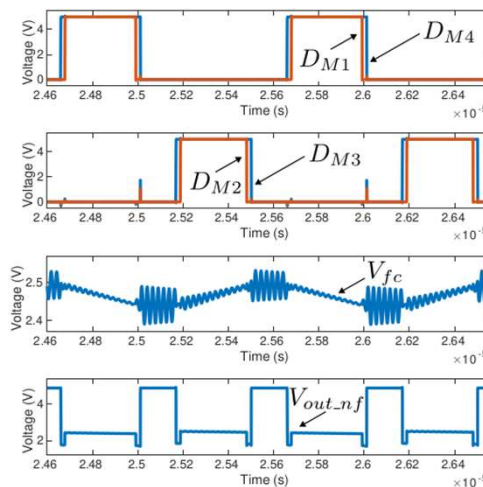


Introduction

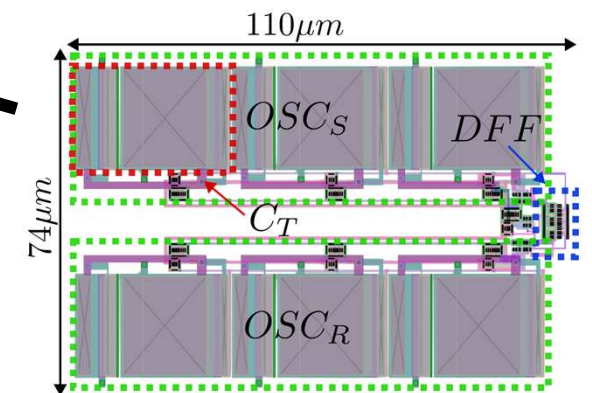
This workshop's plan



**PROJECT (DAYS
4 AND 5)**

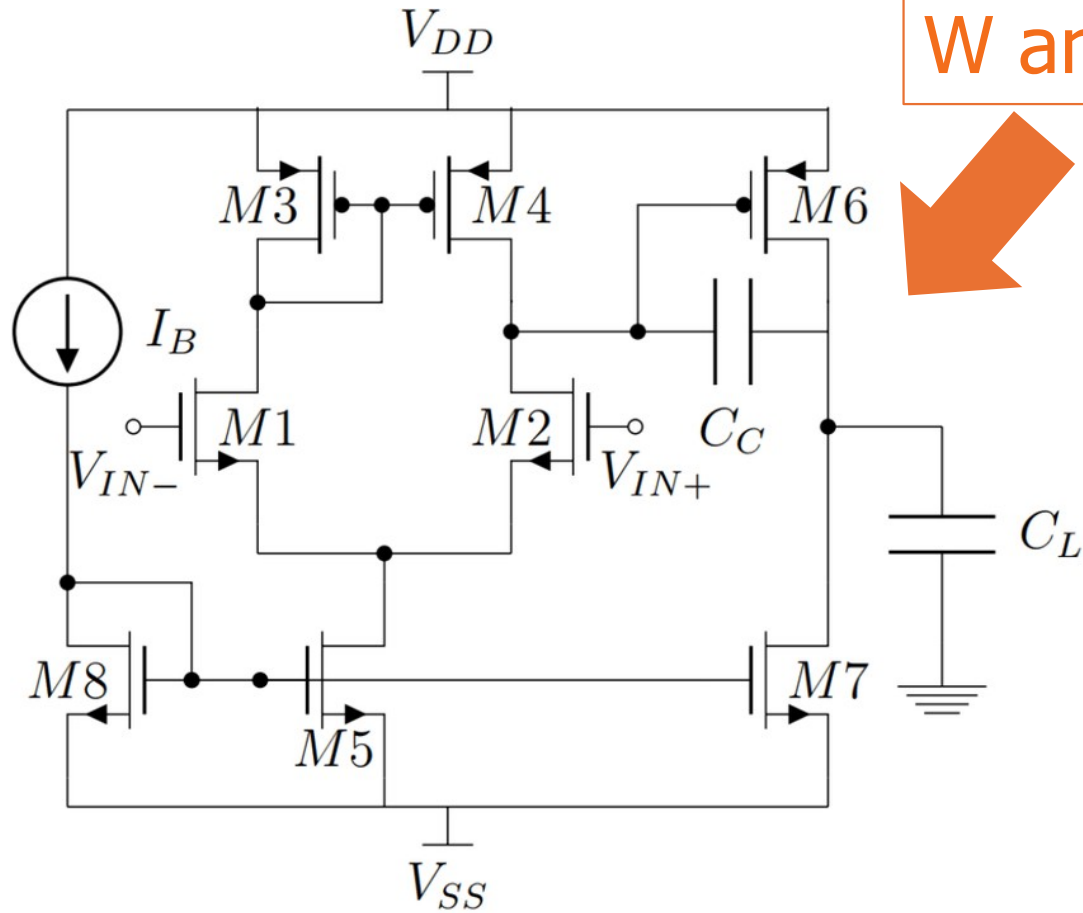


DAYS 2 AND 3

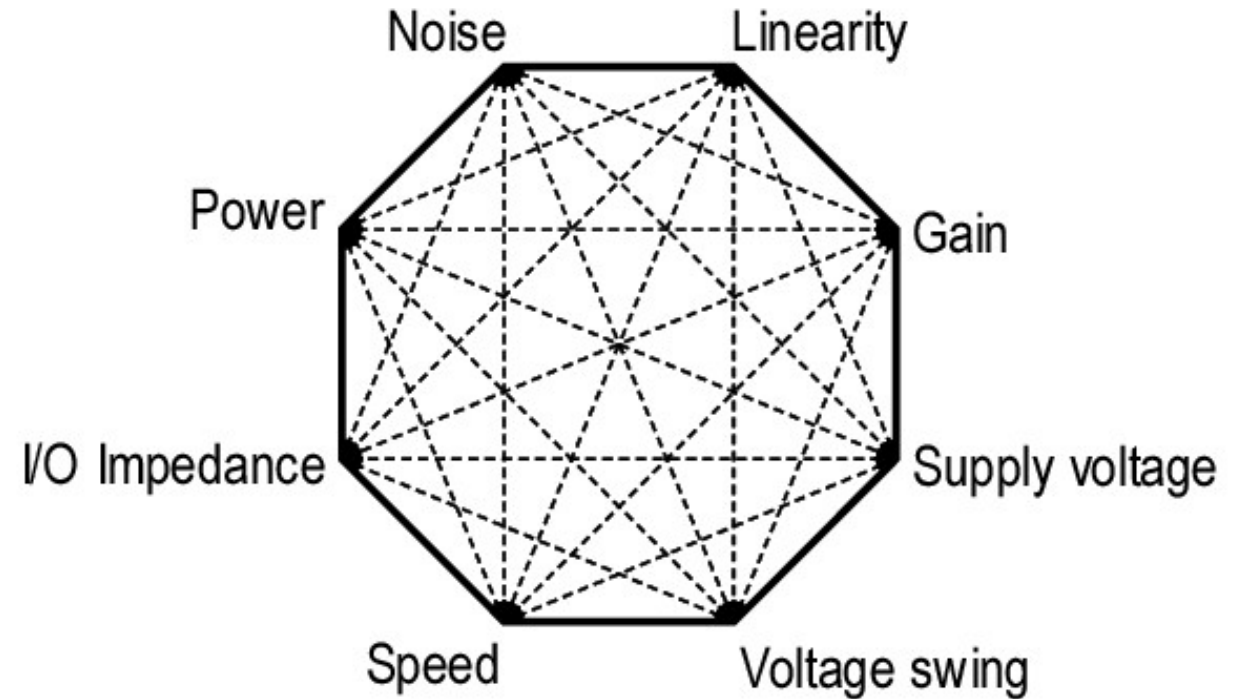


Open-Source Analog Design

Tradeoffs in analog design



W and L for each transistor M1 to M8?



[B. Razavi]

Analog block example: Miller OTA

Performance is limited by the tradeoff in target specifications

Schematic design and simulation

- Relevant tools
 - Xschem → schematic entry and netlist generation
 - Ngspice → simulation based on netlist generated by Xschem
- Visualization
 - Ngspice window → quick checks
 - GAW → integrated in Xschem
 - External viewer through raw data (e.g. Python script)

Simulation types

- DC → analysis of the circuit operating point
- Transient → time-domain behaviour
- AC → frequency sweep
- Noise → simulation of device intrinsic noise
- And others...

Ngspice manual will become your best friend!
<https://ngspice.sourceforge.io/docs/ngspice-manual.pdf>

Xschem GUI basics part 1

www.xschem.sourceforge.io

File Edit Options View Properties Layers Tools Symbol Highlight Simulation

Netlist Simulate Waves Help

not.sch +

'w'

draw wire

'm'

move element

'ALT + f'

flip

'SHIFT + r'

rotate

'u'

undo

'c'

copy

'q'

open object query window

'a'

auto symbol creation

'insert'

open insert device window

'e' / 'CTRL + E'

descend/ascend hierarchy

Generate netlist

Execute simulation

Check waveforms (GAW)

SNAP: 10

GRID: 20

NETLIST MODE: spice

mouse = 40 -630 - selected: 0 path: .X1.

Simulation scope

- Nominal

Ideal simulation without considering many fabrication effects

- P(VT) corners

Considers global process variation (P) and environment (Voltage, temperature, T)

```
.lib cornerMOSlv.lib mos_tt  
.lib cornerRES.lib res_typ  
.lib cornerCAP.lib cap_typ
```

- Mismatch

Considers local statistical variation among devices

→ See examples in /opt/pdks/ihp-
sg13g2/libs.tech/xschem/sg13g2_tests/mc_*.sch

- Parasitic extraction/ post layout simulations

Components associated to extrinsic structures (metallization)

Simulation examples

Clone Workshop repo

- Set PDK to IHP 130nm → INSIDE Docker:
 - ls /opt/pdks/ → see installed PDKs
 - set_pdk ihp-sg13g2

```
designer ~  
$ set_pdk ihp-sg13g2  
PDK set to ihp-sg13g2
```

- OUTSIDE Docker:
 - cd [YOUR_INSTALL_FOLDER]\uniccass-icdesign-tools\shared_xserver\
 - git clone https://github.com/JorgeMarinN/OS_AnalogIC_UCU_July2025

Example #1: Basic inverter

- Github link:

→ https://github.com/JorgeMarinN/OS_AnalogIC_UCU_July2025/blob/main/Day1/tb_inv_1_manual.sch

Simulation/measurement
SPICE code

NGSPICE

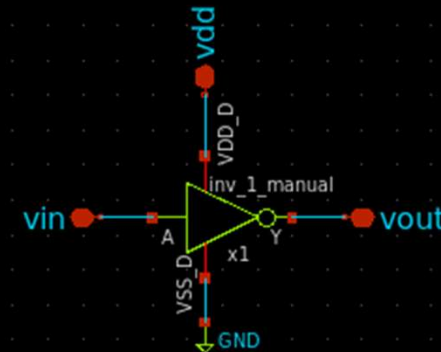
```
vin vin 0 dc=0.6
vdd vdd 0 dc=1.2

.control
save all

dc vin 0 1.2 0.01

plot v(vout)

.endc
```



Schematic

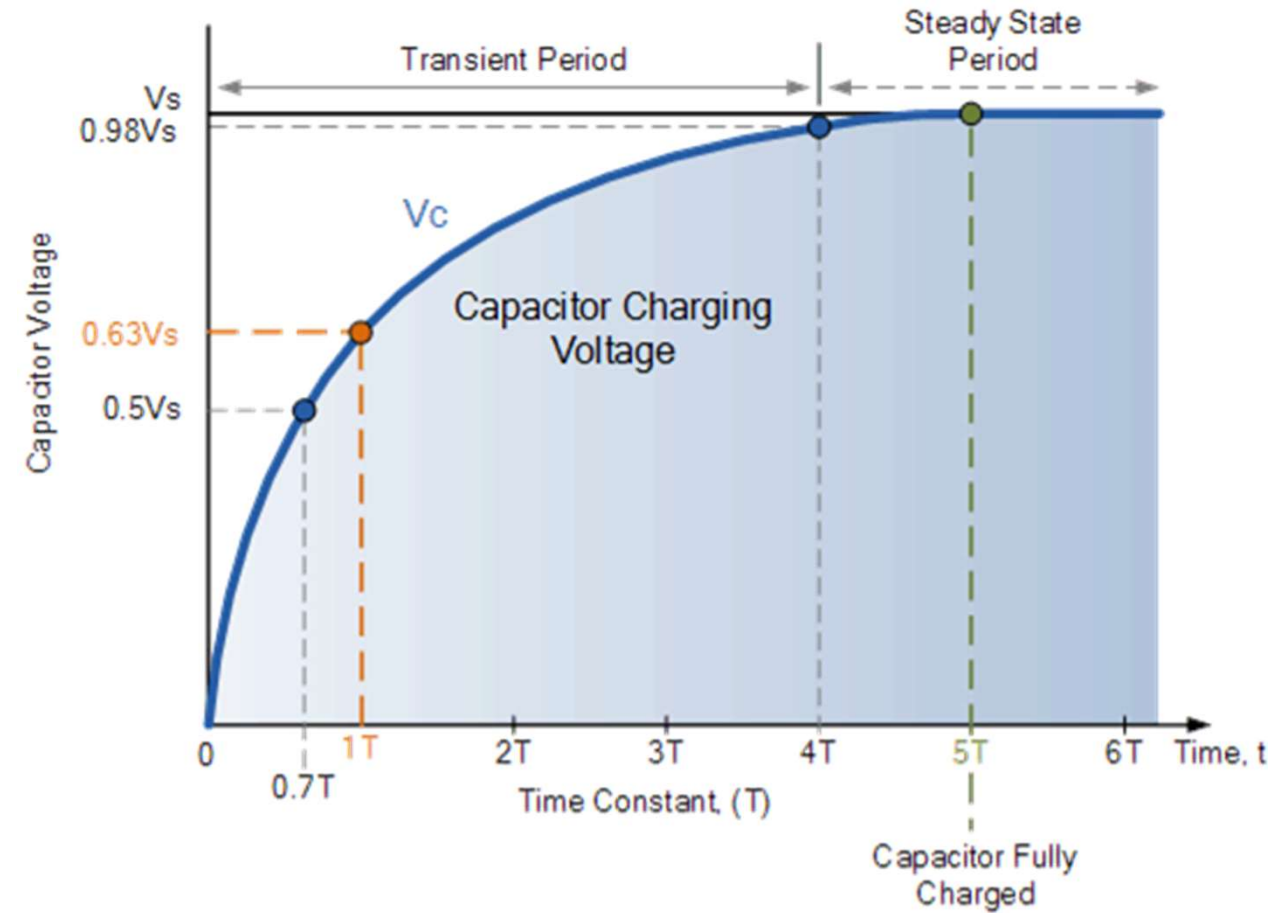
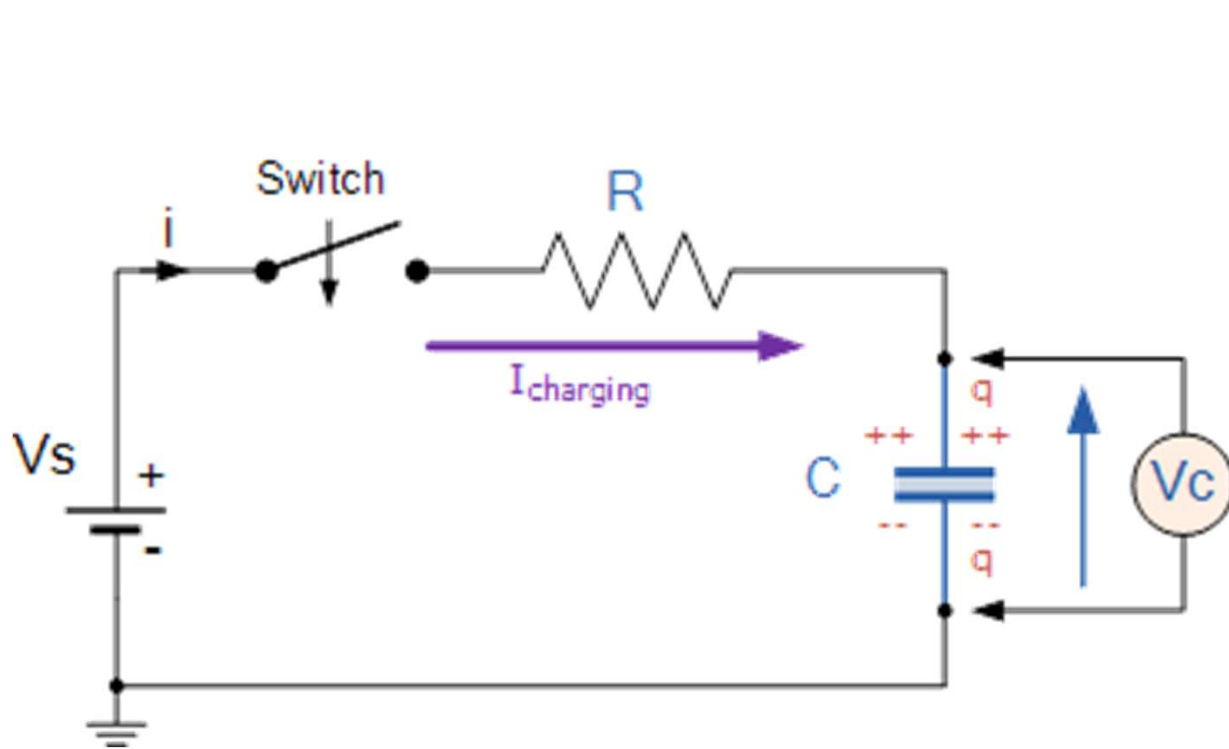
MODEL1

```
.param corner=0

.if (corner==0)
.lib cornerMOSlv.lib mos_tt
.lib cornerRES.lib res_typ
.lib cornerCAP.lib cap_typ
.endif
```

SPICE deck
definition

Example #2: RC constant calculation

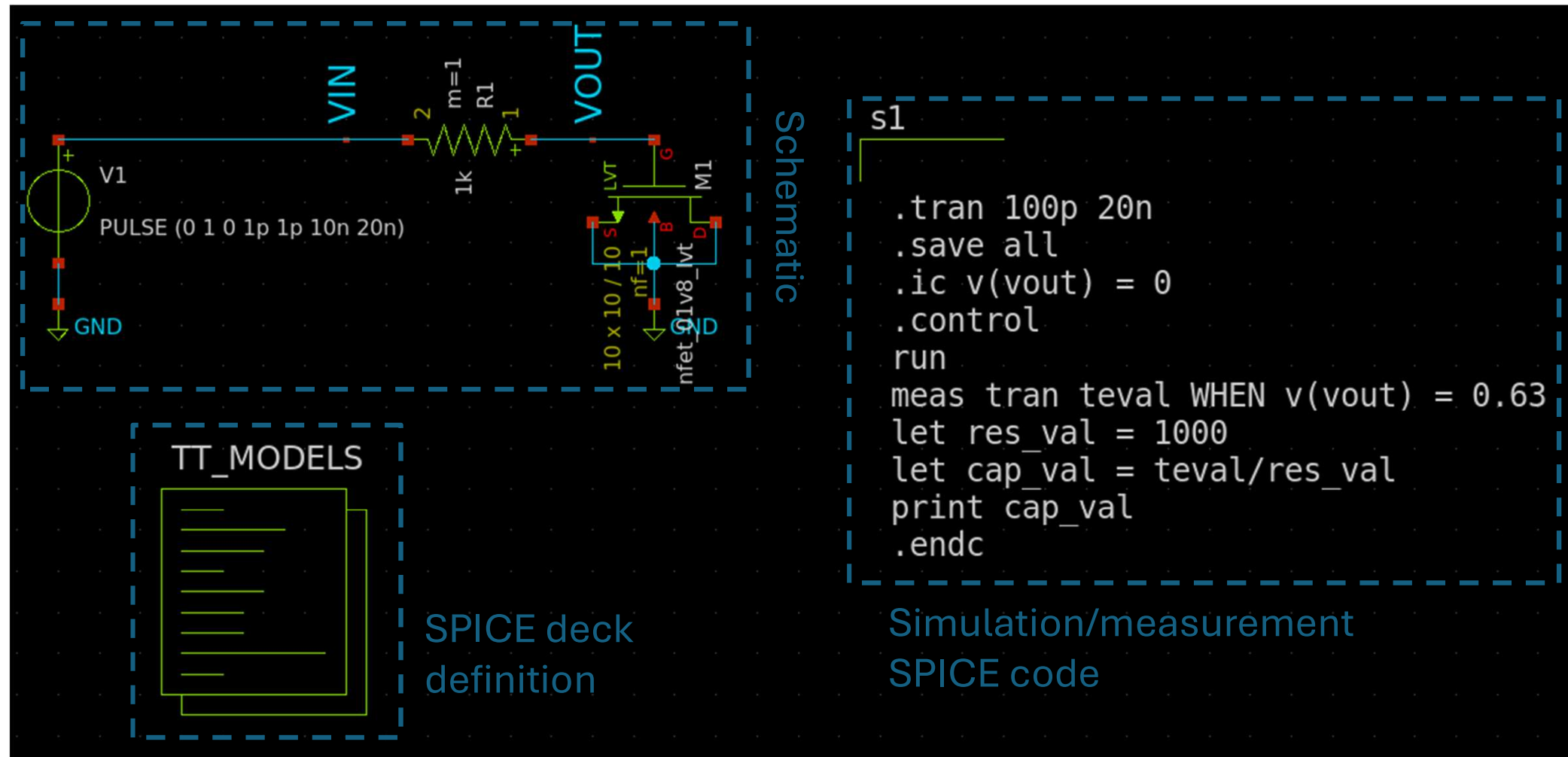


Example #2: RC constant calculation

- Github link:

→ https://github.com/JorgeMarinN/OS_AnalogIC_UCU_July2025/blob/main/Day1/rc-ext_circuit.sch

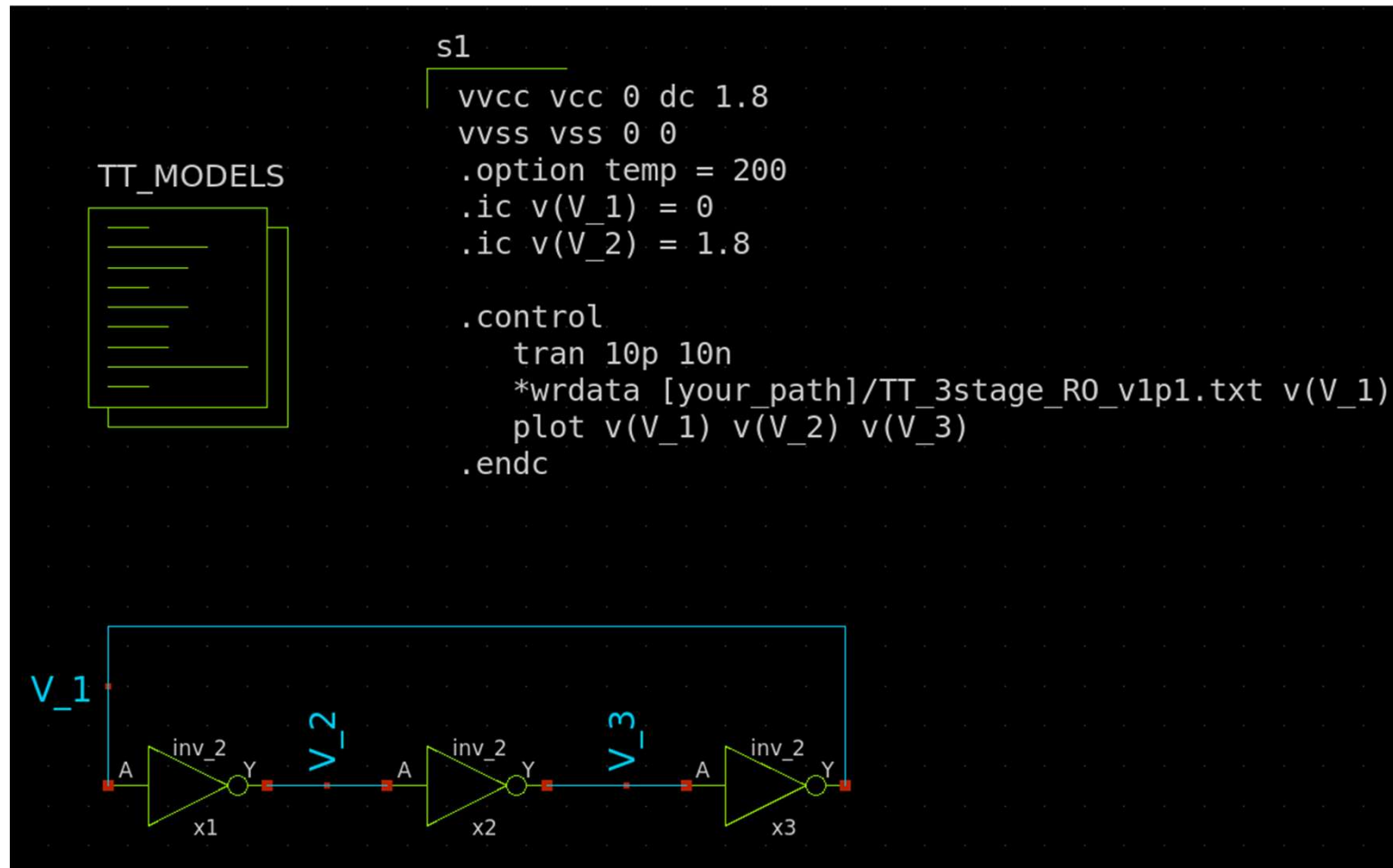
→ https://github.com/JorgeMarinN/OS_AnalogIC_UCU_July2025/blob/main/Day1/cgate-ext_circuit.sch



Example #3: ring oscillator

- Github link:

→ https://github.com/JorgeMarinN/OS_AnalogIC_UCU_July2025/blob/main/Day1/tb_3stage_RO.sch



Education using AMS design OS tools

- Traditional IC design flows are not designed for educational purposes
 - The wide variety of tools and workflows can be overwhelming for beginners
 - High costs and restricted PDK availability limit accessibility
 - Limited documentation and minimal community-driven collaboration hinder learning
- Tapeout courses require significant budgets, making them inaccessible to many universities and regions
- IC design environments have traditionally been restrictive
 - Strict NDAs restrict access to essential resources
 - Information sharing is trust-based and highly limited
 - However, this landscape is rapidly evolving, opening new opportunities for education!

Removing barriers: knowledge base

- JKU's "Analog Circuit Design course" → <https://github.com/iic-jku/analog-circuit-design>
 - Fully-open content for intermediate-level MOSFET circuit design course
 - Based on Xschem and Ngspice examples + IHP technology
 - Uses JKU's IIC-OSIC-TOOLS Docker
- University of Hawai'i's "Analysis and Design of Integrated Circuits" tapeout course → <https://github.com/bmurmannel/EE628>
 - Open content for lectures and assignments
 - Design of a Sigma-delta converter using OS design flow + IHP technology

Removing barriers: knowledge base

- MANY other sources:
 - Carsten Wulff's course: https://youtube.com/playlist?list=PLybHXZ9FyEhbm9-A3QR1NRlt6VxeTXyr5&si=31ccv4rhWpso_Ci
 - Angel Abusleme's course [in Spanish]: <https://youtube.com/playlist?list=PLDYu8HgBbvRFf2PahRmg4ABDxRN60ujKQ&si=jnnEGgbled8ik8av>
 - Tiny tapeout: <https://tinytapeout.com/specs/analog/>
 - [NEW] IHP Analog Academy: <https://github.com/IHP-GmbH/IHP-AnalogAcademy>

Thank you!
Questions?