



Leibniz Institute
for high
performance
microelectronics

IHP-Open-PDK Review: Present Status and Future Directions

Krzysztof Herman



Herramientas Open-Source para
desarrollo de circuitos integrados

Projects: BMFTR -> FMD-QNC (16ME0831)
VDE/VDI -> IHP Open130-G2 (16ME0852)

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Our motivation and goals in the open source silicon domain

Description of the open source solutions developed and supported by IHP

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Planification of Open MPW runs

Lessons learned and future activities

IHP in a nutshell



- 0 IHP is the European research and innovation centre for silicon-based systems, ultrahigh-frequency circuits and technologies,
- 0 Unique selling point of a 200mm pilot line for state-of-the-art BiCMOS technologies, operated under industry-like conditions, 24/7, for the provision of prototypes and low-volume production runs.
- 0 Qualified technological platform with direct access for science and industry
- 0 Vertical structure from material research to system architecture
- 0 350+ employees, 40+ nationalities



Vision

"We create foundations and prototype applications based on future silicon-based technologies and systems for a digitalized and networked world as well as for the sustainable preservation of our natural living conditions."

130nm SiGe BiCMOS Technologies for RF Applications



	SG13S	SG13G2	SG13G3Cu
HBT f_t/f_{max}	250 / 340 GHz	350 / 450 GHz	470 / 650 GHz
$W_{Emitter}$	170 nm	130 nm	110 nm
HBT BV_{CEO}	1.7 V	1.6 V	1.5 V
CMOS node	130 nm		
Active devices	Schottky diodes, Antenna diodes, PN diodes, ESD		
Varactors	NMOS Varactor		
MIM Caps	Poly-Si, Thin Film 1.5 fF / μm^2 (Al) 2.1 fF / μm^2 (Cu)	Poly-Si, Thin Film 1.5 fF / μm^2 (Al) 2.1 fF / μm^2 (Cu)	Poly-Si 2.1 fF / μm^2
Metallization	7 Layers AL incl. 2 & 3 μm layers or *Cu: 4 + 2 (3 μm) Al: 2 (3 μm)	7 Layers AL incl. 2 & 3 μm layers or *Cu: 4 + 2 (3 μm) Al: 2 (3 μm)	*Cu: 4 + 2 (3 μm) Al: 2 (3 μm)

*Cu BEOL from X FAB

- SG13G2 technology was selected for the development of an open source PDK

- 0 Target are high-end technology developments, low volume market introduction, technology transfer for potential mass production in commercial fabs
- 0 SG13S & SG13G2 are qualified and ready for Low Volume of high end products
- 0 SG13G3Cu is early access - qualification scheduled 2025

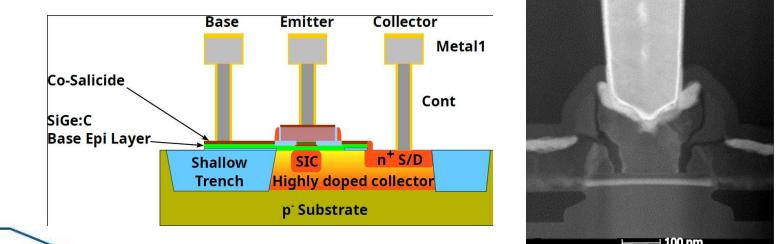


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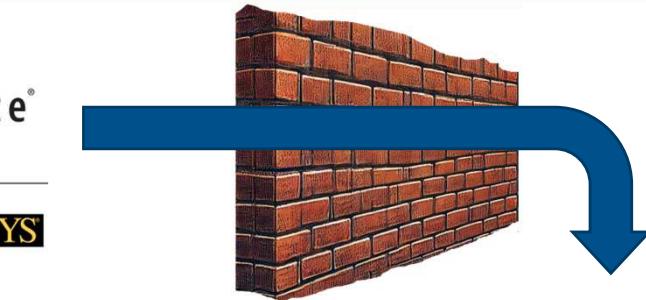
Traditional ASIC development (academic perspective)



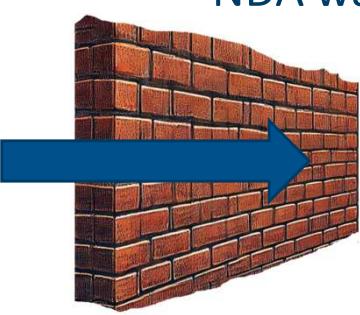
Existing IP blocks



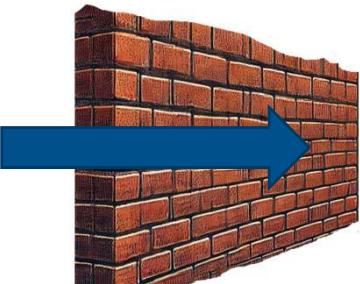
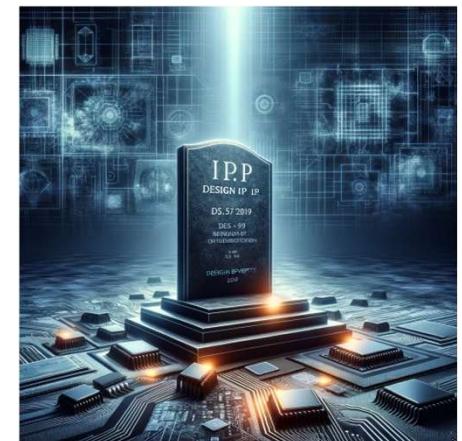
Foundry



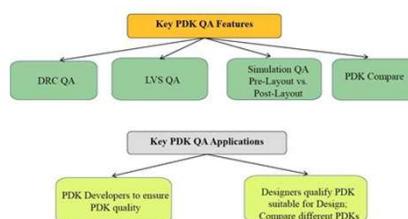
NDA walls



Designer

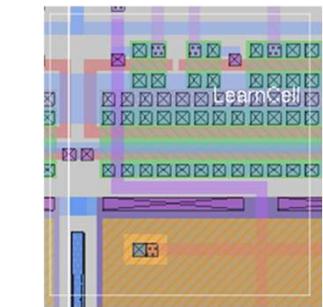


PDK

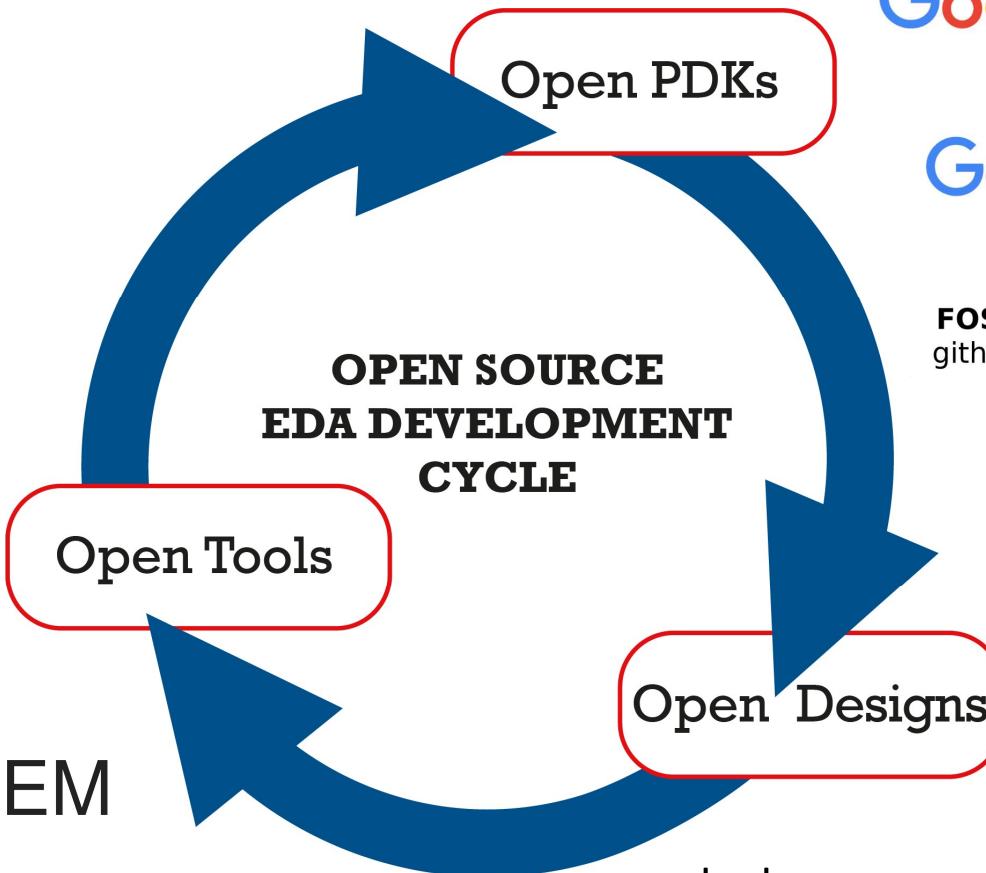


Flexibility is wanted

Open source ASIC development as an alternative



XSCHEM



Google + SKYWATER TECHNOLOGY

Google + GLOBAL FOUNDRIES

FOSS 180nm Production PDK
github.com/google/gf180mcu-pdk



IHP-Open-PDK



test cases, regression tests, benchmarks, use cases,
user stories, feedback, error reports, feature requests

IHP Open PDK on github



IHP-GmbH / IHP-Open-PDK

Type / to search

Issues 135 Pull requests 19 Discussions Actions Projects 1 Wiki Security Insights Settings

IHP-Open-PDK Public Edit Pins Unwatch 30 Fork 96 Star 560

dev 2 Branches 2 Tags Go to file Add file Code

This branch is 162 commits ahead of main .

KrzysztofHerman Merge pull request #559 from FlinkbaumFAU/remove_verilogp... 961 Commits · 1 hour ago

.github Update the klayout installation for actions 5 months ago

ihp-sg13g2 Merge pull request #559 from FlinkbaumFAU/remove_verilo... 1 hour ago

About 130nm BiCMOS Open Source PDK, dedicated for Analog, Mixed Signal and RF Design

ihp-open-pdk-docs.readthedocs.io open-source pdk ihp

Readme

Preview Mode

A screenshot of the GitHub repository page for "IHP-Open-PDK". The page shows various repository statistics and navigation links. A large watermark reading "Preview Mode" is overlaid across the middle of the page. On the right side, there is an "About" section describing the repository as a "130nm BiCMOS Open Source PDK, dedicated for Analog, Mixed Signal and RF Design". Below this, there is a link to the documentation at "ihp-open-pdk-docs.readthedocs.io" and several tags: "open-source", "pdk", and "ihp". A QR code is also present on the right.

Minimal installation – plug and play approach

Working with the IHP Open PDK



Welcome to IHP 130nm BiCMOS Open Source PDK documentation!

• Warning

This documentation is currently a work in progress.



Current Status – Experimental Preview



- Search docs
- PDK Contents
- Installation
- Process Specifications
- Layout Rules
- Analog Design
- Digital Design
- Physical & Design Verification
- Contribution
- References



1. Dependencies

The tools supported by IHP-Open-PDK are open source and are not always distributed as binaries or through packages available to install using programs such as apt-get. In order to use the tools one have to compile/build it from the sourc code usually available on platforms like github, gitlab, sourcforge codeberg. Having all the build tools installed and meeting all necessary dependencies the installation program is usually straightforward.

1.1. Build tools

The first step to build a tool/program from a source code is to have build tools, what means necesary compilers and make systems, which allows the user to build the source code.

```
sudo apt-get install -y build-essential  
sudo apt-get install -y qtbase5-dev qttools5-dev  
sudo apt-get install -y clang cmake libtool autoconf  
sudo apt-get install -y python3 python3-dev python3-pip python3-virtualenv python3-venv  
sudo apt-get install -y ruby ruby-dev
```

1.2. Useful tools

Before performing installation from sources it is recommended to install some tools that are useful:

```
sudo apt-get install -y btop tree xterm graphviz git  
sudo apt-get install -y octave liboctave-dev
```

Ubuntu 22.04 + compatible

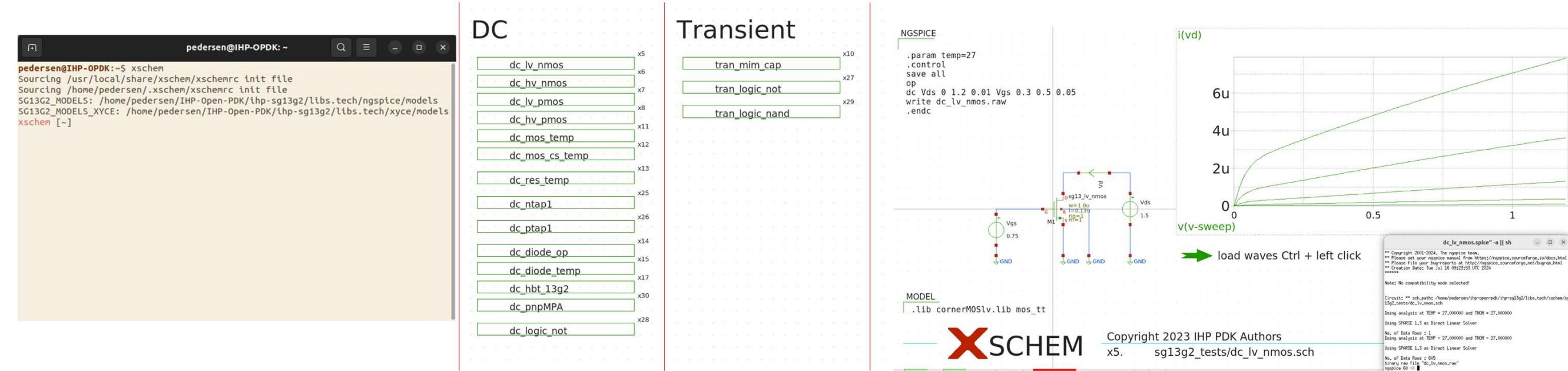
Configuration: \$PDK_ROOT, \$PDK

Dependencies installation: mainly apt-get

Tools have to be installed (binaries, sources)



Getting started really isn't that hard!



Some of the Information Available in ChatGPT



1. Process Technology

- Overview of advanced semiconductor technology, including high-performance devices and integrated components
- Offers various modules for expanded functionality

2. Multi-Project Wafer (MPW) Services

- Includes details on pricing, schedules, and supported processes
- Specifies chip area requirements and approval process for smaller designs

3. Layout and Process Specifications

- Defines design rules, device specifications, and physical constraints
- Includes details on available materials and process layers



Design examples and courses



IHP-GmbH / IHP-AnalogAcademy

Code Issues 32 Pull requests Actions Projects

IHP-AnalogAcademy Private

main ▾ 2 Branches 0 Tags

OS-EDA / Course

Code Issues 3 Pull requests Projects Wiki Security Insights



Course Public

main ▾ 1 Branch 10 Tags

Go to file

Course instance: 1 Week, hands on

Mon	Tue	Wed	Thu	Fri
L1: Introduction T1: Training	Q1, Q2: Recap Feedback L3: Verilog T3: Training	Q3, Q4: Recap Feedback L5: PDK T5: Training	Q5, Q6: Recap Feedback L7: OpenROAD Flow scripts T7: Training	Q7: Recap L8: Tapeout Feedback
L2: OpenROAD tools T2: Training	L4: OpenROAD first run T4: Training	L6: OpenROAD GUI T6: Training	L7: OpenROAD Flow scripts 2 T7: Training	Spare time and Wrap-Up

L : Lectures

T : Training and Hands-On

Q : Questions

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- [Introduction to IHP Open PDK and SG13G2 Technology](#)
- [Foundations](#)
- [Bandgap Reference](#)
- [50GHz Medium Power Amplifier](#)
- [8-bit SAR ADC](#)
- [Final Thoughts](#)

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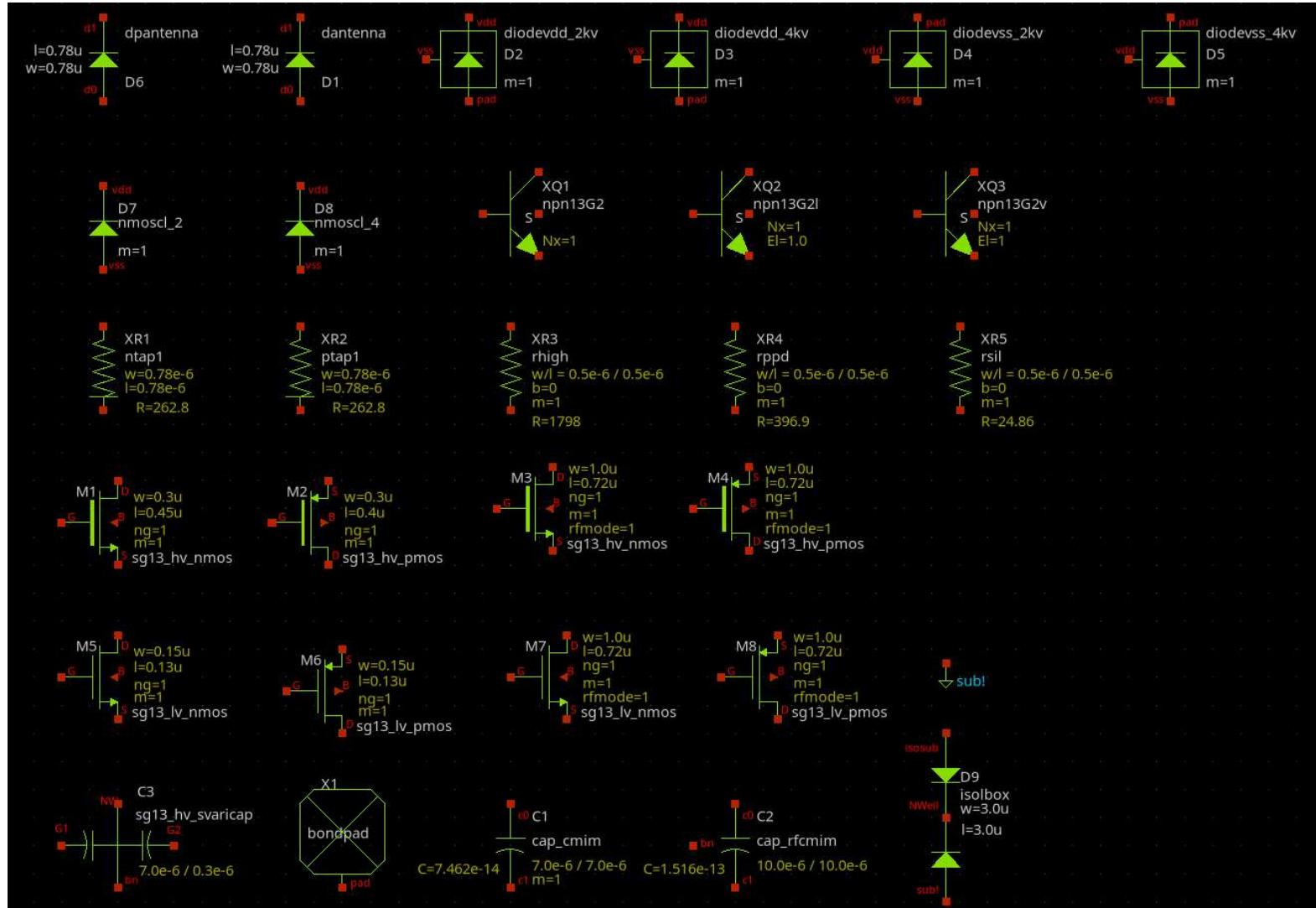
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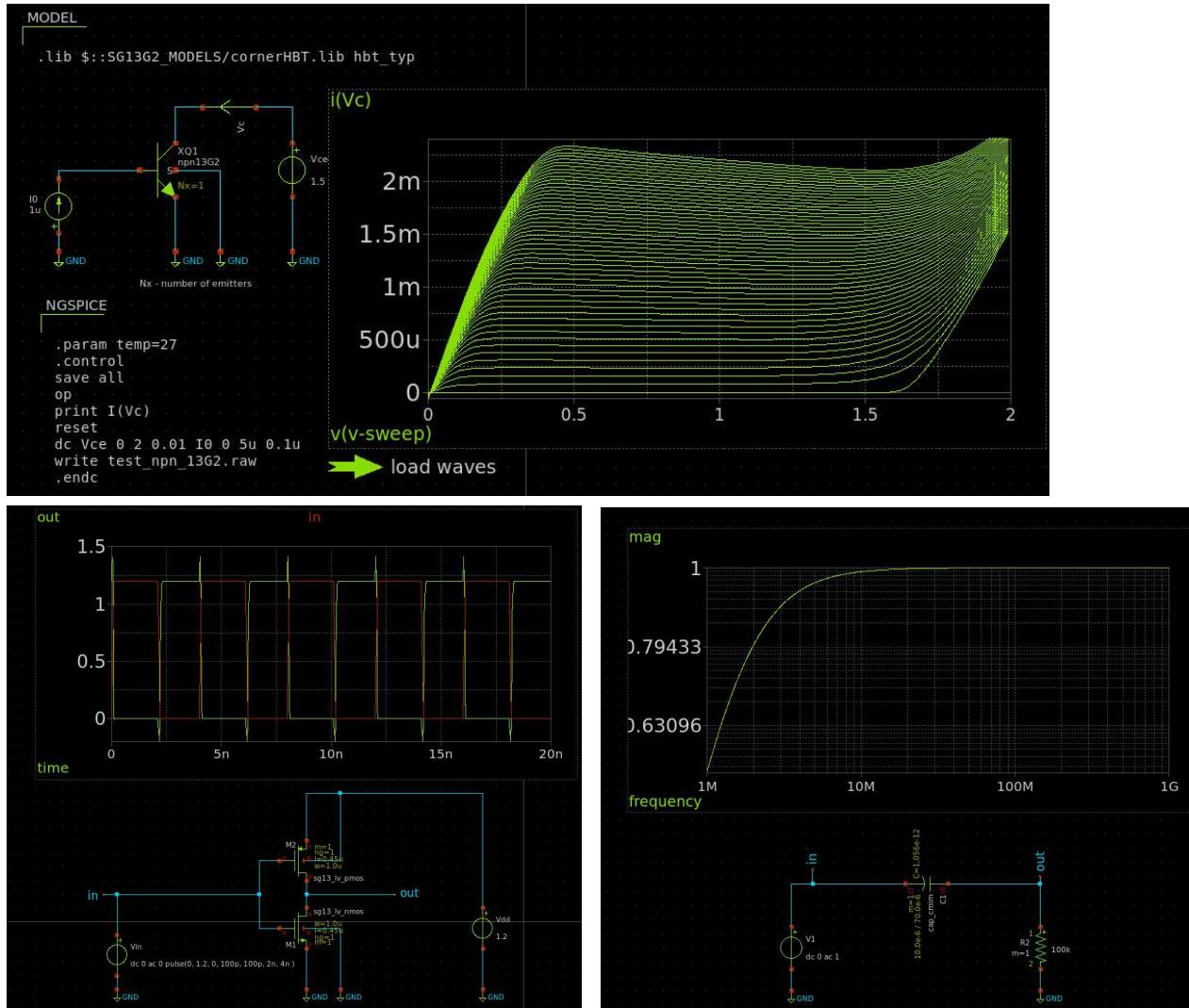
OpenPDK support for schematic capture



The current version of the IHP OpenPDK supports:

- xschem primitives for schematic capture
- automatic ngspice/Xyce compatible netlist generation
- example use cases to show the basic functionalities and parameters of the primitives

OpenPDK support for simulations



Analog simulation facilities:

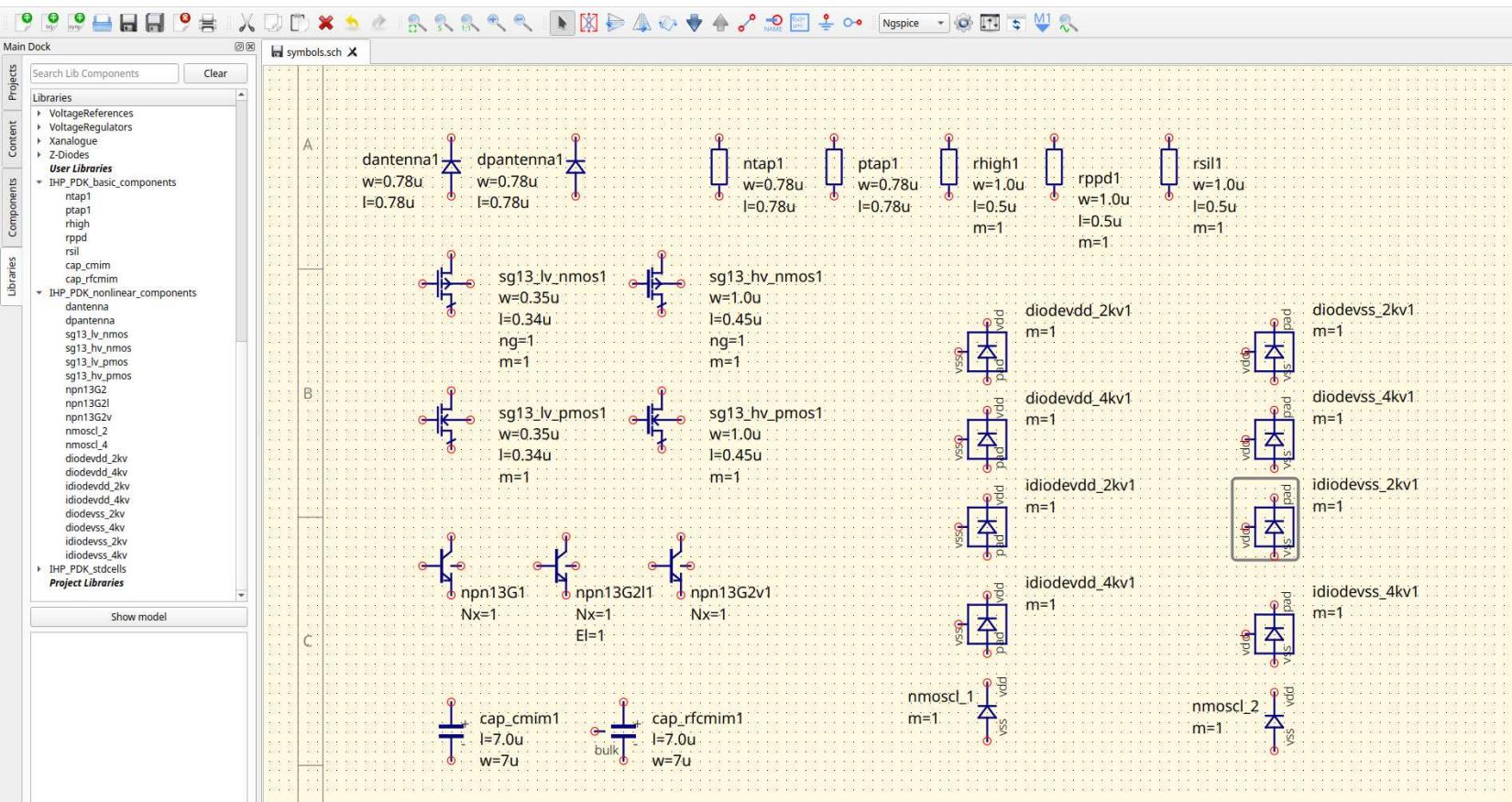
- PSP103.6 MOSFET models from SemiMod,
- ngspice/Xyce compatible netlists,
- process corners: typical, best case, worst case,
- statistics related to the process variation,
- simulation examples segmented by simulation type: DC, TRAN, AC, MonteCarlo, S-parameters
- postprocessing python scripts,
- model extensions for RF frequency range,
- ngspice 40+ compatible

OpenPDK support for Qucs-S schematic capture

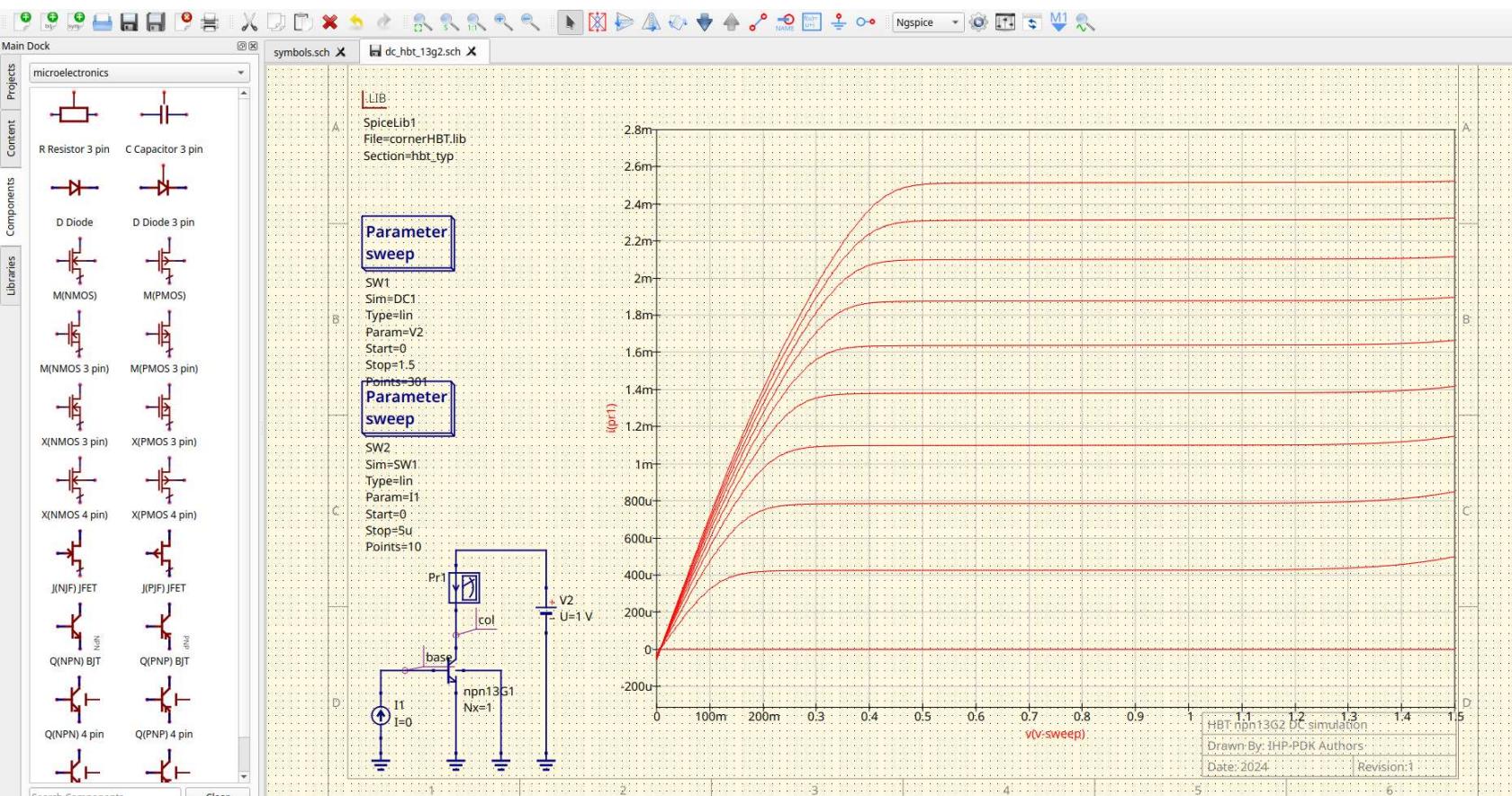


The current version of the IHP OpenPDK supports:

- o primitives for schematic capture
- o automatic ngspice/Xyce compatible netlist generation
- o example use cases to show the basic functionalities and parameters of the primitives
- o XSPICE model support (under development)



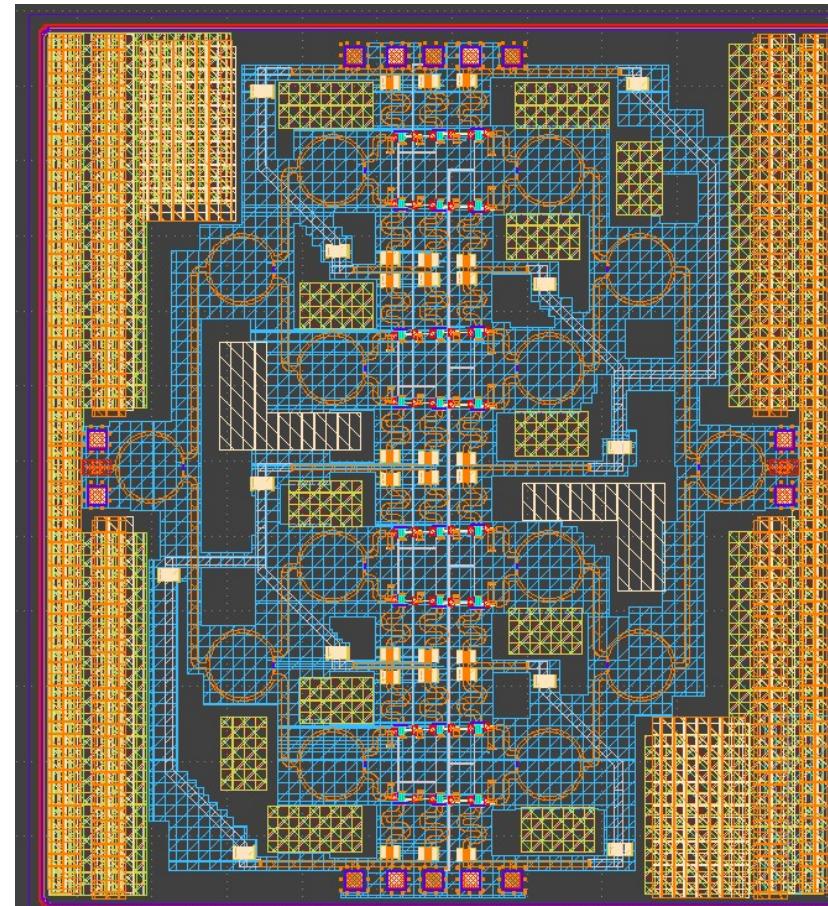
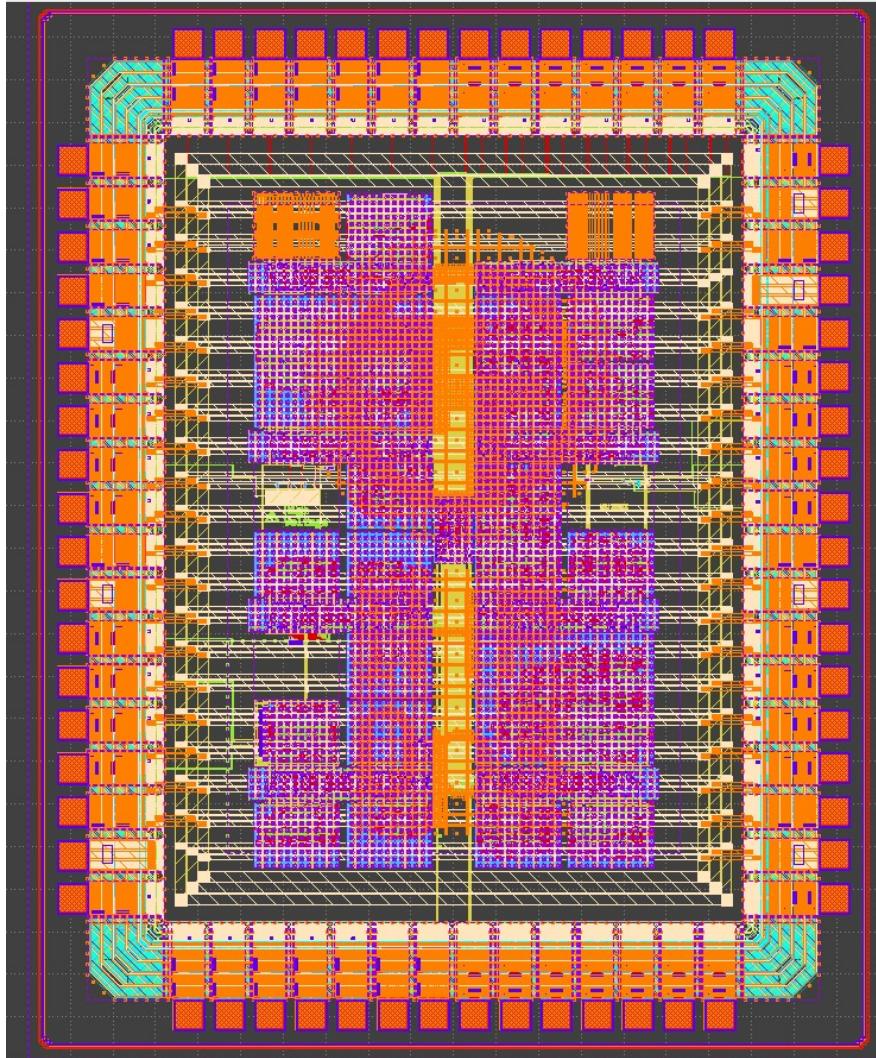
OpenPDK support for Qucs-S schematic capture



Qucs-S development:

- 0 Agnostic support for PDK
- 0 CDL netlisting
- 0 Interoperability with OpenEMS and Klayout
- 0 XML symbol library import
- 0 RF related features

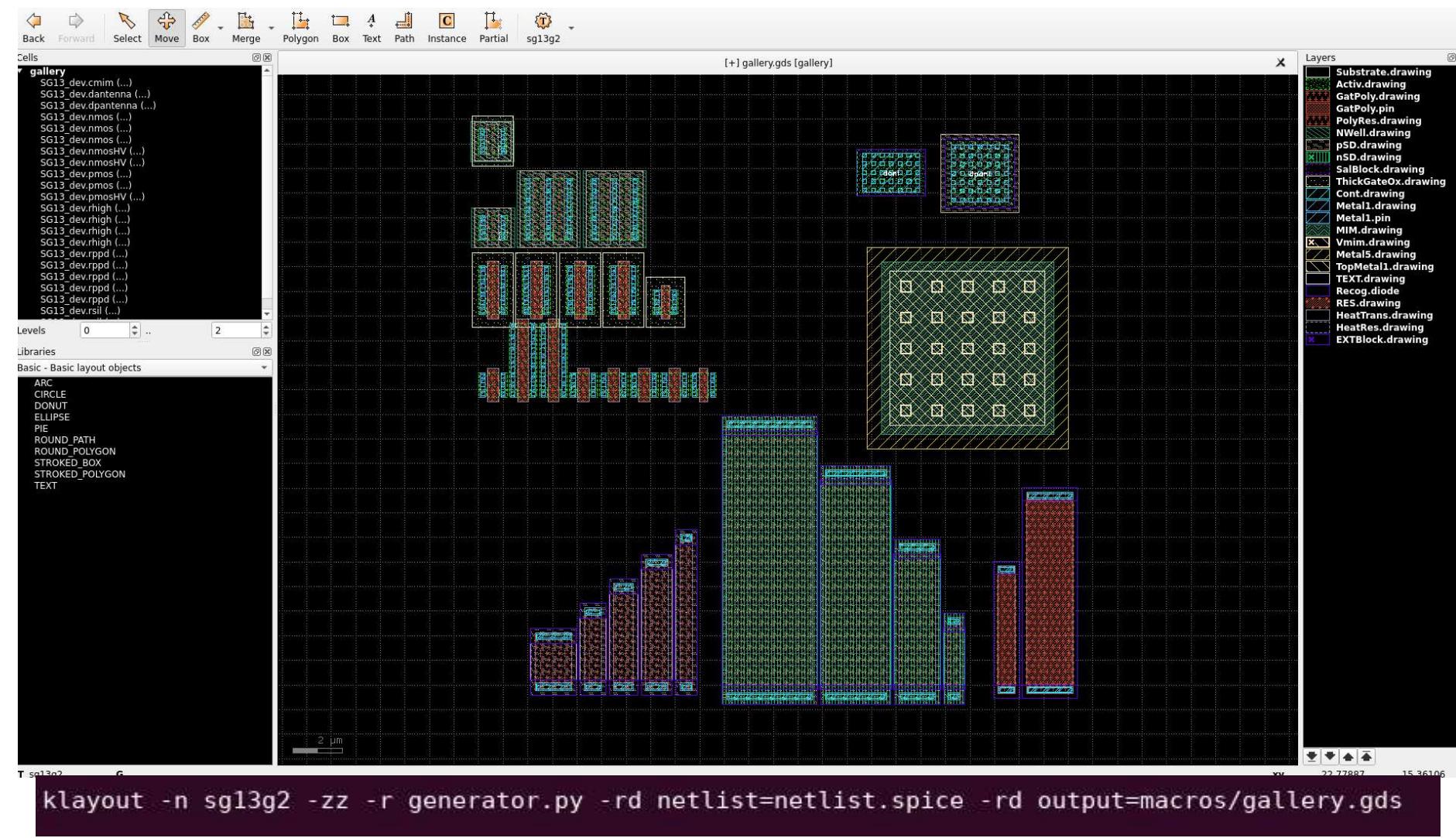
KLayout – primary tool for open source layout design



KLayout key features:

- o hierarchical view
- o parametric cell support
- o DRC/LVS checks
- o command line batch mode
- o XOR and DIFF tools
- o Custom scripts in Python/Ruby
- o Plugins

KLayout – Pycell support



- o Pycells compatible with Synopsys PyCell Studio and Keysight ADS
- o KLayout wrapper API development
- o Klayout Device generator

KLayout example DRC run on `gatpoly` QA cell



The screenshot shows the KLayout 0.28.12 interface with a project named "sg13g2_qacells.gds [gatpoly]".

Cells: The "gatpoly" cell is selected.

Layers: A list of layers including Activ.drw, GatPoly.drw, Cont.drw, Metal1.pin, pSD.drw, NWell.drw, Substrate.drw, ThickGateOx.drw, and TEXT.drw.

Marker Database Browser:

Cell / Category	Count (Not Visited)
By Cell	37 (35)
[gatpoly]	37 (35)
aFil.g	1
aFil.g2	4 (4)
GFil.g	1
Gat.d	8 (8)
M1.j	1 (1)
M1Fil.h	4 (4)
Gat.a	12 (12)
Gat.b	6 (6)
By Category	37 (35)
All	37 (35)

Info: Min. GatPoly to Activ space = 0.07

KLayout example LVS run on sg13_lv_nmos mosfets



Netlist LVS

... on layout sg13_lv_nmos.gds

▶

Netlist Schematic Cross Reference Log

Circuits Objects Layout Reference

sg13_lv_r sg13_lv_nmos ↔ \$ sg13_lv_nmos SG13_LV_NMOS

- ▶ -D Pins
- ▶ ↑ Nets
- ▼ ↴ Devices
 - ▶ ↴ sg13_lv_nn \$11 / sg13_lv_nmos [L=(N1 / SG13_LV_NMOS [L=0.13, W=0.15]
 - ▶ ↴ sg13_lv_nn \$12 / sg13_lv_nmos [L=(N2 / SG13_LV_NMOS [L=0.13, W=0.2]
 - ▶ ↴ sg13_lv_nn \$14 / sg13_lv_nmos [L=(N3 / SG13_LV_NMOS [L=0.15, W=0.2]
 - ▶ ↴ sg13_lv_nn \$9 / sg13_lv_nmos [L=0. N4 / SG13_LV_NMOS [L=0.15, W=0.3]
 - ▶ ↴ sg13_lv_nn \$6 / sg13_lv_nmos [L=0. N5 / SG13_LV_NMOS [L=0.3, W=0.3]
 - ▼ ↴ sg13_lv_nn \$13 / sg13_lv_nmos [L=(N6 / SG13_LV_NMOS [L=0.25, W=0.6]
 - ▶ -o S ↔ D ⚠ \$35 (1) D6 (2)
 - ▶ -o D ↔ S ⚠ \$36 (1) S6 (2)
 - ▶ -o G \$37 (1) G6 (2)
 - ▶ -o B \$1 (26) SUB (27)
 - ▶ ↴ sg13_lv_nn \$16 / sg13_lv_nmos [L=(N7 / SG13_LV_NMOS [L=0.15, W=0.6]
 - ▶ ↴ sg13_lv_nn \$4 / sg13_lv_nmos [L=3. _PATTERN_37 / SG13_LV_NMOS [L=3.74, W=5.55]
 - ▶ ↴ sg13_lv_nn \$5 / sg13_lv_nmos [L=4. _PATTERN_40 / SG13_LV_NMOS [L=4.6, W=7.09]

KLayout LVS ruledeck:

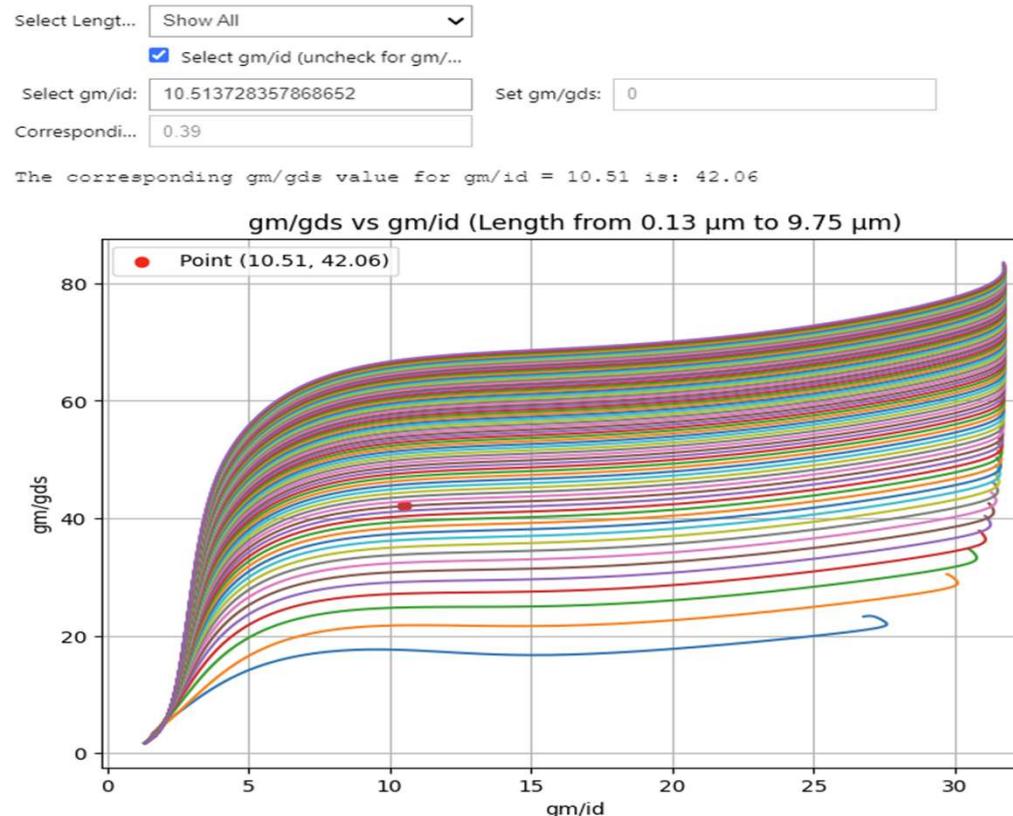
- accepts CDL netlist,
- extracts devices from layout,
- creates extracted netlist,
- performs checks and compares:
 - Pins
 - Nets
 - Devices
- reports inconsistencies
- can run in batch mode

OS tools for Advanced IC Design?



MOSFET Sizing with GM/ID Curves:

- 0 Using Python scripting alongside Ngspice to generate GM/ID curves for efficient MOSFET sizing



Mixed Signal Design

- 0 Verilator
- 0 Xspice
- 0 Creating digital models in conjunction with analog design

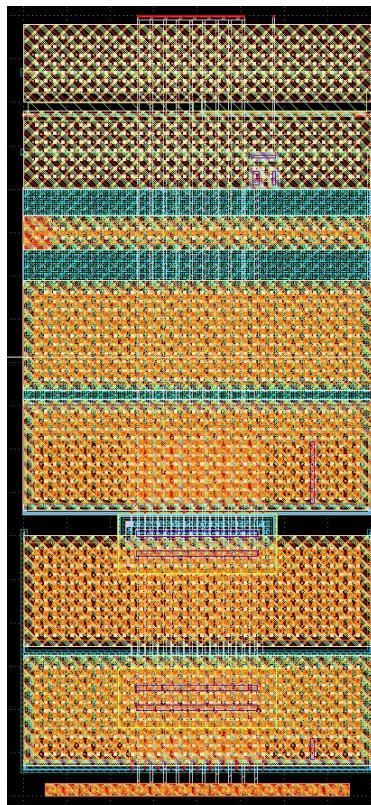
Layout Automation

- 0 Physical verification, filler scripts
- 0 Pcells generation from SPICE-Files
- 0 Streamlining the layout process

Digital primitives

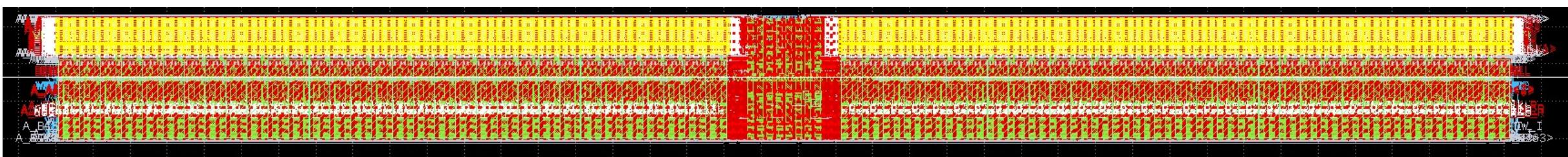
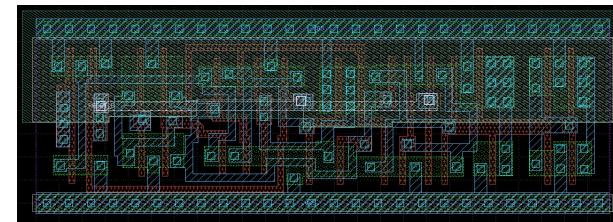


	StdCells	IOCells	SRAM
Verilog	x	x	x
LIB	x	x	x
LEF	x	x	x
CDL	x	x	x
SPICE	x	x	x
GDS	x	x	x

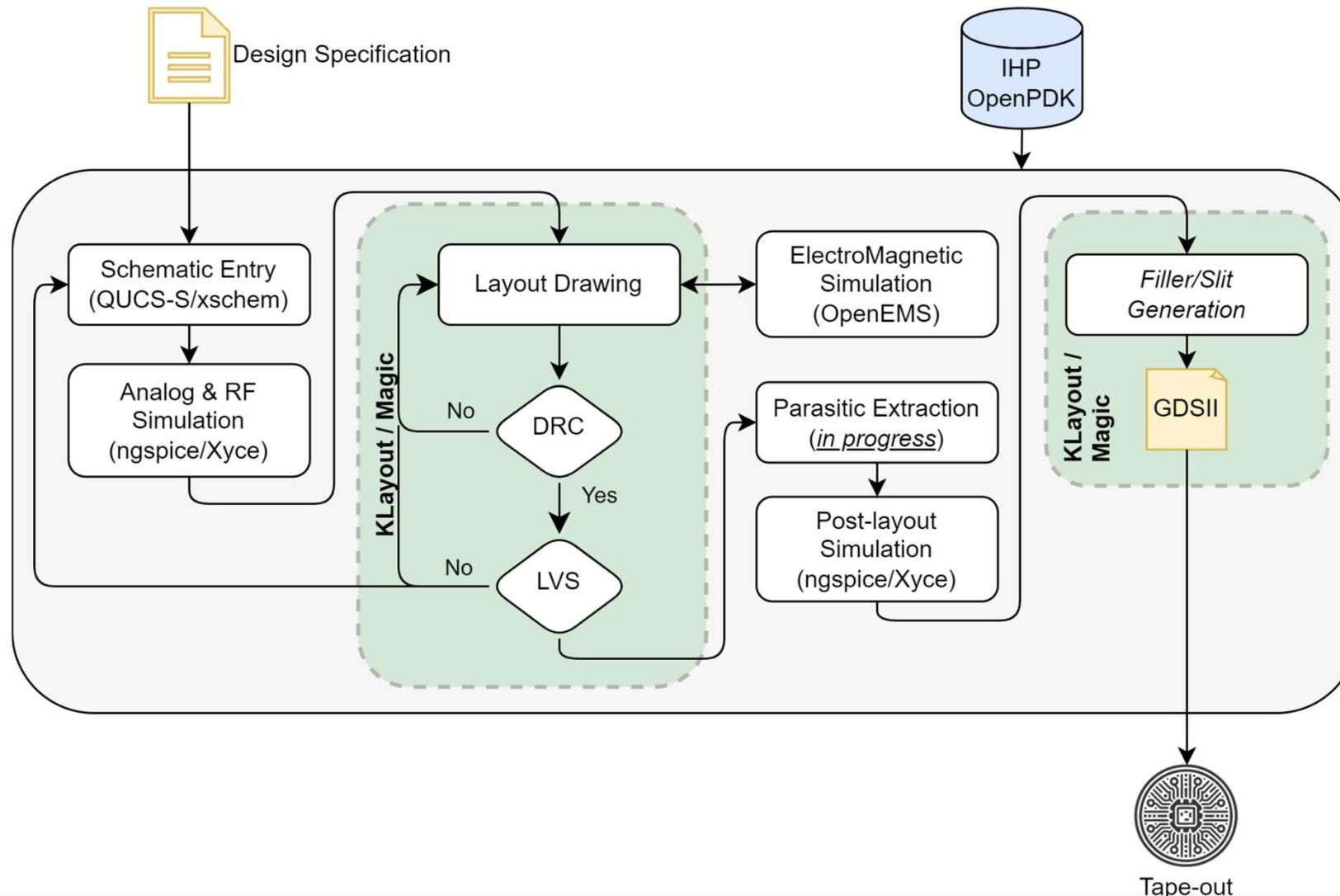


Digital components:

- o stdcells
 - o 84 cells,
 - o combinatorial logic,
 - o sequential elements,
 - o scan flops,
 - o gated cells.
- o IOCells,
 - o In, Out, InOut, Analog
 - o different drive strengths
- o SRAM
 - o hard macros of a single port SRAM
 - o different sizes

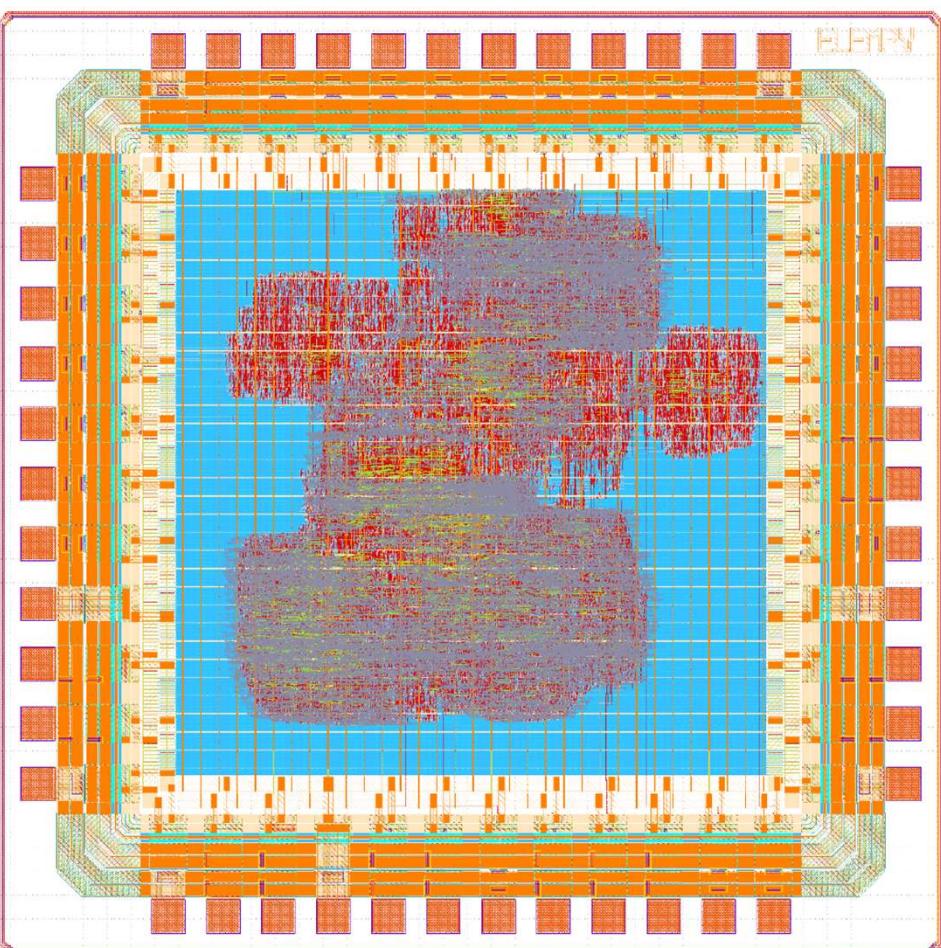


Analog/RF Open Source Design Flow: status at a glance

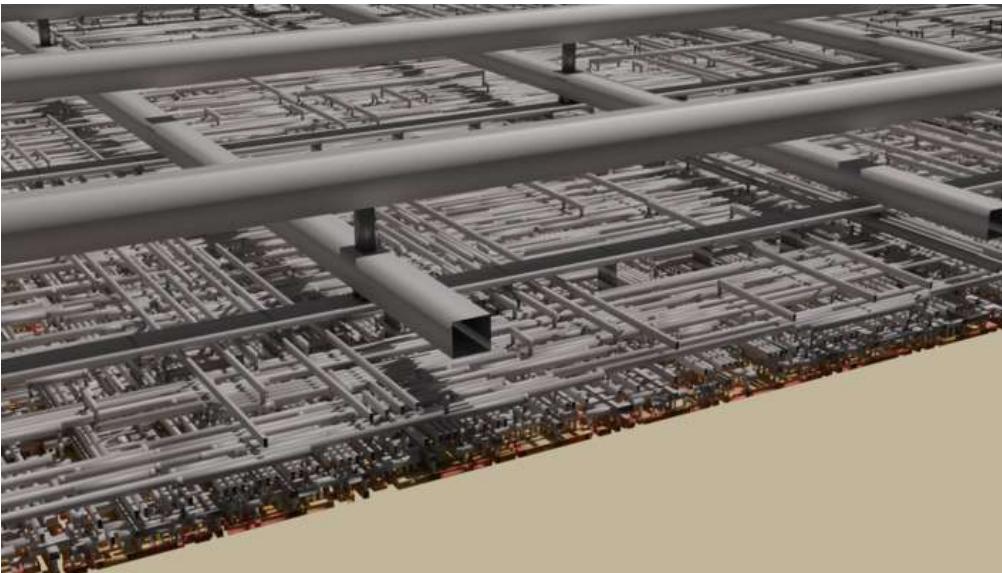


- 0 KLayout-oriented flow
 - 0 Layout design
 - 0 Parameterizable cells
 - 0 Physical Verification
- 0 QUCS-S, xschem
- 0 ngspice, Xyce
- 0 OpenEMS, ElmerFEM, AWS Palace
- 0 Working on a faster solver for EMS (ELMER)

Digital OpenROAD-flow-scripts Flow

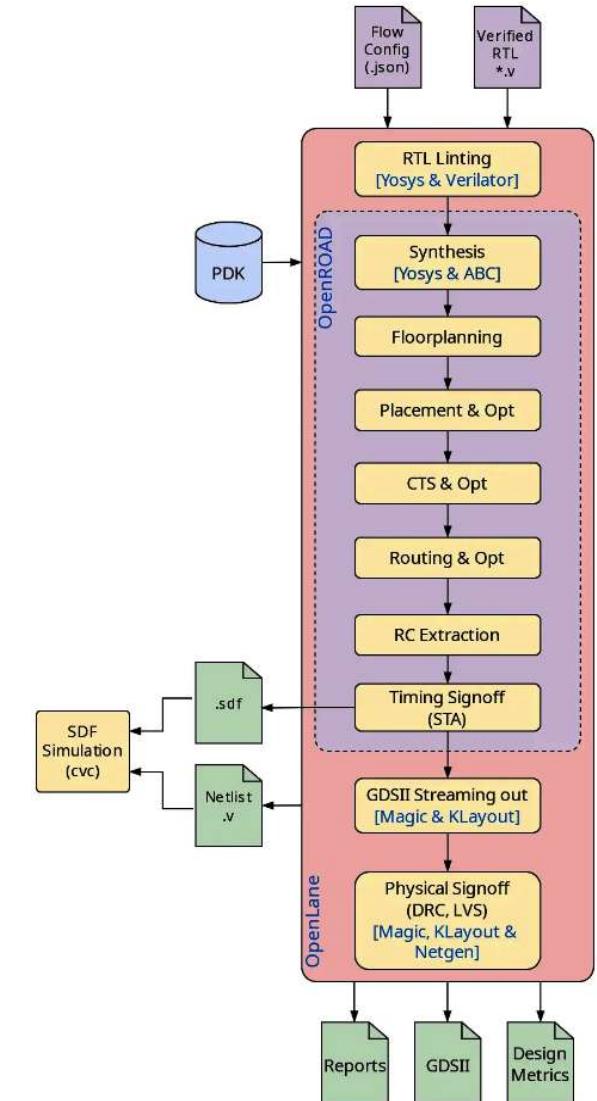
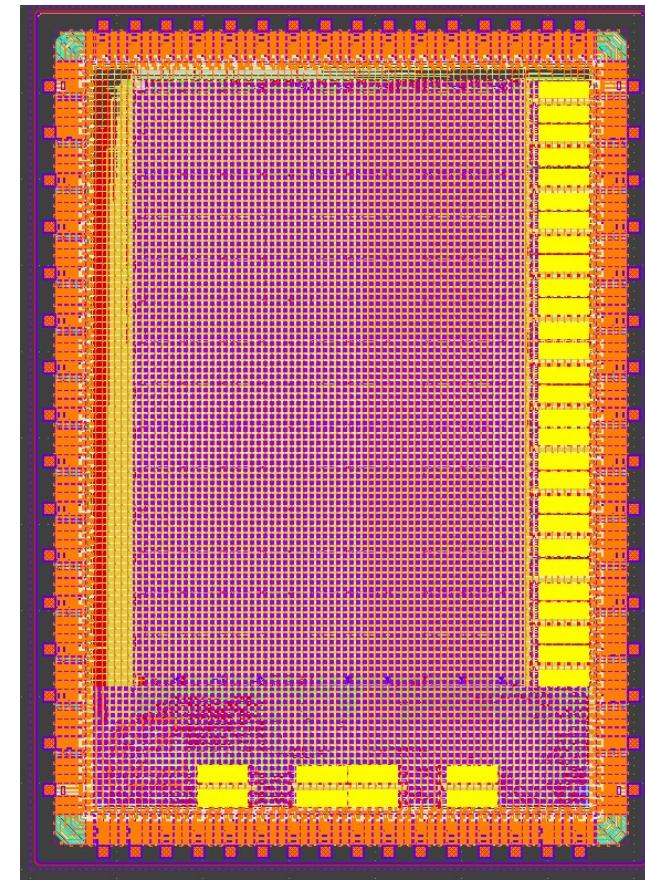
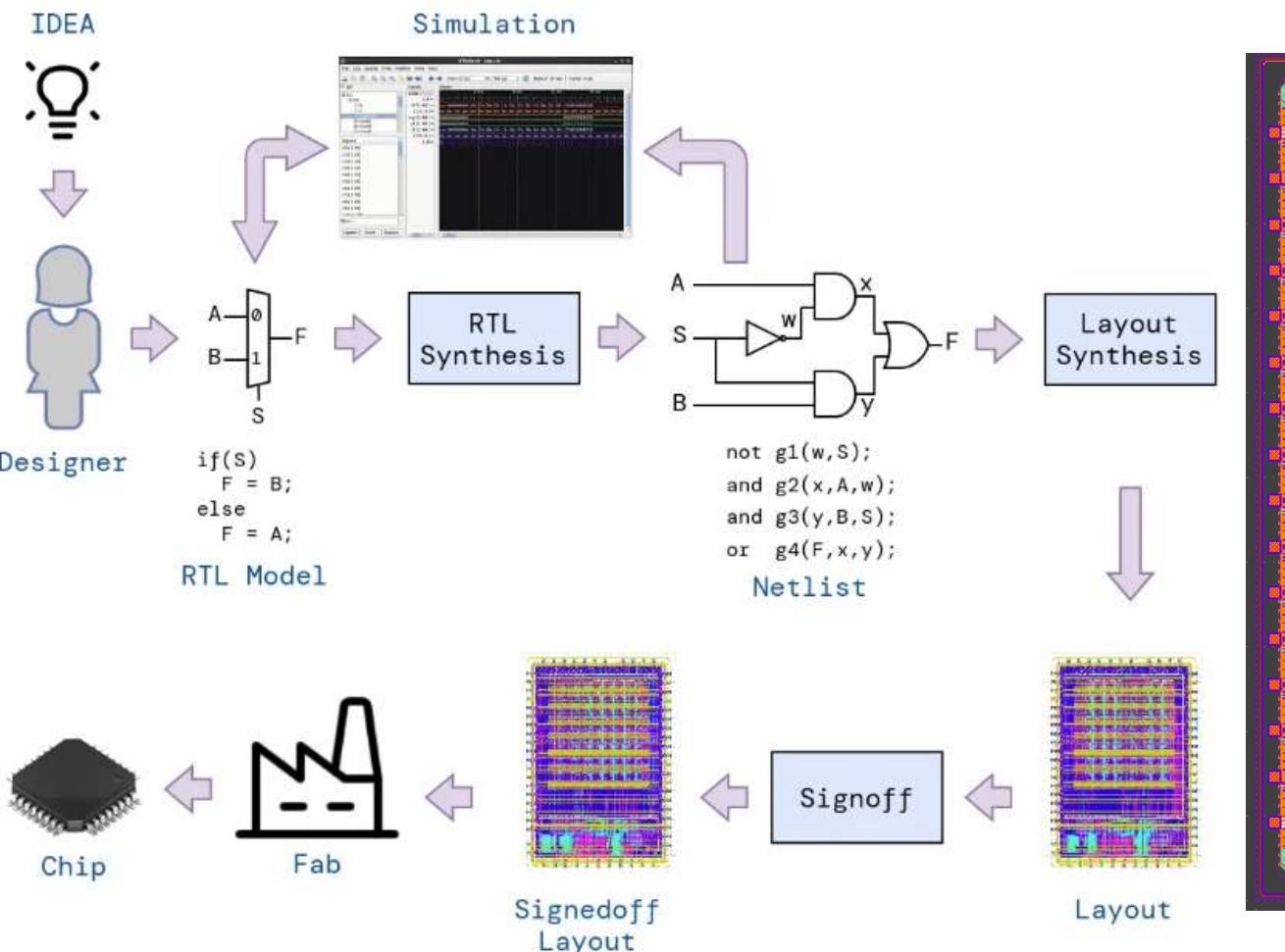


- o Yosys + ABC -> synthesis
- o OpenROAD -> PnR
- o Klayout -> GDS streaming+checks



<https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts>

Digital LibreLane flow



<https://github.com/librelane/librelane>

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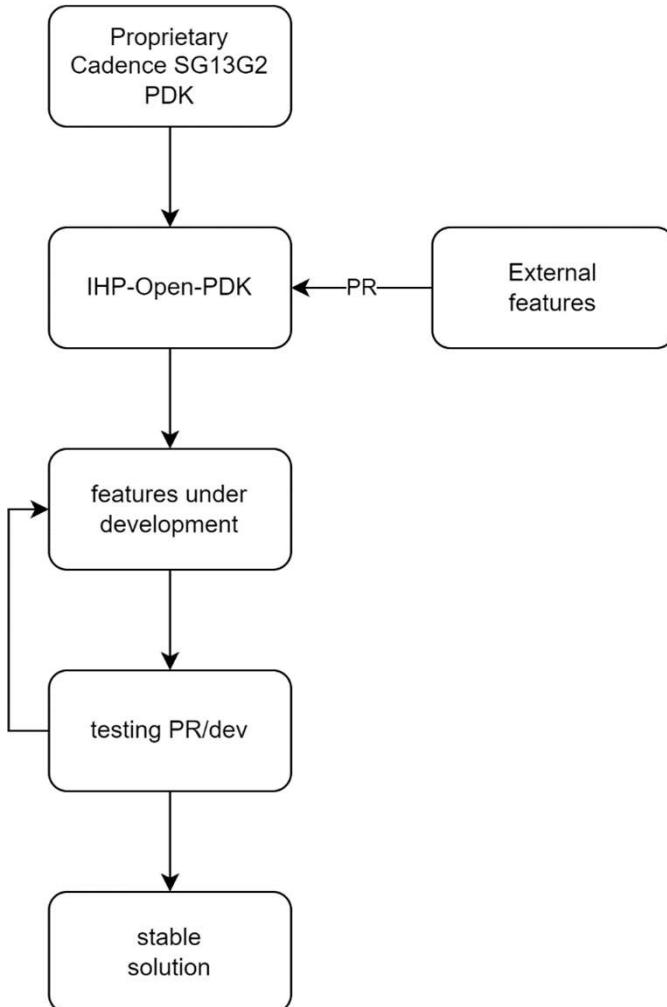
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PDK development cycle

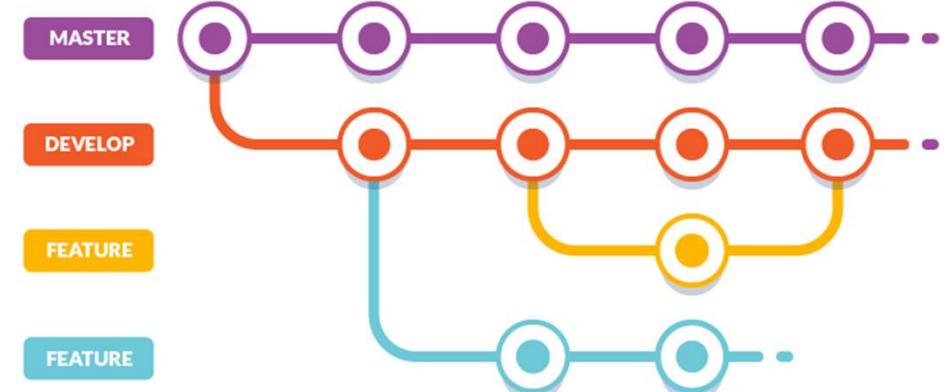


Principal rules

- Tight link between SG13G2 PDK and its open-source equivalent
- Compatibility with the open-source EDA tools
- Preserving the structure proposed in SKY130
- Read-only
- Based on git and following git flow

Key actors

- PDK core team
- Tools and flow developers
- Designers
- OS Community



PDK development cycle – community support



Issues 135 Pull requests 24 Discussions Actions Projects 1 Wiki

is:issue

Open 135 Closed 165 Author Labels

- Cannot run simulation on test scheme** #566 · by thonglinh90 was closed yesterday
- Questions about sealring For MPW shuttle runs** question #562 · EngGhaith opened 4 days ago
- Xyce plugins support limited to only 2 plugins** bug #560 · KrzysztofHerman opened 4 days ago
- Double prefix in stdcell names in verilog netlist created by xschem** bug #557 · by FlinkbaumFAU was closed 4 days ago
- Discrepancy in LVS Netlist Extraction for Parallel Capacitors** #555 · PhillipRambo opened last week

Issues 135 Pull requests 24 Discussions Actions Projects 1 Wiki

Filters ▾ is:pr is:open

Author ▾

- 24 Open** ✓ 231 Closed
- Code changes fixes the problem that Xyce/ADMS can't handle switch...** #568 opened 10 hours ago by dwarning
- Adding some updates for LVS run setup and actions** ✓ #567 opened yesterday by FaragElsayed2
- Stdcell update 2. Hot Fix 1.** ✓ #565 opened 3 days ago by b10346
- Changes in Act and GatPoly filler macro.** ✓ #564 opened 3 days ago by KrzysztofHerman
- Added bulk node to resistor models rhigh + rppd + rsil cont.** ✓ #563 opened 3 days ago by KrzysztofHerman • Draft
- Xyce plugins sourced from a plugin list** ✓ #561 opened 4 days ago by KrzysztofHerman • Draft

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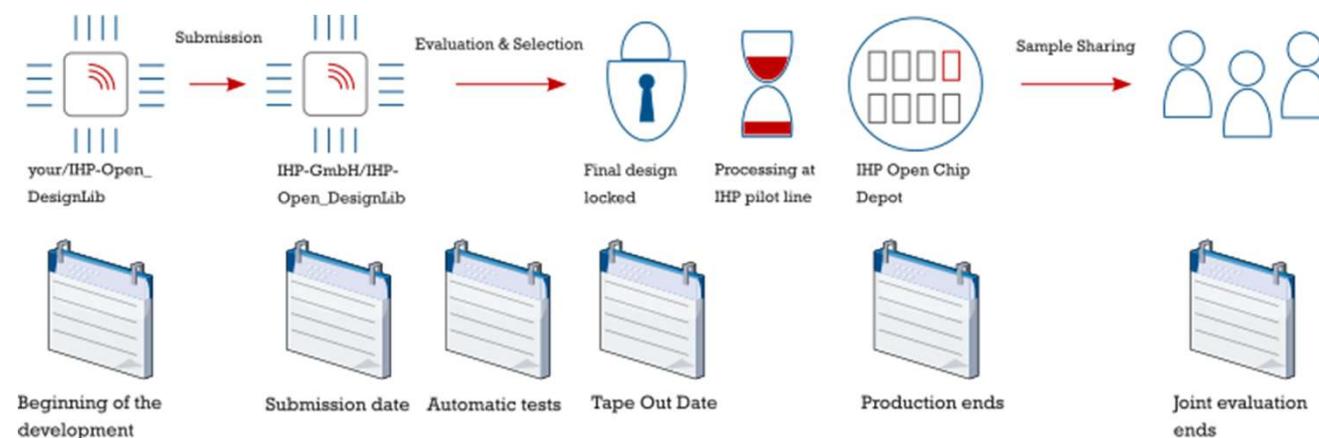
Lessons learned and future activities

Free MPW Runs - support open source PDK & design

- 0 The table provides schedule of MPW Runs for FMD-QNC project in 2025 and 2025

Tape out date	22/05/24	11/11/24	22/11/24	01/03/25	09/05/25	18/07/25	15/09/25
Technology	SG13G2	SG13CMOS	SG13G2	SG13G2	SG13G2	SG13G2	SG13CMOS
Area [mm ²]	10	220	20	140	30	30	220

For more details check: <https://ihp-open-ip.readthedocs.io/en/latest/>



- 0 Project funds can be used exclusively to produce chip designs for non-economic activities, such as university education, research projects, and others
- 0 A concept for sustainable provision of free or low-cost MPW area for the open source community is to be developed.



Criteria for design IP selection from open community

Mandatory criteria for IP selection

- Completeness of IP data (all data need to be open source)
- DRC error free designs
- Area below 2 mm² preferred (larger designs only if area is available)
- Potential export restrictions

Additional criteria for IP selection

- First time submission (preferred)
- Design should use open source tools supported by IHP open PDK
- For SG13G2 runs designs using SiGe (preferred)
- Documentation quality
- Uniqueness, not yet seen designs (i.e. if there were no ADCs before, an ADC design would get a higher point)



Flow to upload designs for MPW run

- 0 Before a design can be considered for fabrication start a pull request at https://github.com/IHP-GmbH/TO_<date>
- 0 All design data need to be submitted at **least 2 weeks** before TAPE OUT
- 0 Europractice will check designs regarding mandatory criteria (Completeness, DRC clean GDS, ...)
- 0 Europractice registers area and upload selected GDS files
- 0 Designs will be processed by IHP
- 0 IHP can rent samples for joint evaluation **under certain agreement (Continuation on next slide)**
- 0 Evaluation results need to be published on <https://github.com/IHP-GmbH/IHP-Open-DesignLib>
- 0 Evaluation to provide permanent samples are under evaluation

The principal goal is to build an open source design library for future projects



Low Cost Open MPW Runs

In order to maintain open source MPW IHP plans to have two OpenMPW runs per year

- 0 SG13CMOS – CMOS only run with AL BEOL where price „P“ in EUR is calculated based on total area (mm^2) „A“ booked

$$P = \begin{cases} 1500 & \text{if } A < 100 \\ 150000/A & \text{if } 100 \leq A \leq 150 \\ 1000 & \text{if } A > 150 \end{cases}$$

- 0 SG13G2 – fully featured G2 with AL BEOL at approx. 2800 EUR/ mm^2

The above mentioned prices refer to the open-source designs, where all the views are compatible with the open source EDA tools.

For customers who do not wish to disclose their IP, we offer participation in the OpenMPW program at a 20% discount off the regular price, as the wafers can be shared with other customers.

The turn around processing time is approx. 6 months for CMOS - 8 months for BiCMOS

The typical offer includes 20 bare die samples. Packaging will be offered on request (additional fee can be applied)

The first run can take place Nov 2025 (CMOS)

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Introduction to the IHP

Our motivation and goals in the open source silicon domain

Description of the open source solutions developed and supported by IHP

Understanding the power of the community

Planification of Open MPW runs

Lessons learned and future activities

Key takeaways



- o Strong open-source community and interest
- o The open source enables and facilitates education and collaboration
- o OS tools develops your understanding of semiconductor manufacturing
- o Chip design demystification - hands on experiences
- o EDA tools well oriented to support open source PDK's, but still a lot to be implemented (get involved)
- o Open source Design library is still missing (get involved!)
- o Our team is growing, check out the open positions

Work in progress – analog/mixed/RF flow

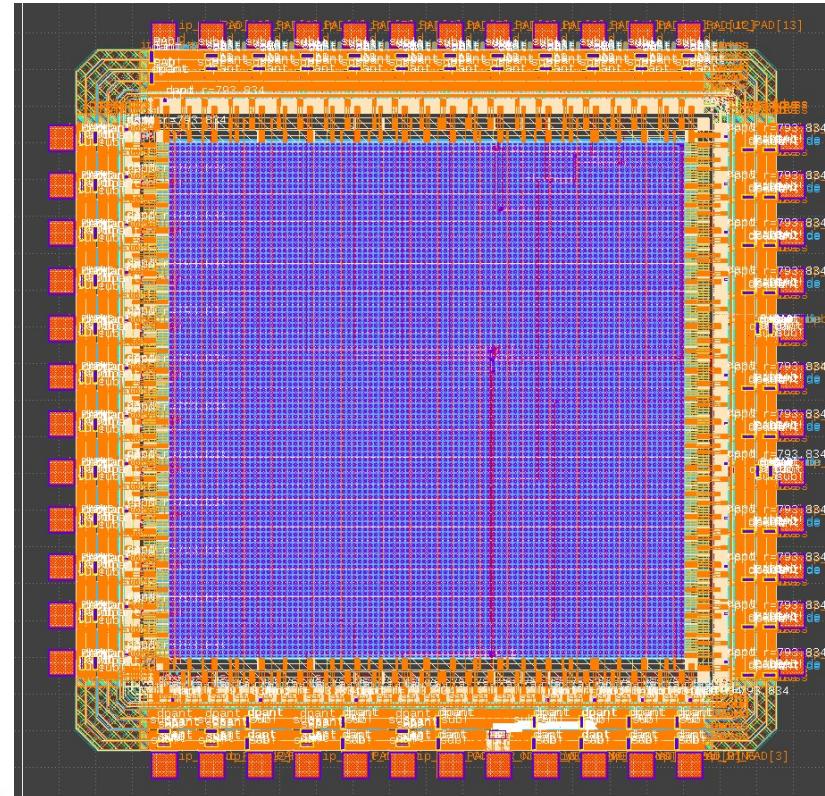


- 0 Parasitics Extraction PEX – ongoing, <https://github.com/martinjankoheler/klayout-pex>
- 0 Noise modeling in ngspice (transient noise, low frequency noise) – ongoing
- 0 Qucs-S support – ongoing, agnostic PDK support, RF features
- 0 Device models – issues found and reported by community members, migration to Verilog-A behavioral models
- 0 New and fast DRC ruledeck for klayout
- 0 OpenEMS integration for EM field solving
- 0 Mixed mode testcases using xspice + verilator

Full chip design example

- OpenROAD-flow-scripts does not provide full chip design example
- Padring design can be a tedious thing
- <https://github.com/KrzysztofHerman/orfs-design-template>

Cell / Category		Count (Not Visited) - Waived
▼ By Cell		
▼ [ihp_top]		
AFil.g		102 (101)
AFil.g2		102 (101)
M1.j		1 (1)
M2.j		11 (11)
M3.j		1 (1)
M4.j		1 (1)
M5.j		1 (1)
M1Fil.h		11 (11)
M2Fil.h		36 (36)
M3Fil.h		14 (14)
M4Fil.h		14 (14)
M5Fil.h		9 (9)
TM2.c		1
▶ By Category		
All		102 (101)
		102 (101)



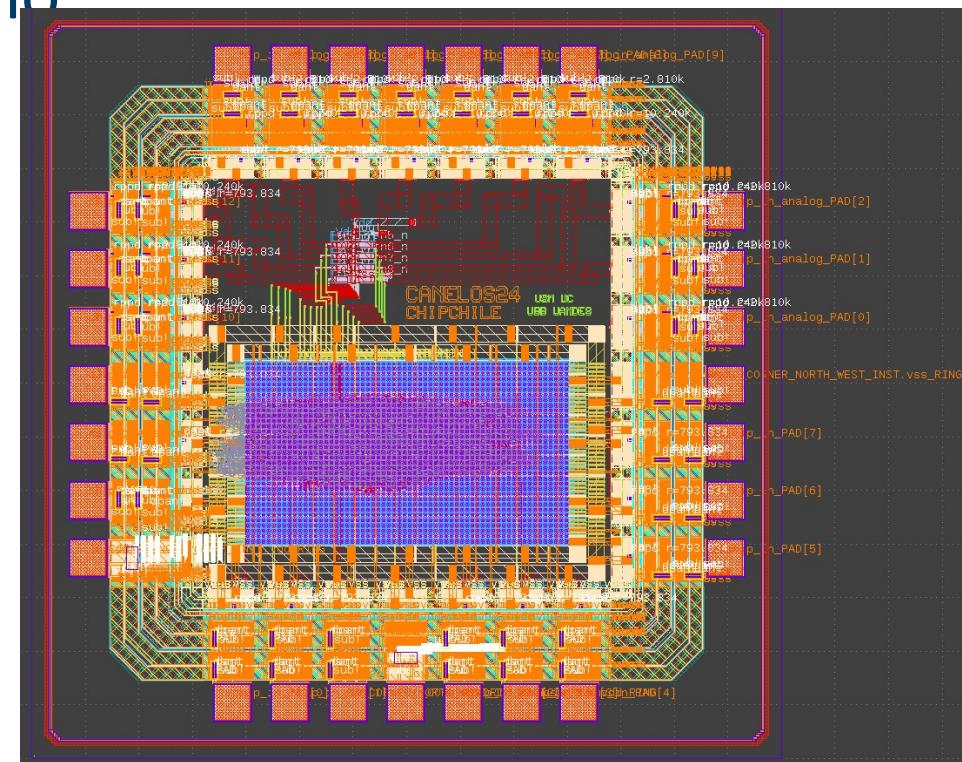
Mixed signal design using Ngspice



- NGSPICE is capable to handle a mixed mode simulation using shared object generated by Verilator from Verilog behavioral code.

<https://canelosworkshopihp2025-docs.readthedocs.io>

- o 8:1 analog mux
 - o SPI interface
 - o neural network



How to reach us



Email

-o openpdk@ihp-microelectronics.com



GitHub

-o issues – for reporting issues, questions

-o discussions – for requesting features

Open Source Fossi-Chat.org channel:

#ihp-sg13g2

-o general discussions

-o announcements



The screenshot shows the GitHub repository for IHP-GmbH / IHP-Open-PDK. The Code tab is selected, showing 135 issues, 19 pull requests, and 1 discussion. The discussion thread includes a question about a cross-section diagram and a reply confirming there are no inductors available. It also shows a schematic of a ring oscillator with component dimensions labeled.

Acknowledgment



- 0 Thanks to my colleagues at IHP and all the people involved in the development of the PDK
- 0 And special thanks to the following public founded German projects:
 - 0 VE-HEP (16KIS1339K) <https://elektronikforschung.de/projekte/ve-hep-1>
 - 0 IHP Open130-G2 (16ME0852) <https://www.elektronikforschung.de/projekte/ihp-open130-g2>
 - 0 FMD-QNC (16ME0831) <https://www.elektronikforschung.de/projekte/fmd-qnc>



Thank you for your attention!

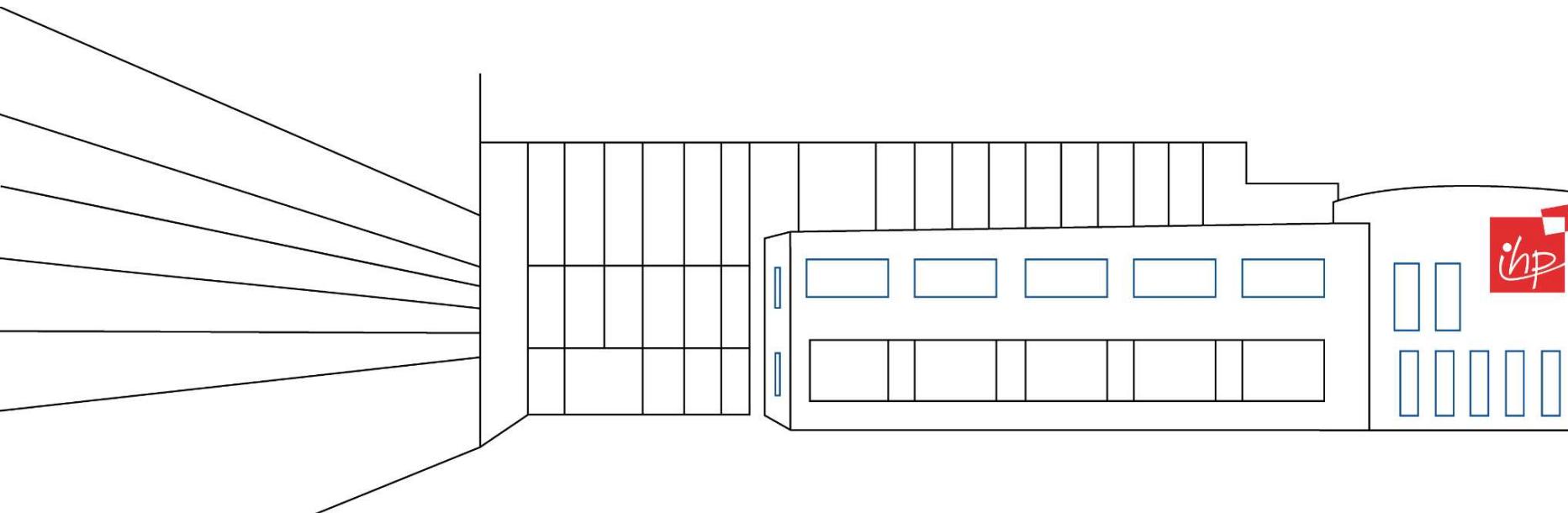
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