Open-Source IC Design Workshop

2.2 Simple layout-level design: transmission gate

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AC3E

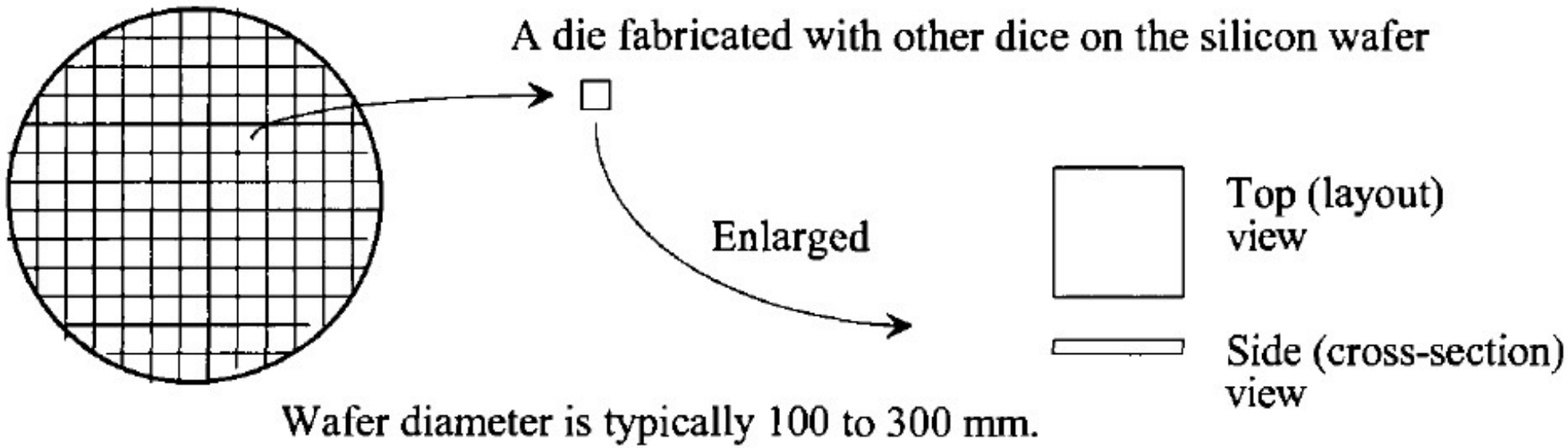
UCU Universidad Católica del Uruguay

Agenda

- Introduction: layout basics
- Transmission gate layout
- Task: Tgate + inverter layout

Introduction: layout basics

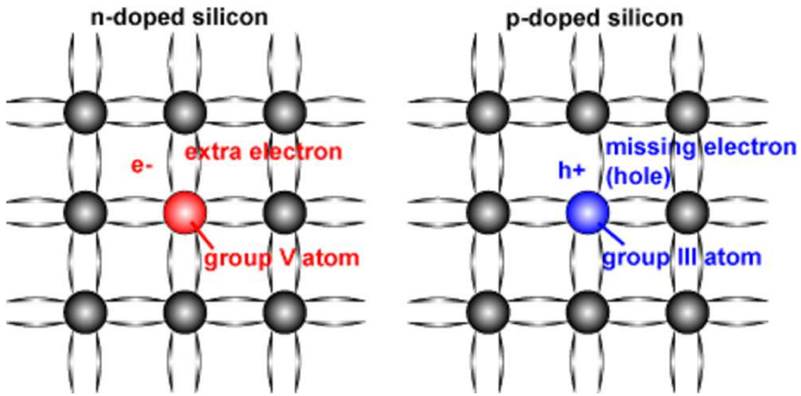
CMOS chips

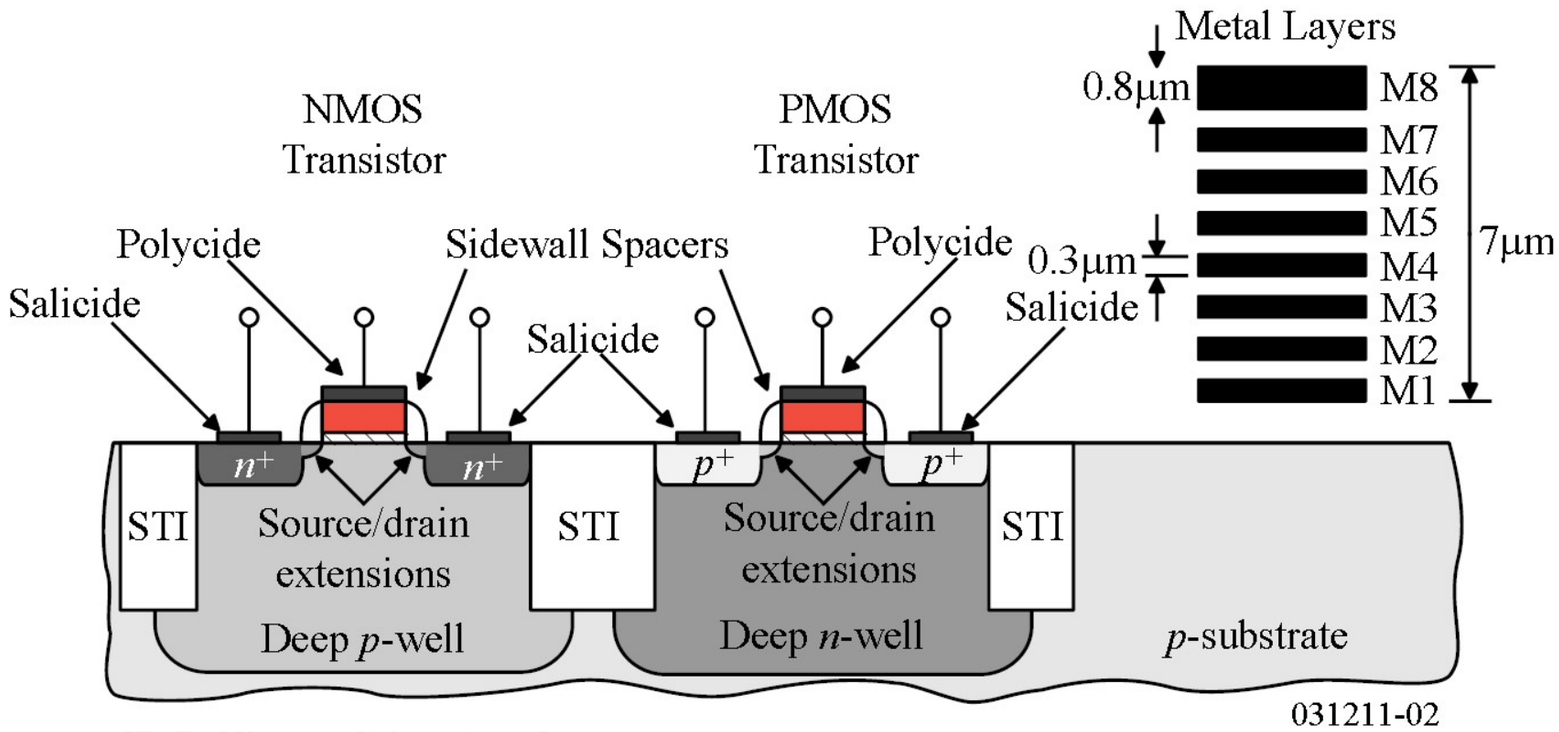


[J. Baker, 2010]

- Mass production
- Multi-project wafer (MPW)
- Production chips are glued, bonded and packaged

CMOS devices cross-section

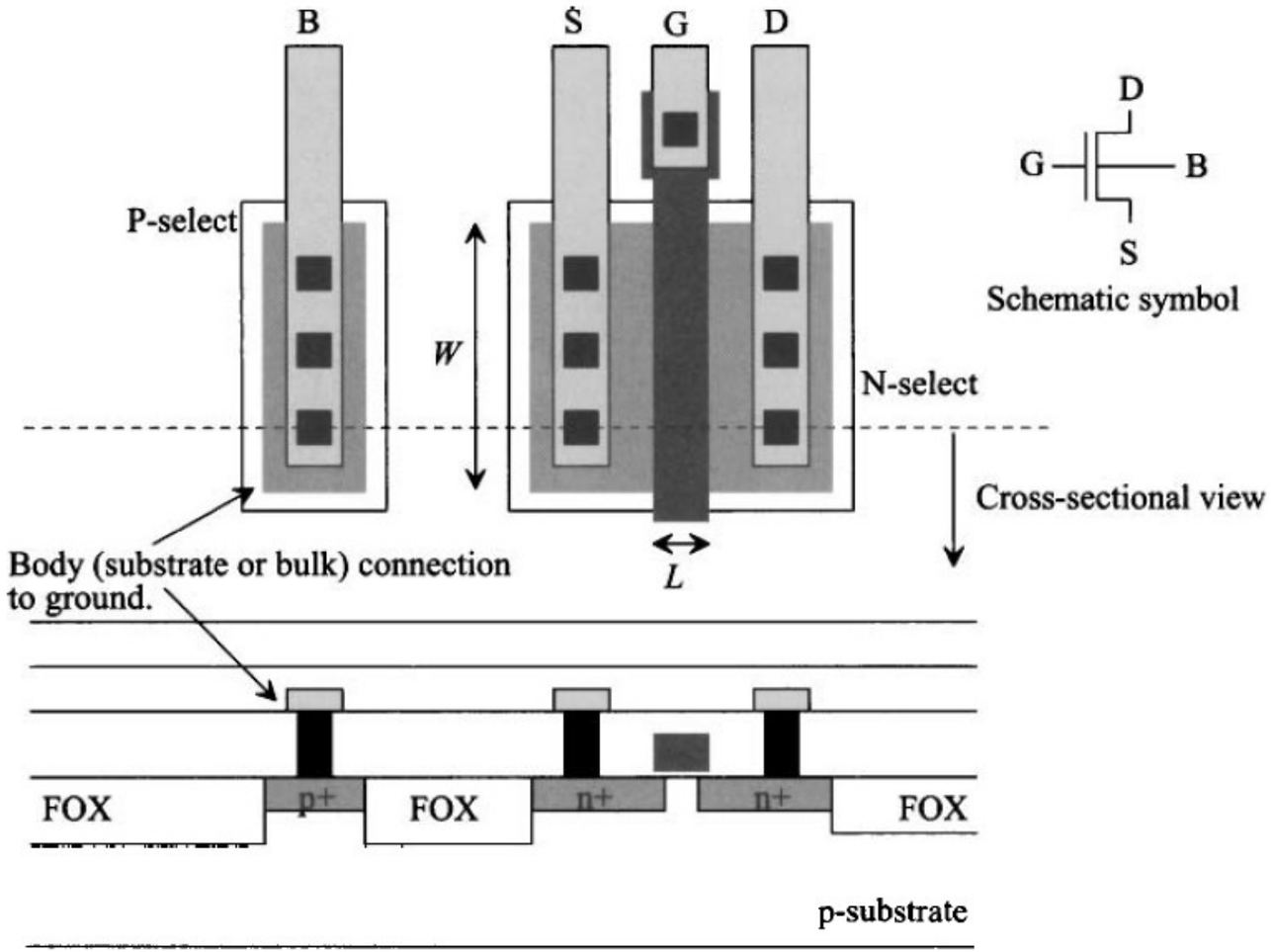




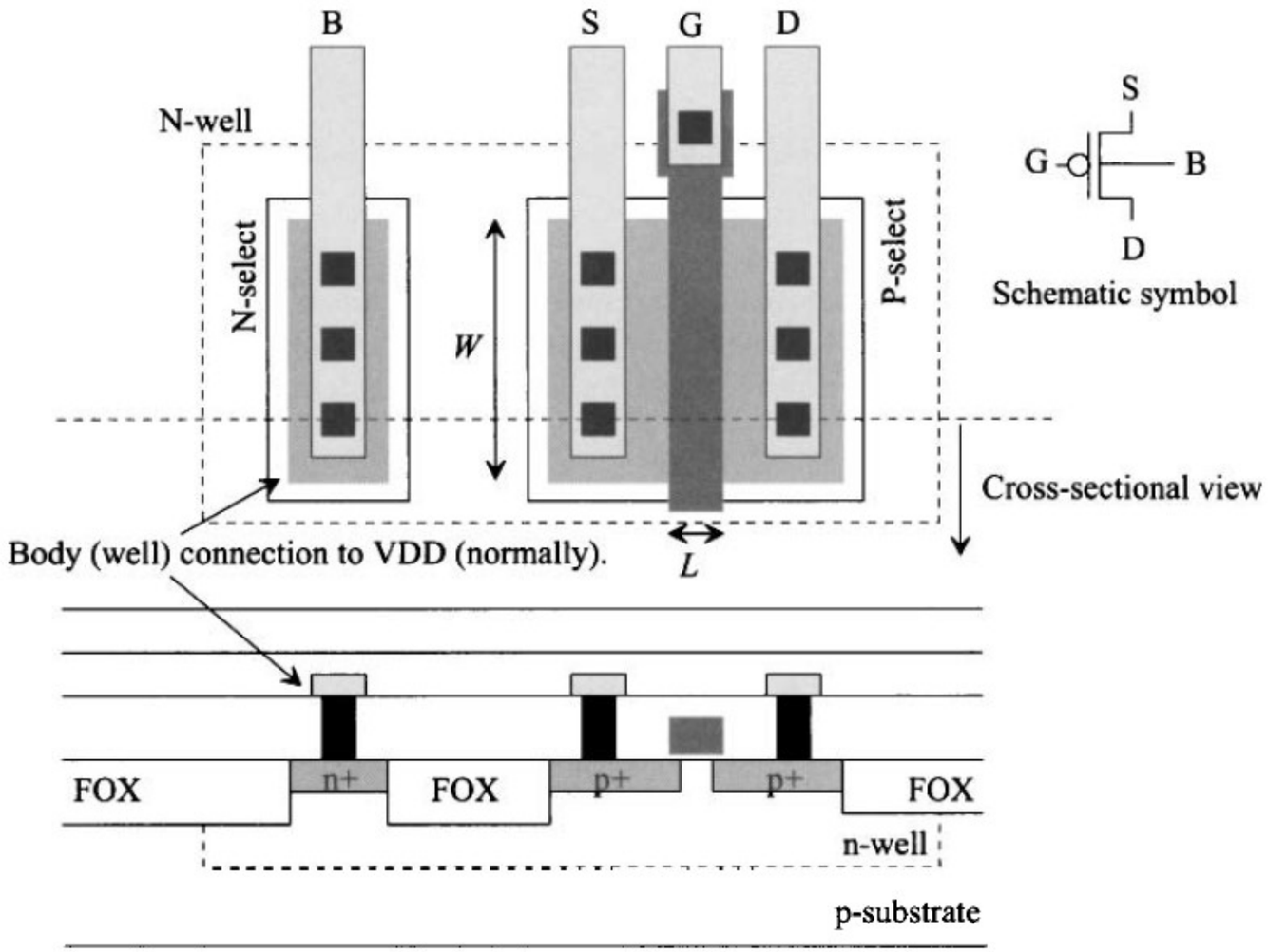
[P. E. Allen's slides, 2016]

- STI → shallow trench isolation, insulator used to isolate devices
- S-D extension (LDD) → reduce short-channel effects (e.g. HCI)
- Salicide/polyside → conductive layer to have small sheet R

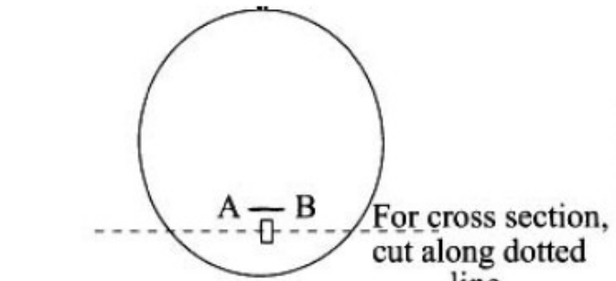
NMOS layout and cross-sectional view



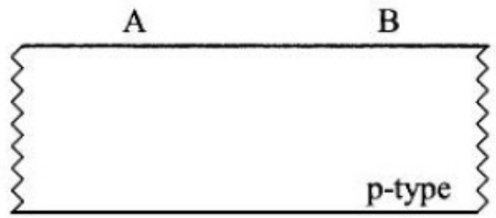
PMOS layout and cross-sectional view



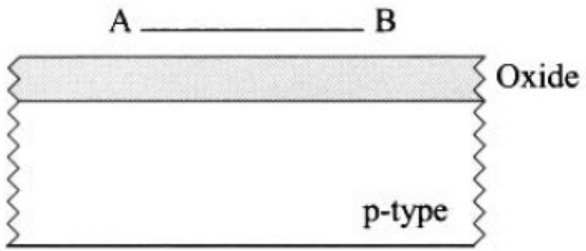
Process steps: Patterning 1



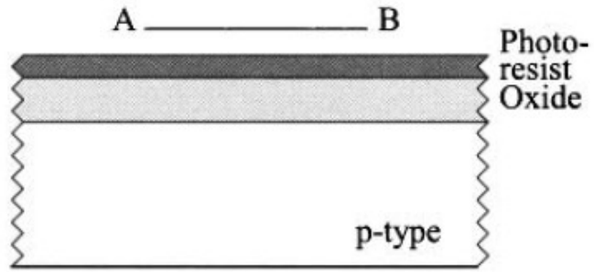
(a) Unprocessed wafer



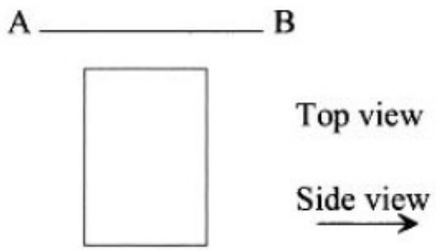
(b) Cross-sectional view of (a)



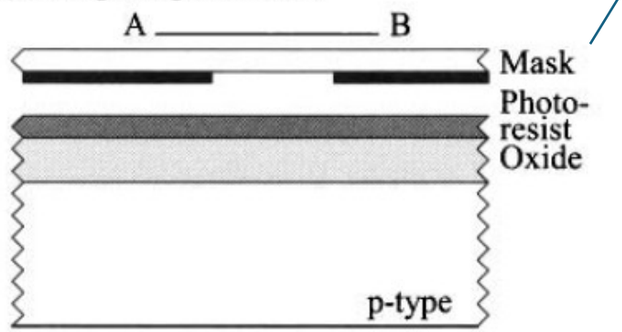
(c) Grow oxide (glass or SiO_2) on wafer.



(d) Deposit photoresist

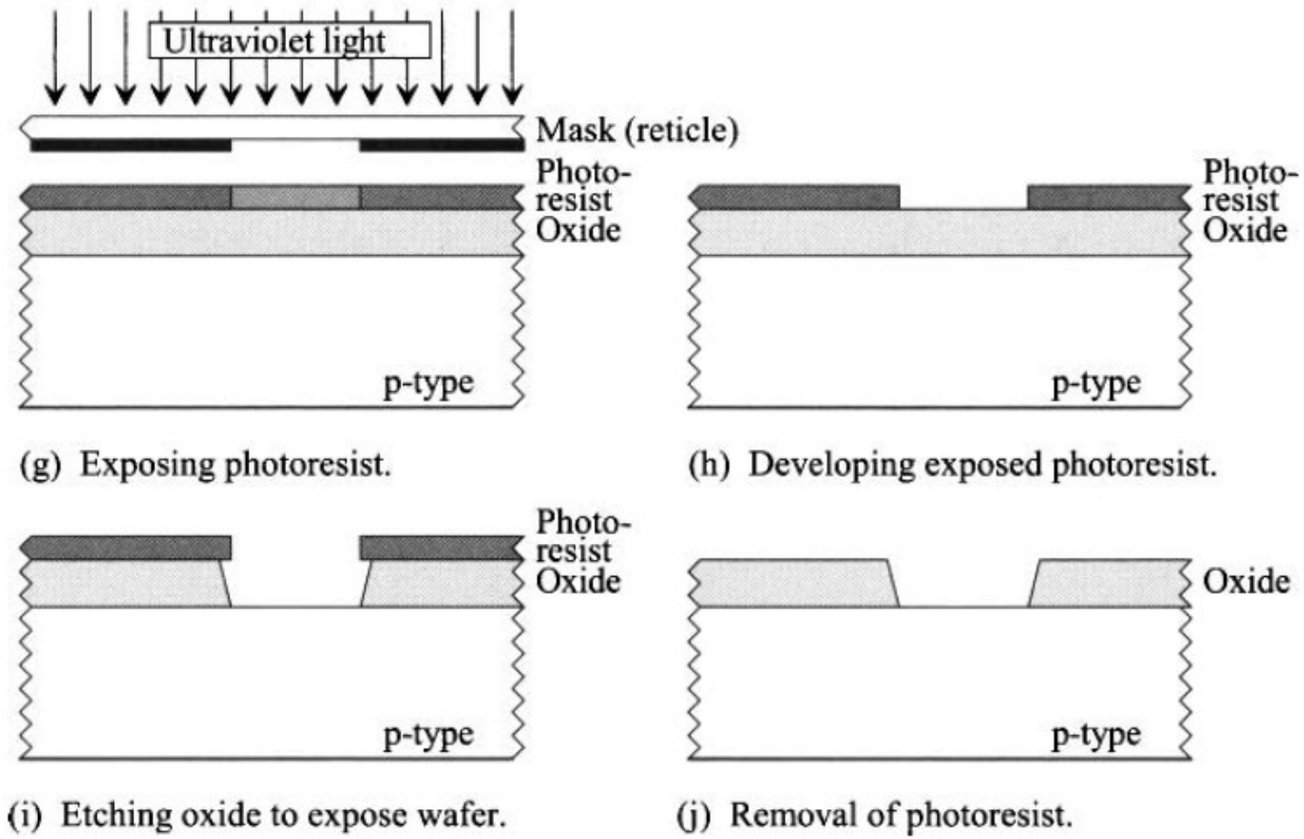


(e) Mask made resulting from layout.



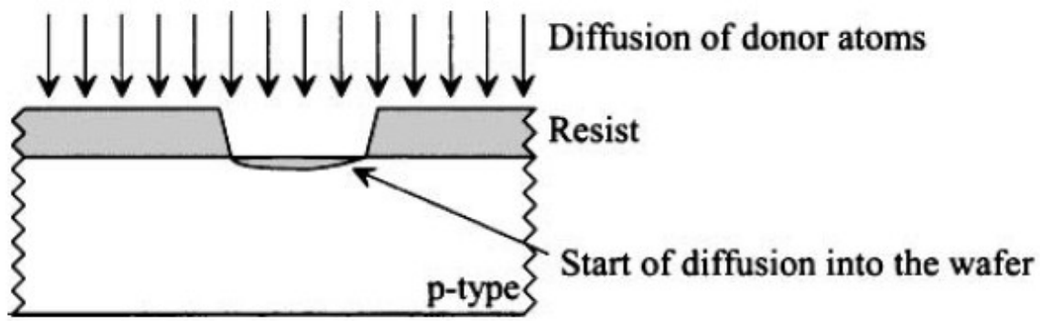
(f) Placement of the mask over the wafer.

Process steps: Patterning 2

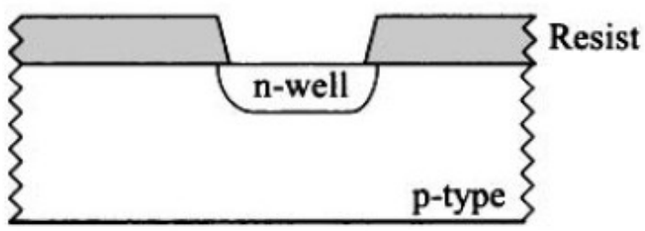


Asianometry – “Etch: Lithography's Unheralded Sibling”
→ https://www.youtube.com/watch?v=po-nlRUQkbI&t=140s

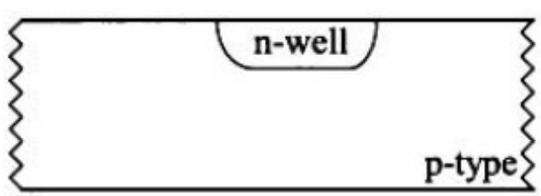
Process steps: Patterning the N-well



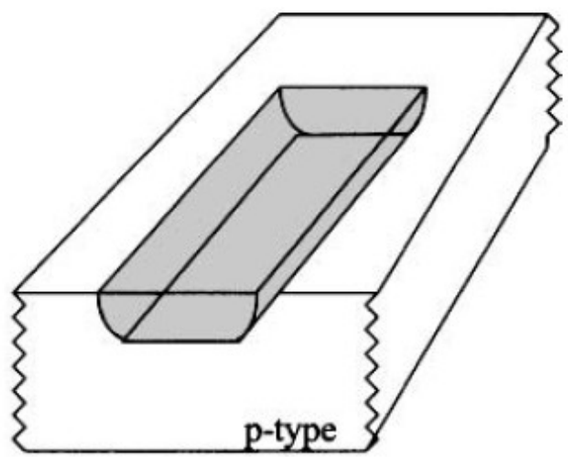
(a) Diffusion of donor atoms



(b) After diffusion

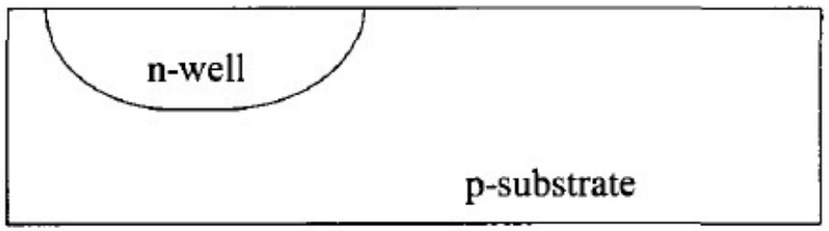


(c) After resist removal

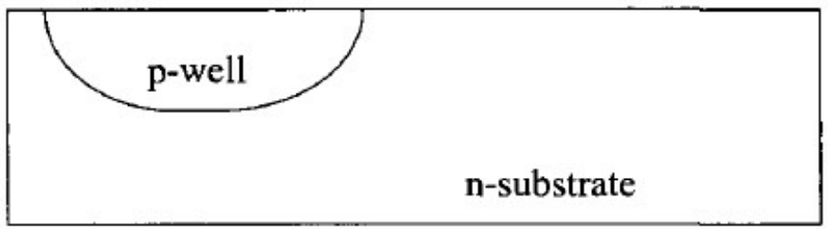


(d) Angled view of n-well

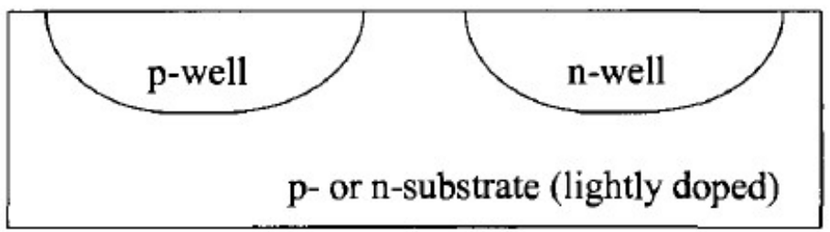
Process types



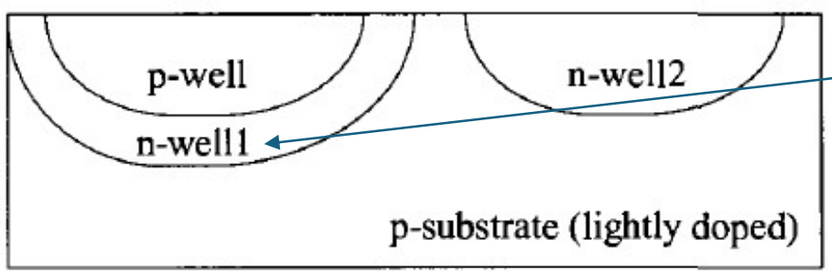
(a) n-well process



(b) p-well process



(c) Twin-well process

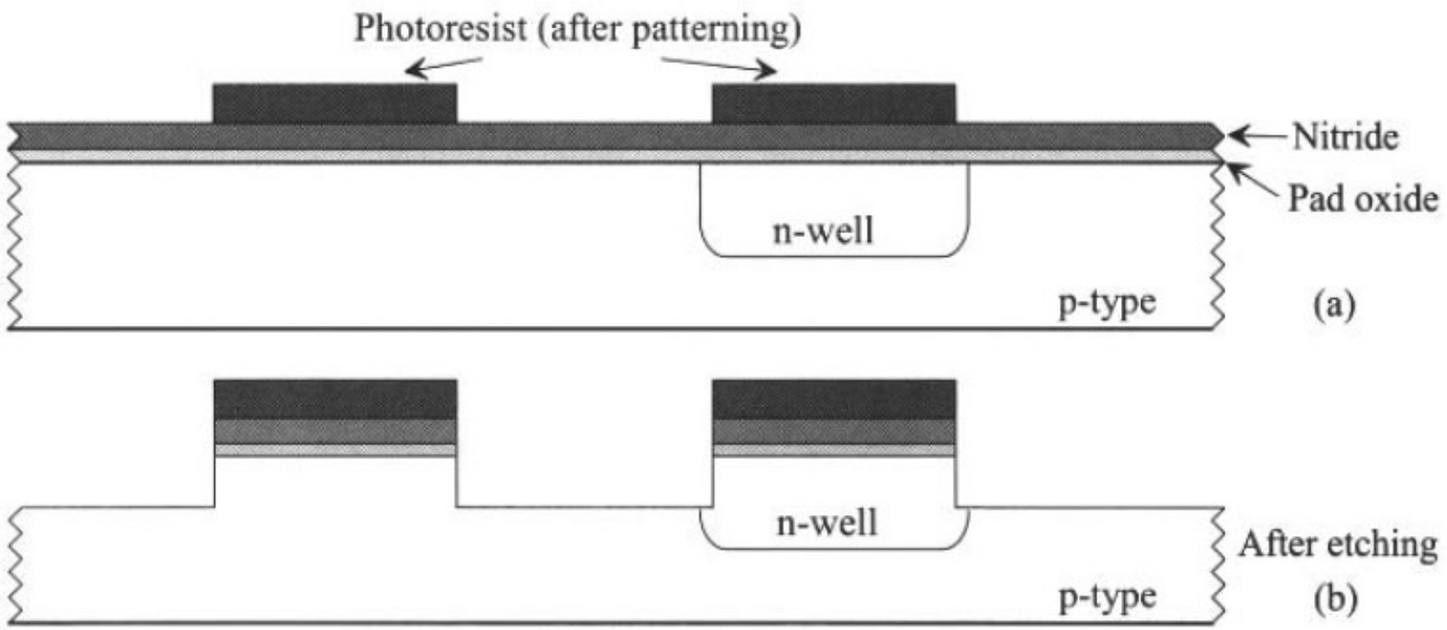


(d) Triple-well process using p-substrate

- P-substrates and N-substrates are possible
- Counter doping generates slower devices
- Triple well allow to isolate NMOS bulk terminal among devices

Deep-NWELL

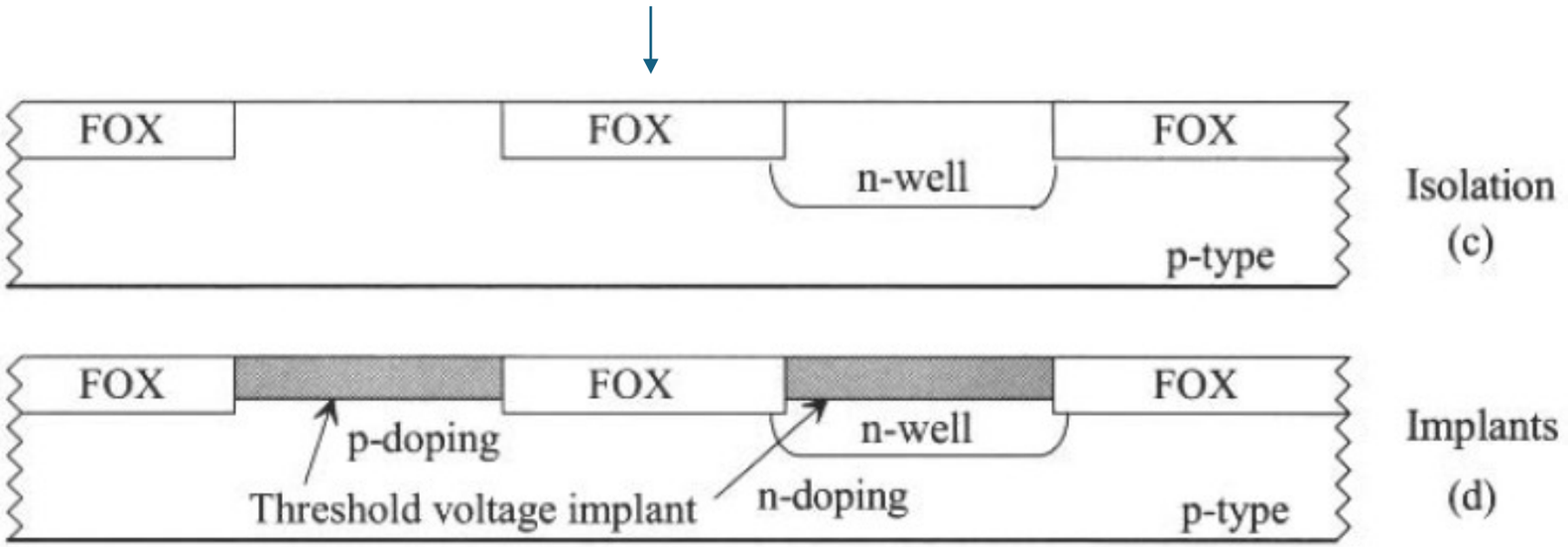
General CMOS process flow 1



- (a) Thin oxide + nitride + patterned photoresistor
- (b) Etching for shallow trench generation

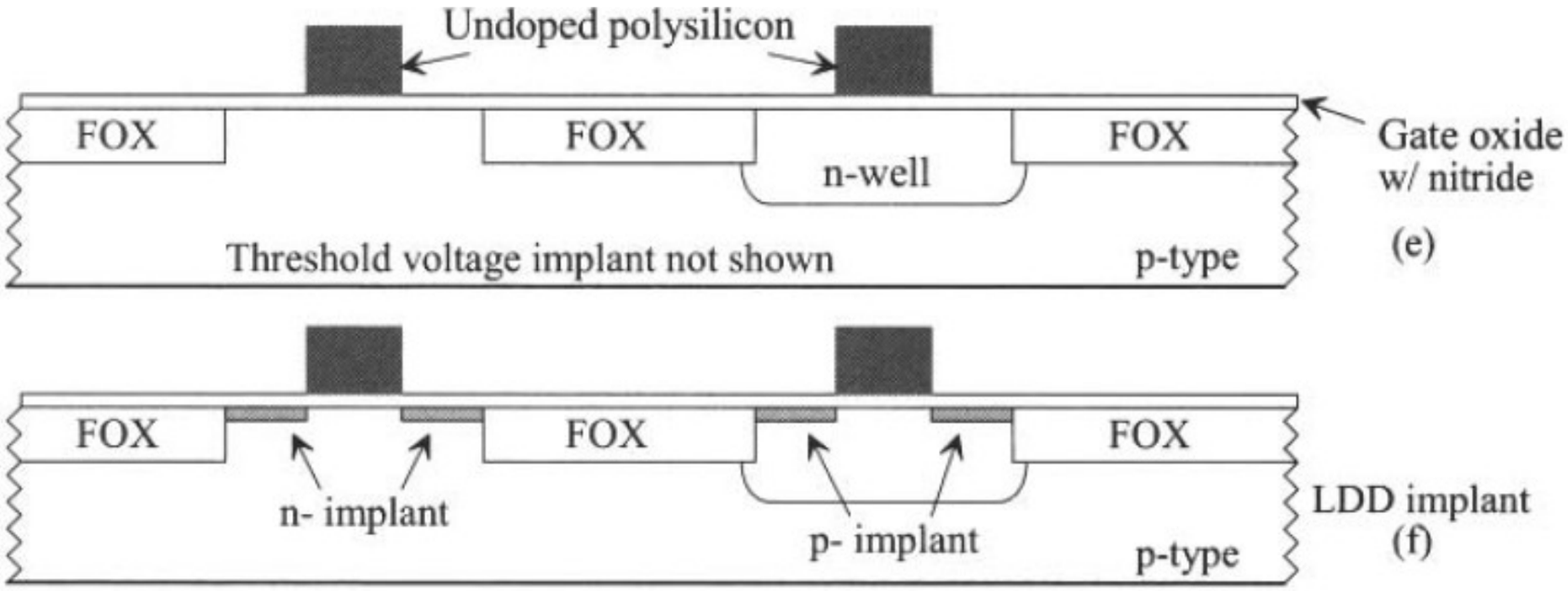
General CMOS process flow 2

Shallow-trench isolation (STI) with SiO_2



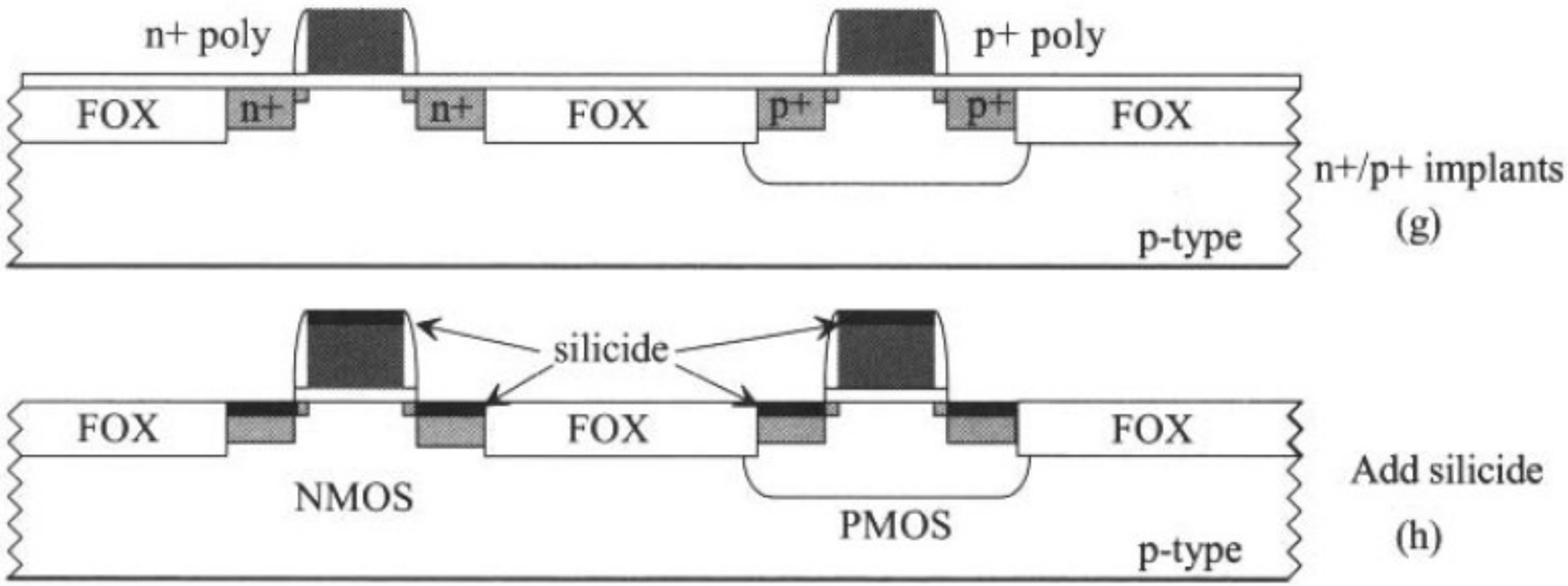
- (c) Shallow trench filled with SiO_2 → active area isolation
- (d) Doping through masks to set Vth

General CMOS process flow 3



- (e) Deposition and patterning of polysilicon - polycrystalline silicon - for the MOSFET gate
- (f) Lightly doped drain implant → prevent high electric field

General CMOS process flow 4

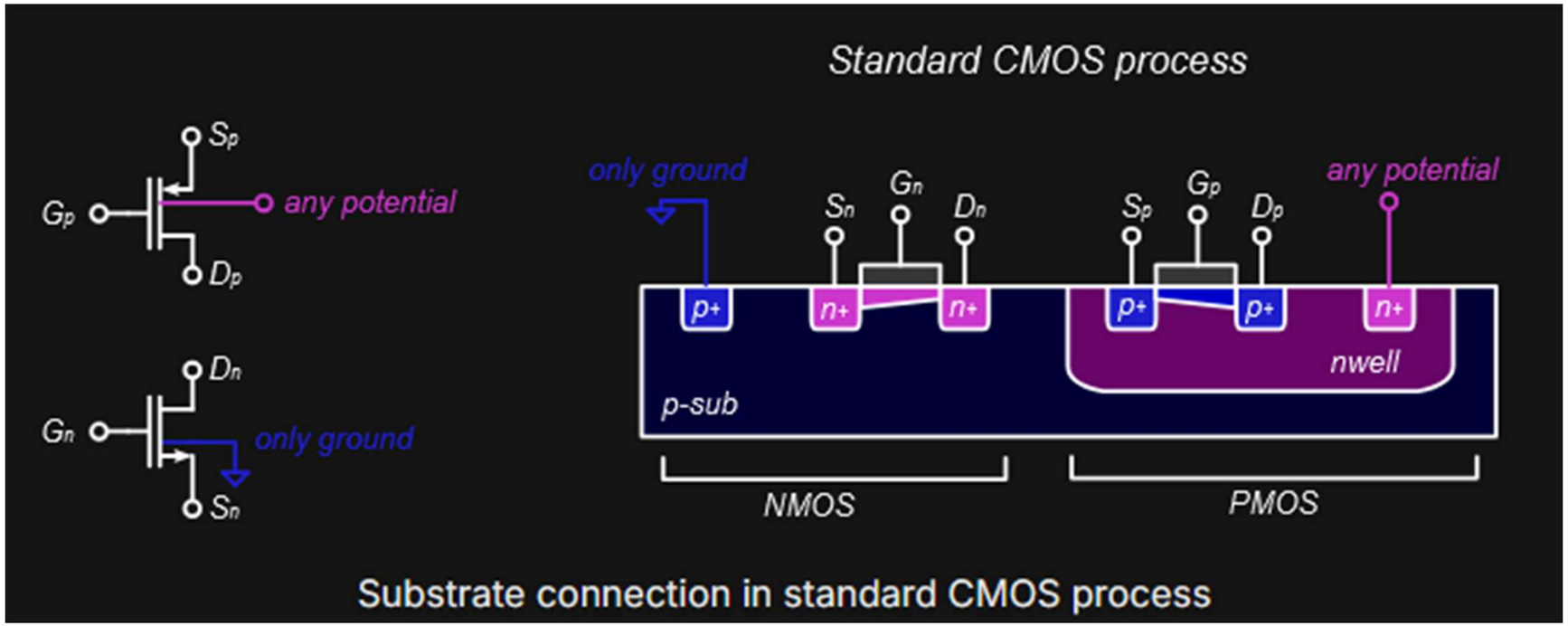


- (g) n+/p+ doping (including polysilicon)
- (h) Silicide to reduce sheet resistance of n+/p+ regions and polysilicon

Bulk connection in standard CMOS process

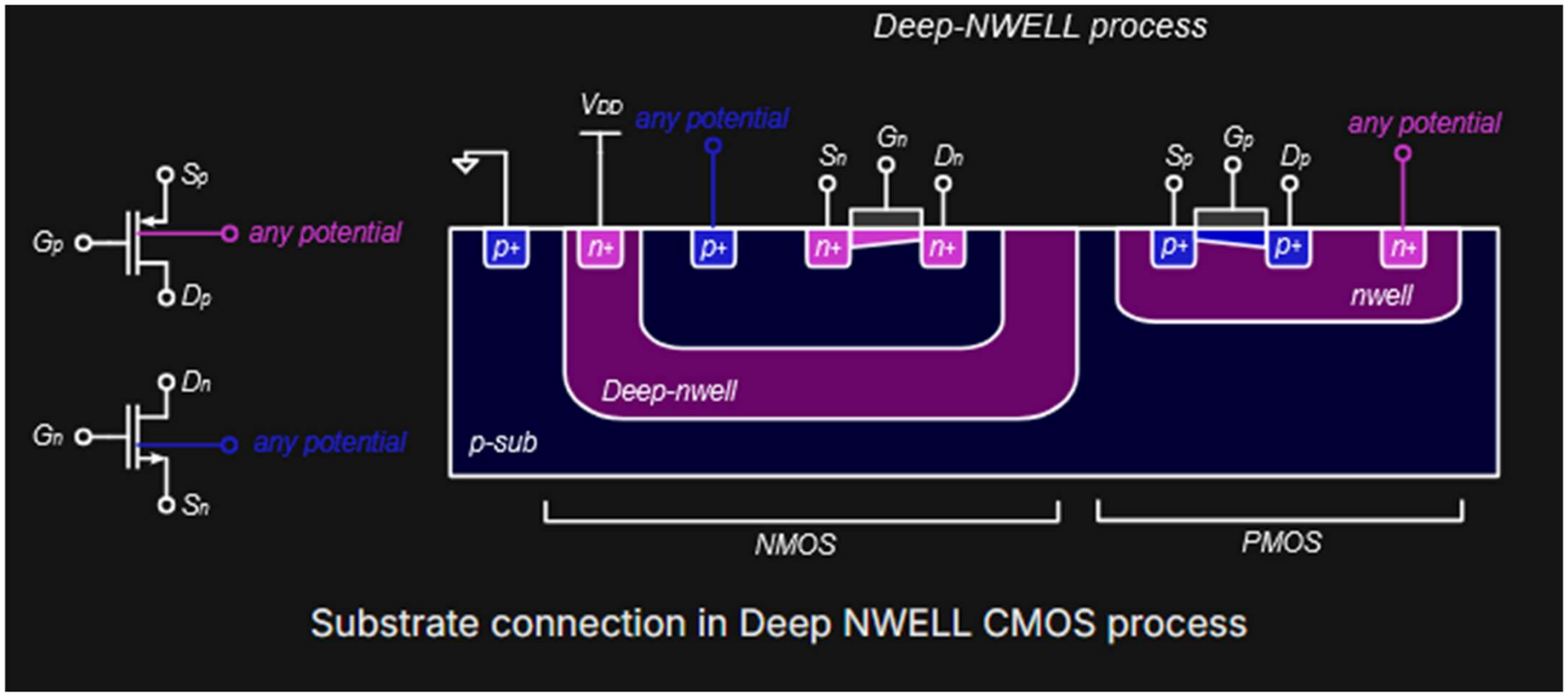
Standard process summary:

- *PMOS body can be connected to any potential;*
- *NMOS body can be connected only to ground (shorted to the substrate);*



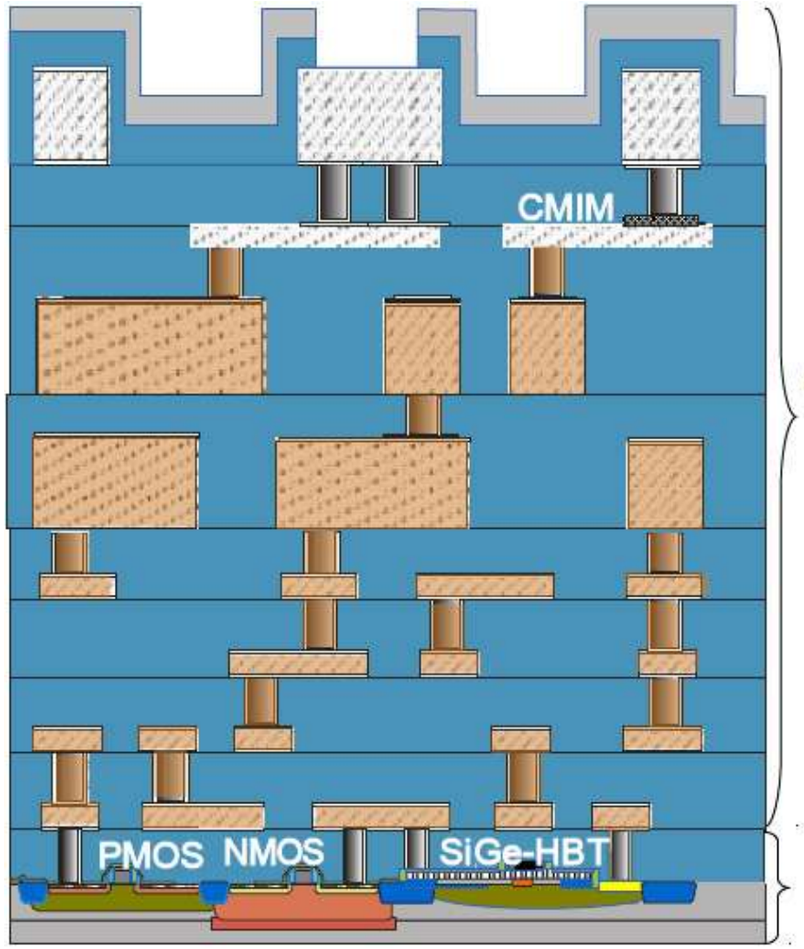
https://analoghub.ie/category/Layout/article/layoutBasics

Bulk connection in triple-well CMOS process



https://analoghub.ie/category/Layout/article/layoutBasics

IHP 130nm BiCMOS technology stack



Cu BEOL
X-FAB

FEOL
IHP

PDK
Customer Interface
TAPE OUT

SG13 FEOL

Cu BEOL
(Start M1)

PCM Test
Shipment to
customer

Action
IHP

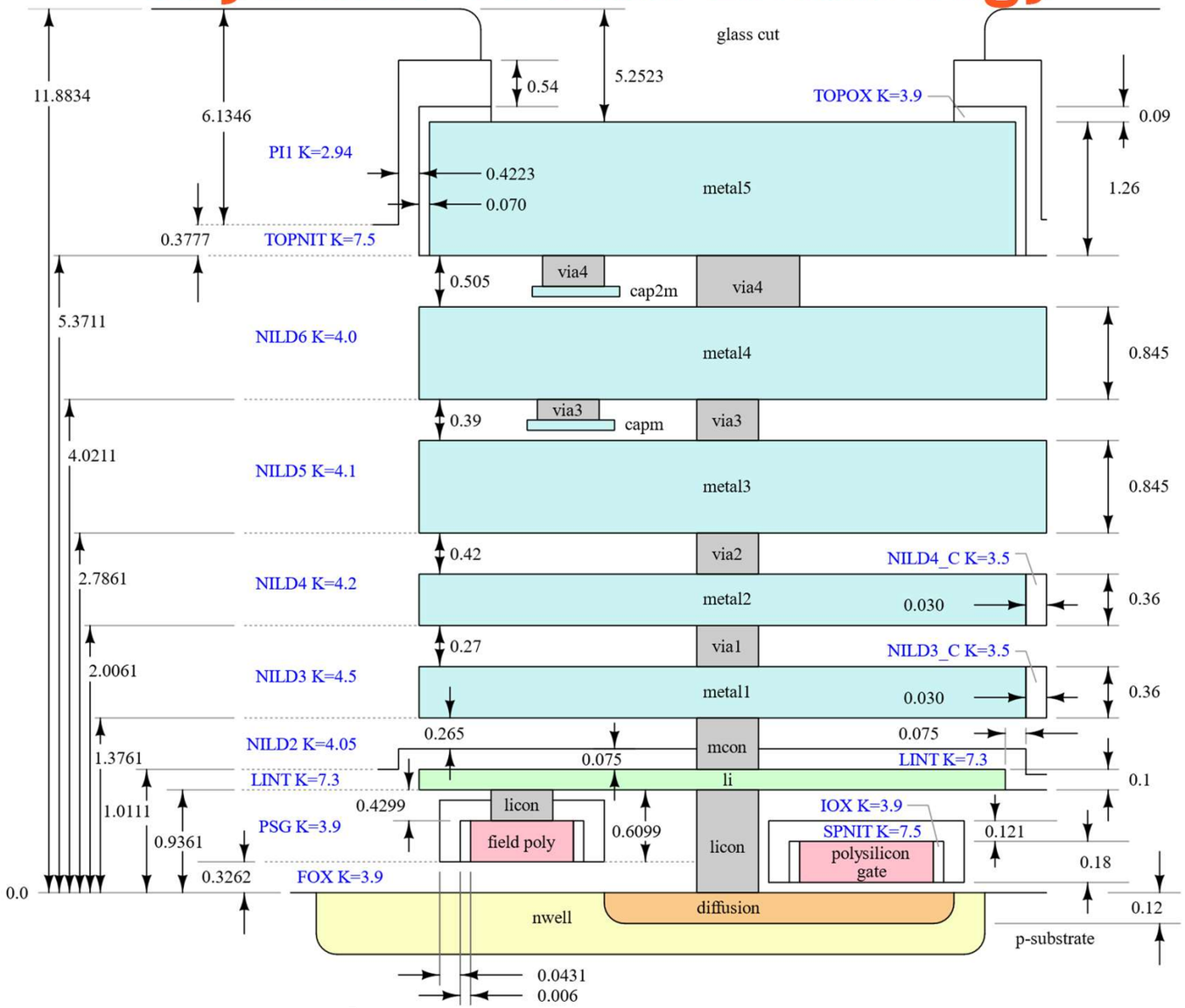
Action
XFab

https://www.ihp-microelectronics.com/services/research-and-prototyping-service/mpw-prototyping-service/sigec-bicmos-technologies
https://github.com/IHP-GmbH/IHP-Open-PDK

IHP 130nm BiCMOS technology features

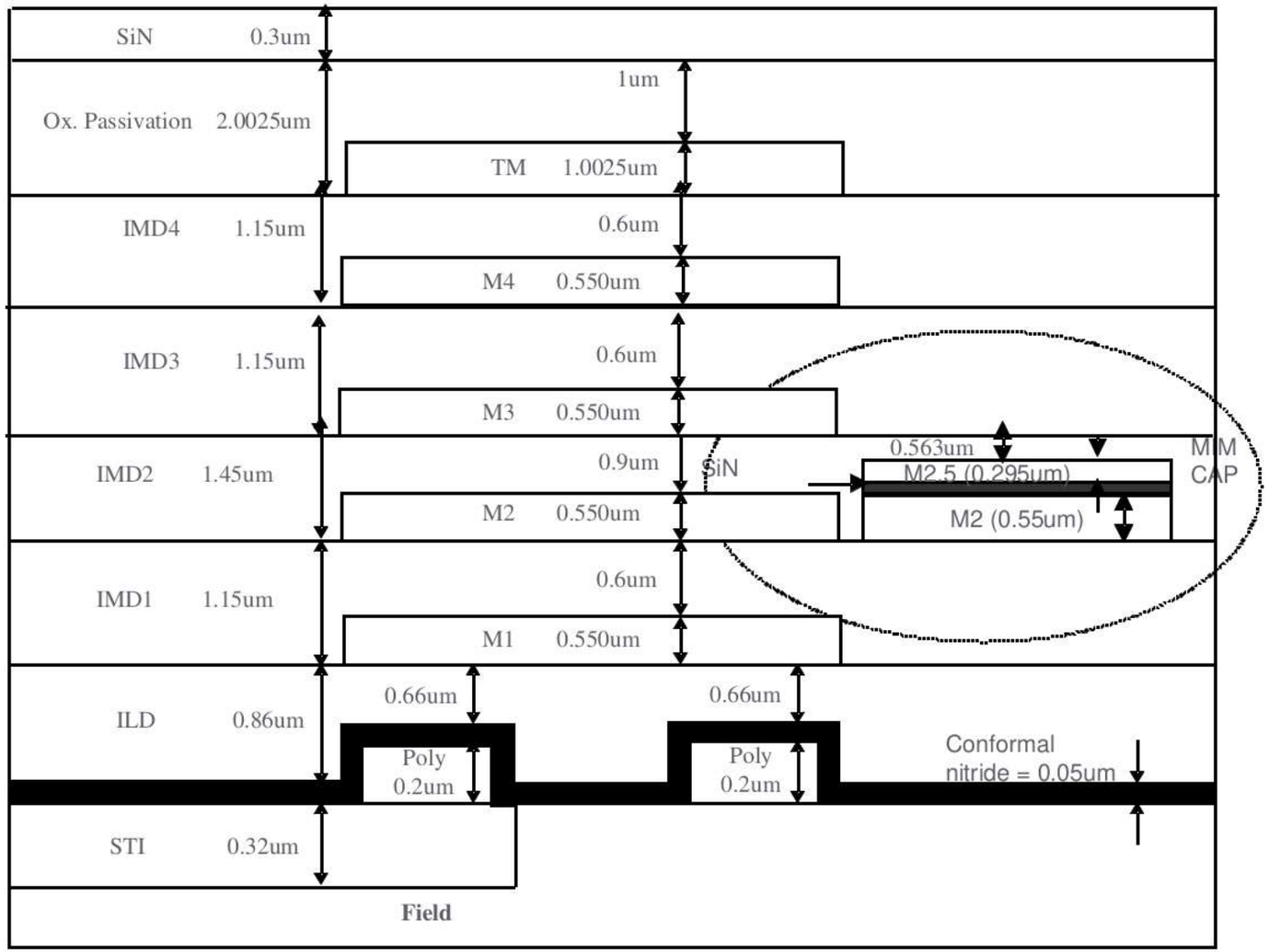
- SG13G2 is a high performance BiCMOS technology with a 0.13 µm CMOS process
- 2 gate oxides: A thin gate oxide for the 1.2 V digital logic and a thick oxide for a 3.3 V supply voltage
- PMOS and isolated NMOS transistors are offered
- Passive components like poly silicon resistors and MIM capacitors are available
- 5 thin metal layers, two thick metal layers (2 and 3 µm thick) and a MIM layer

Skywater 130nm technology



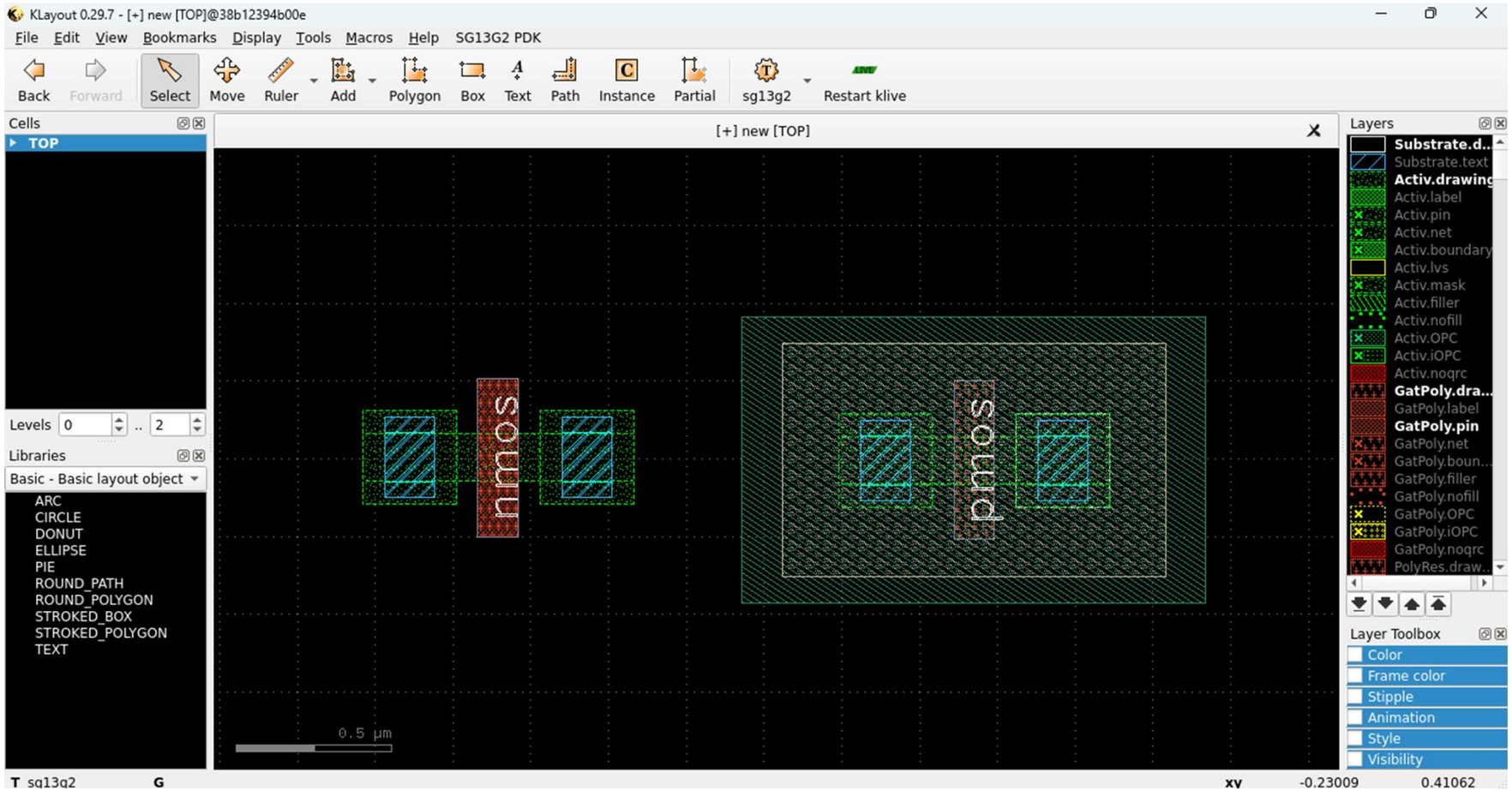
SKY130 → https://skywater-pdk.readthedocs.io/

Global Foundries 180nm technology



GF180MCU → https://gf180mcu-pdk.readthedocs.io/en/latest/

DEMO: IHP NMOS and PMOS in KLayout



Layout rules → https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs.doc/doc/SG13G2_os_layout_rules.pdf

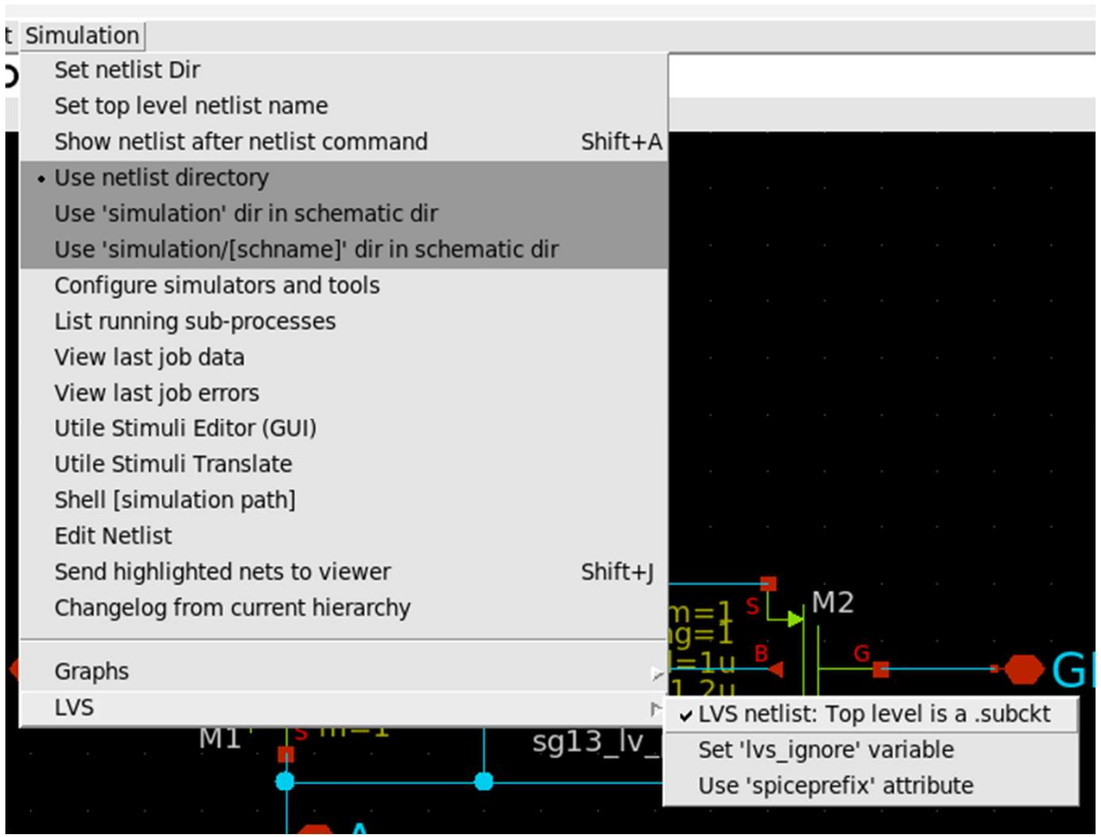
Transmission gate layout

Layout in IHP + KLayout

- Enable editing: sudo chown -R designer /opt/pdks/ihp-sg13g2/
- TOP
  - Rename cell
  - Show as new top
- Klayout → Tools → DRC
  - IHP PDK documentation
    - https://github.com/IHP-GmbH/IHP-Open-PDK/tree/main/ihp-sg13g2/libs.doc/doc
    - Design rules: https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs.doc/doc/SG13G2_os_layout_rules.pdf
- LVS
  - Netlist SCH
  - SG13G2 PDK → SG13G2 LVS options
  - SG13G2 PDK → Run Klayout LVS
- Example video (for GF180, from 9.51 on it's different for DRC/LVS): https://www.youtube.com/watch?v=vamfMryYPS4

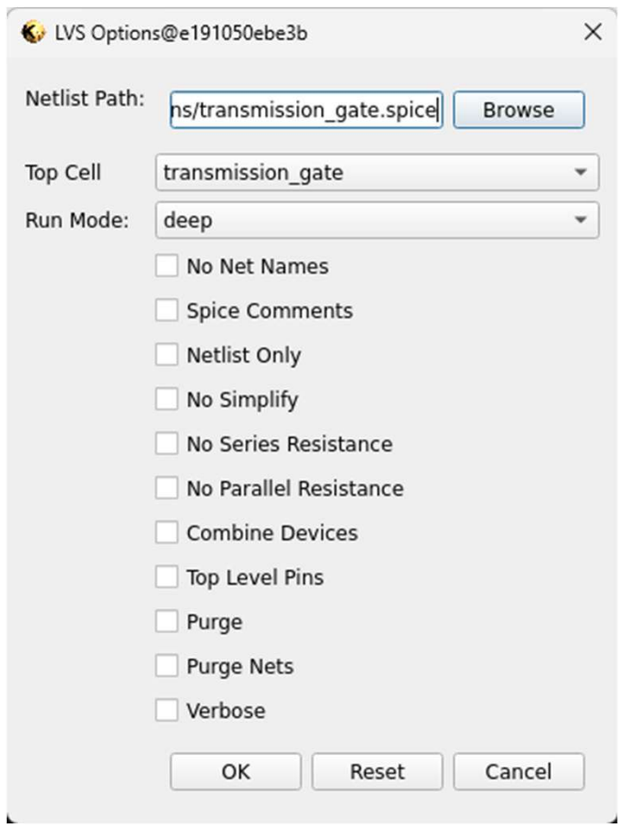
Layout in IHP + KLayout

- Settings for schematic netlist generation in Xschem



Layout in IHP + KLayout

- Settings for schematic netlist loading in Klayout



Task: tgate + inverter layout

Task

- Create the transmission gate layout for your design, including the inverter
  - Option 1: custom layout
  - Option 2: add stdcell layout
- [extra] Design a 4-bit analog MUX layout

Thank you!
Questions?