Open-Source IC Design Workshop

2.1 Simple schematic-level design: transmisión gate

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Agenda

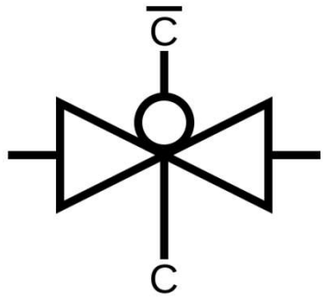
- Introduction
- MOSFET basics
- Transmission gate simulation
- Task: Tgate + inverter

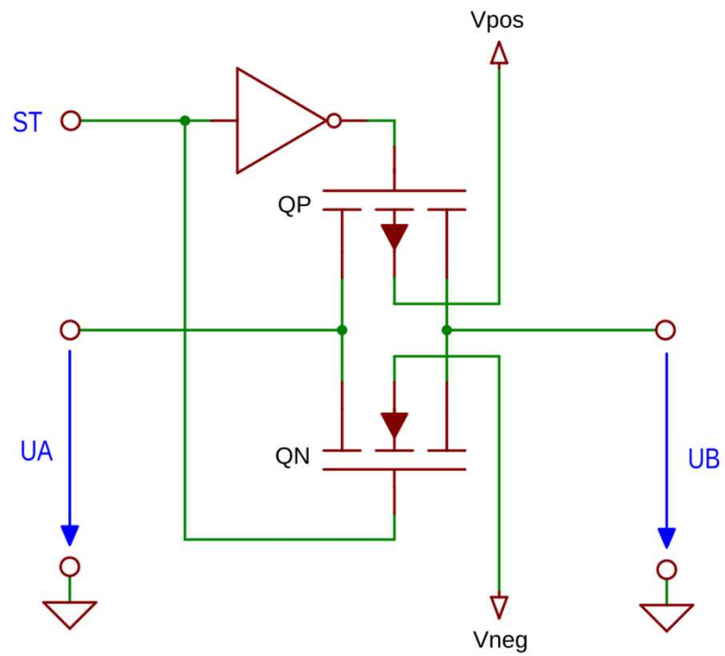
Introduction

Introduction

Transmission gates

- Complementary CMOS switch, used in analog application for its symmetry
- QN and QP in parallel, controlled with complementary signals
- Why symmetry?
  - NMOS passes a good 0 but a poor 1
  - PMOS passes a good 1 but a poor 0
- Operation
  - C high → both transistors are ON
  - C low → both transistors are OFF

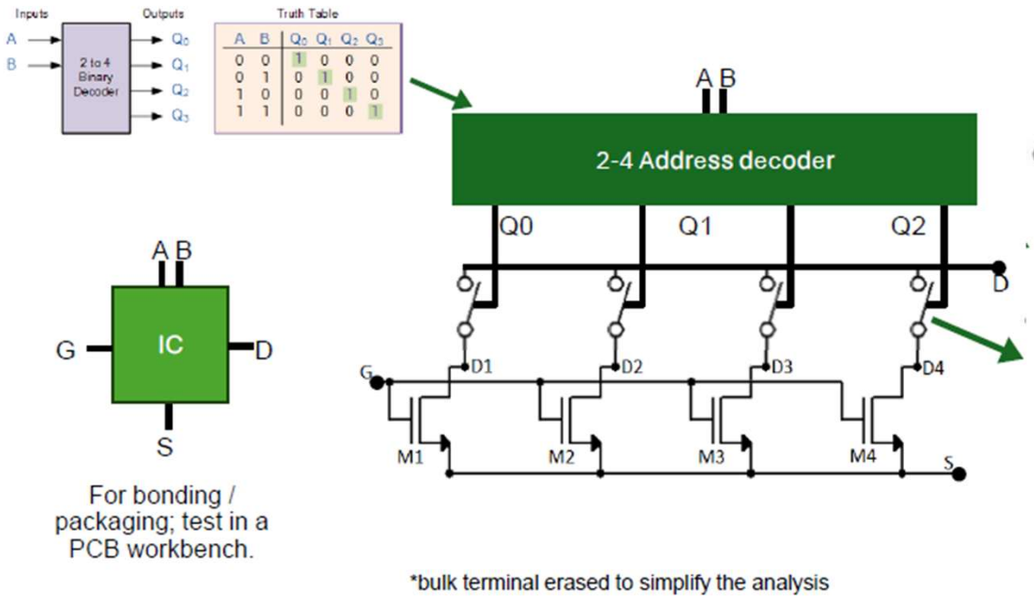


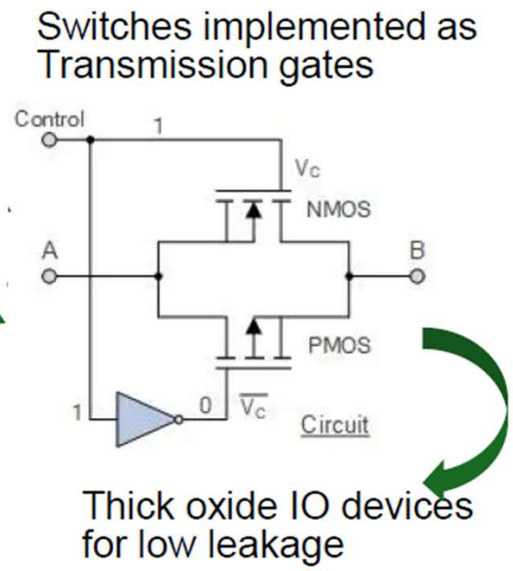


Introduction

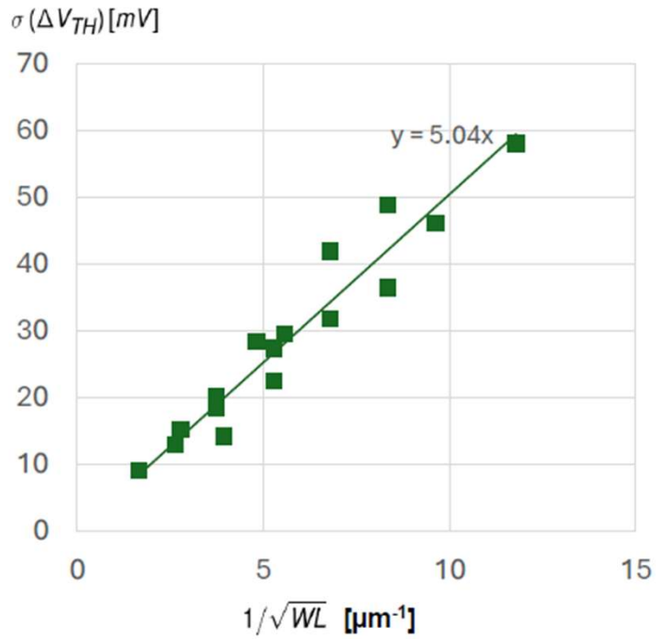
Motivation: integrated analog muxes for device characterization

- Characterization chips need access to many analog test points with a limited amount of input/output pins





Pelgrom plot

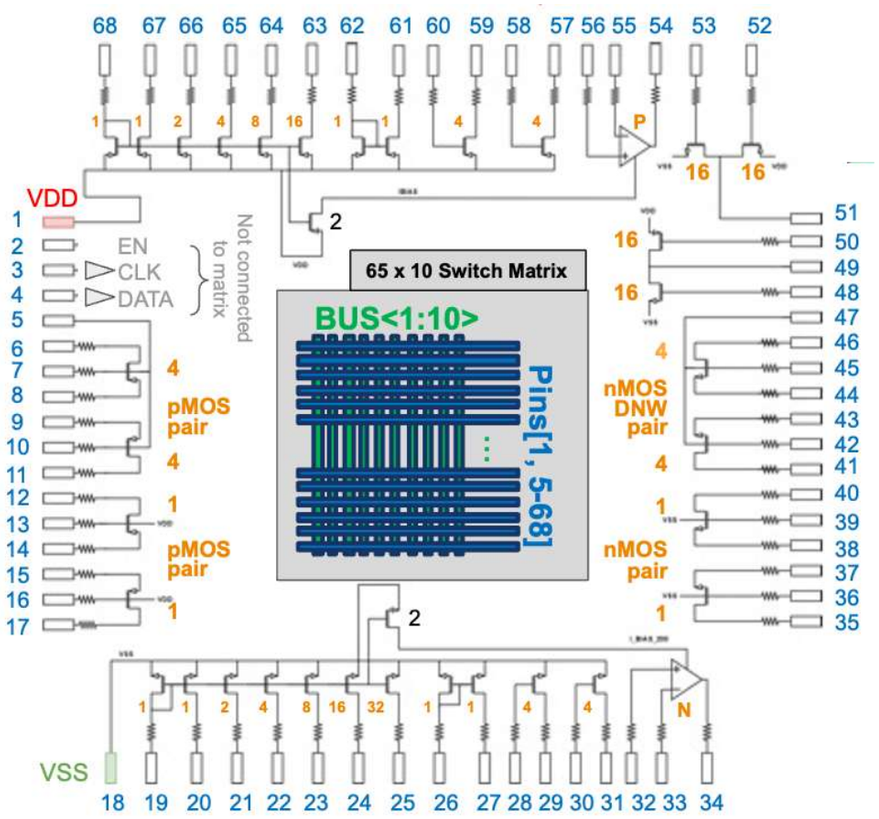


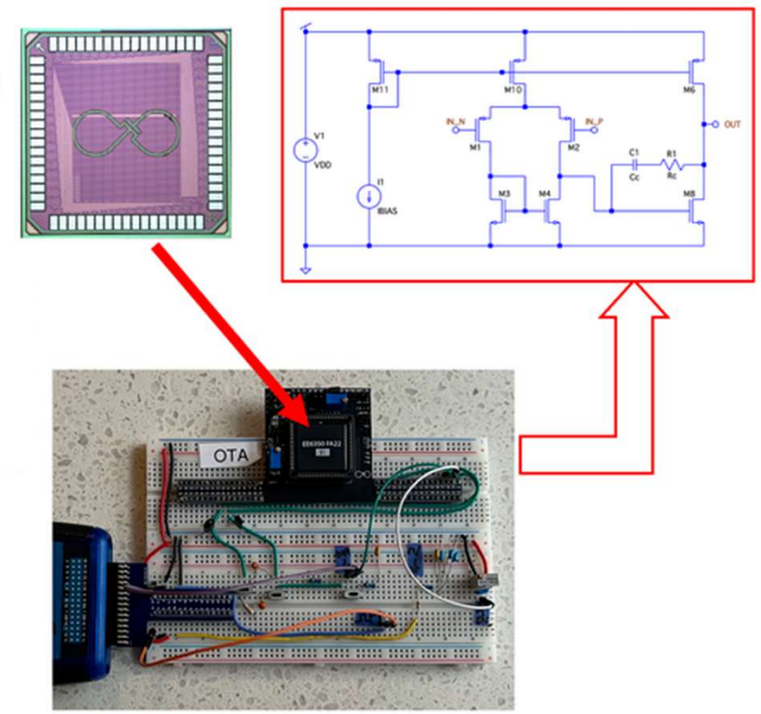
[J. P. Martinez Brito (CEITEC) – “Device Array Testing – without Probe Station”]

Transmission gate simulation

Motivation: MOSBius chip

- Educational chips can benefit from the idea of connecting building blocks for testing

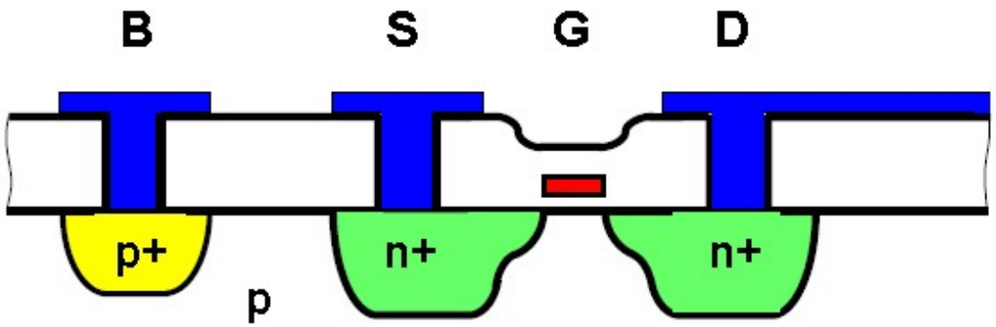


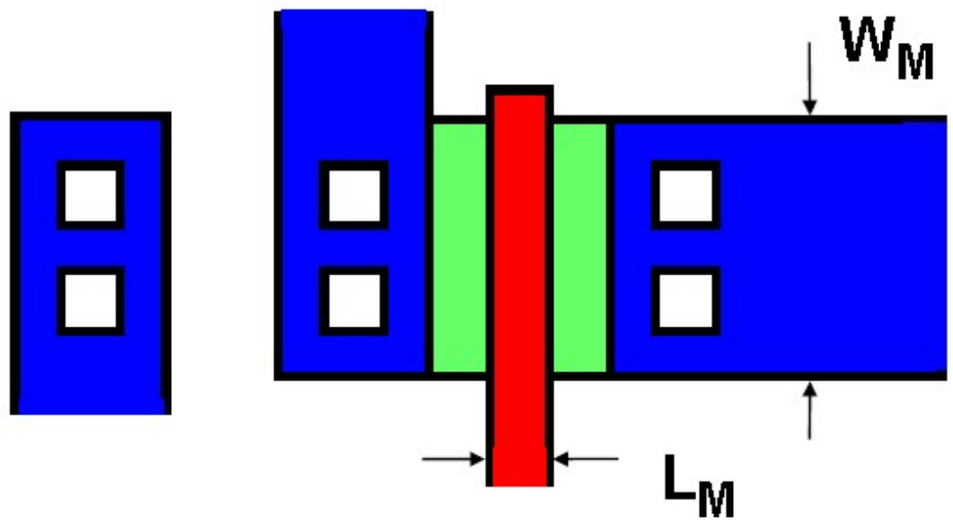


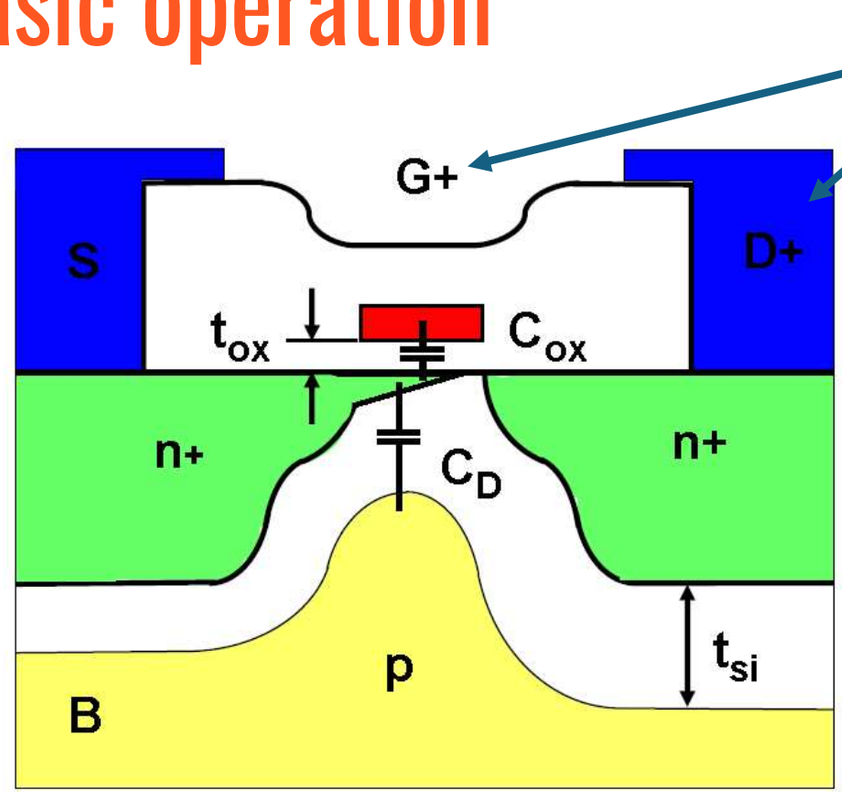
[Peter Kinget - https://mosbius.org]

MOSFET basics

MOSFET basic operation







$$C_D = \frac{\varepsilon_{si}}{t_{si}}$$

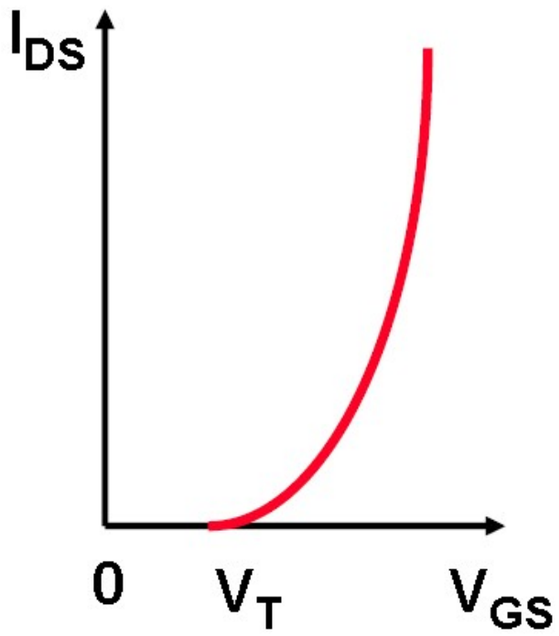
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$\frac{C_D}{C_{ox}} = n - 1$$

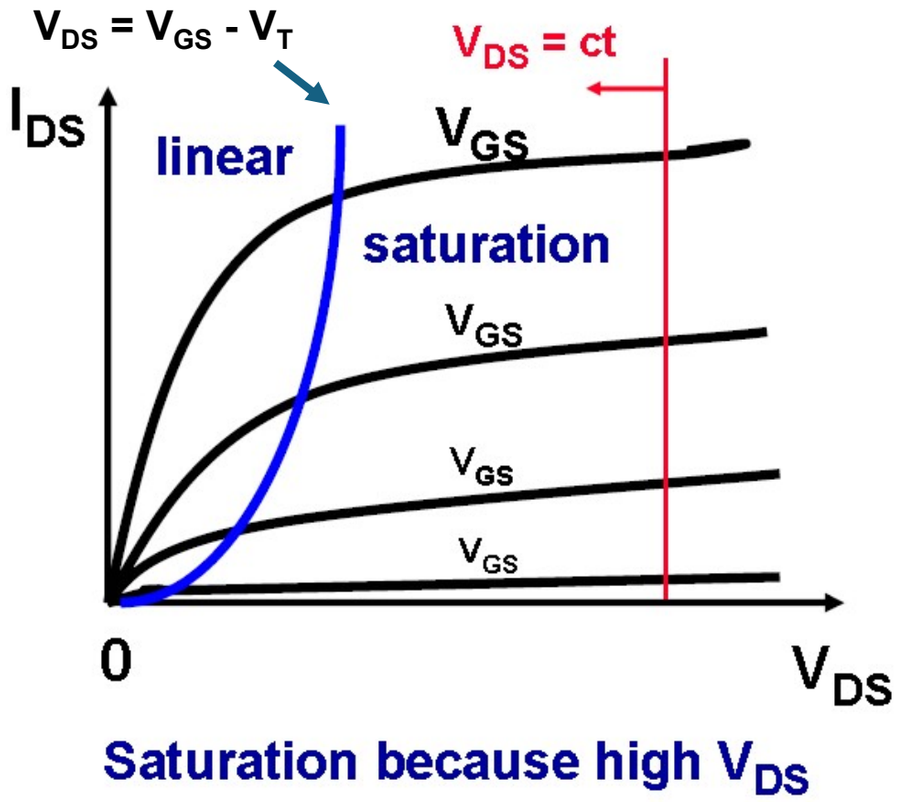
- Gate → MOS channel control
- Bulk → JFET channel control (body effect, parasitic)

[Sansen, 2006]

MOSFET characteristic curves



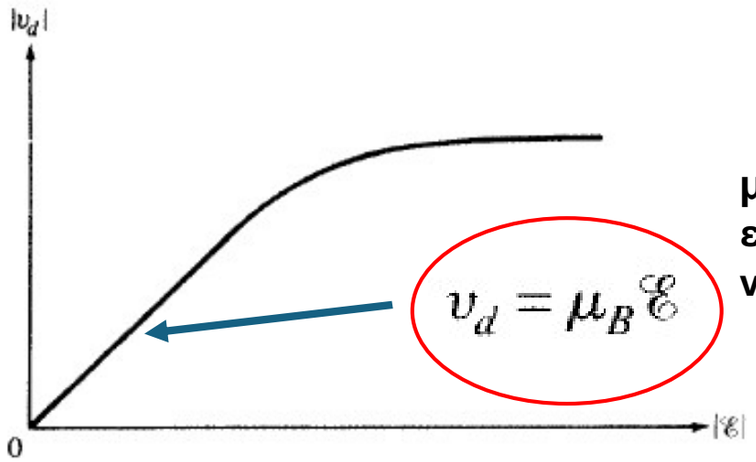
[Sansen, 2006]



- Positive V_{GS} → inversion layer/channel below the gate
- Positive V_{DS} → I_{DS} current flowing from drain to source
- $V_{GS} – V_T$ is the most relevant design parameter

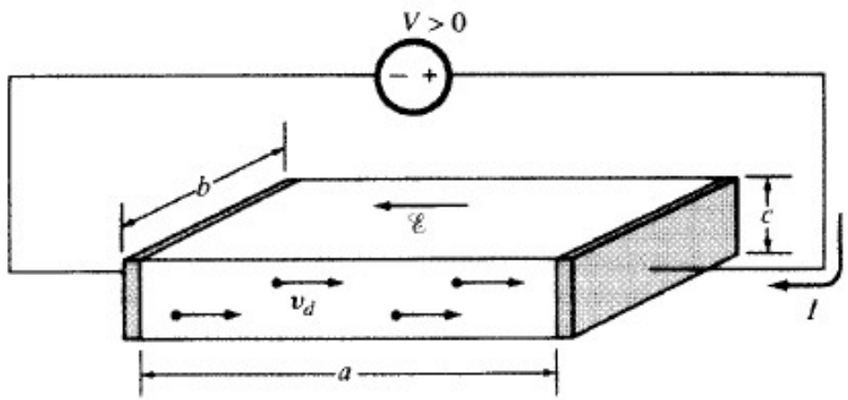
Drift vs diffusion current

[Tsividis, 2010]



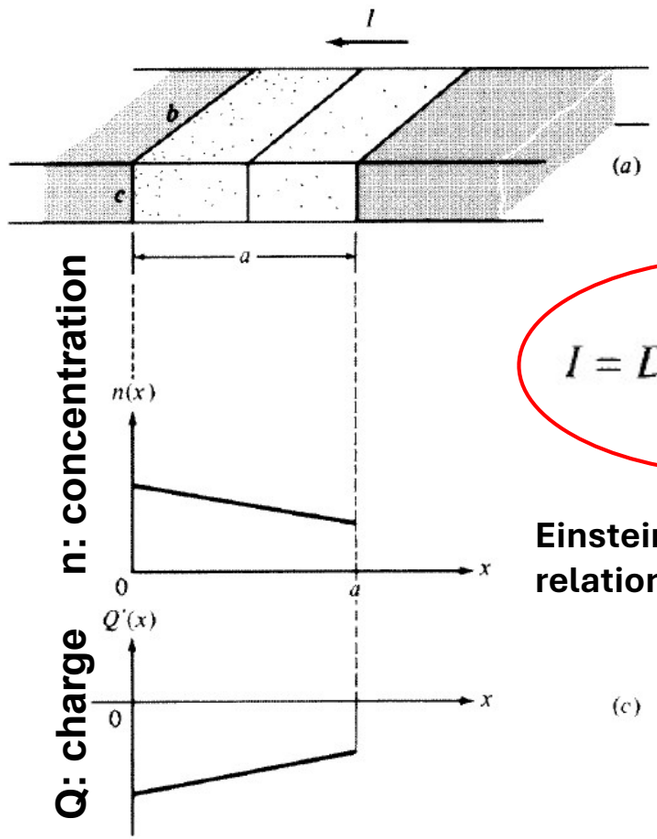
μ_B: mobility
ε: electric field
v_d: drift velocity

FIGURE 1.11
Magnitude of drift velocity versus magnitude of electric field.



$$I = \frac{nq(abc)}{\tau} = nq(bc)v_d$$

FIGURE 1.12
An *n*-type semiconductor bar with uniform electron concentration under external bias.



D: diffusion constant
Φ_t: thermal voltage (kT/q)

$$I = Dq(bc)\left(-\frac{dn}{dx}\right)$$

Einstein relationship → $D = \mu_B \phi_t$

FIGURE 1.15
(*a*) A semiconductor bar with nonuniform electron concentration along its length; (*b*) the electron concentration in (*a*) for a special case of interest; (*c*) charge per unit area corresponding to (*b*).

Drift current model

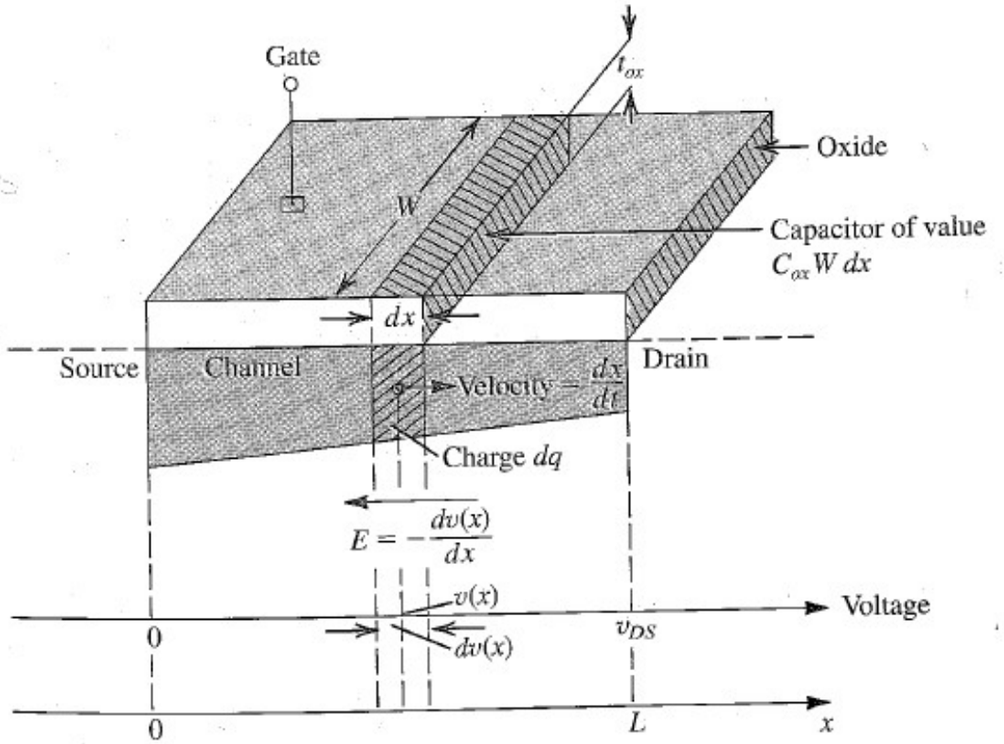
Diffusion current model

Drift vs diffussion current

- Drift current → due to electric field over a piece of semiconductor
  → dominant in MOSFET
  → polynomial
- Diffusion current → due to particle concentration gradient
  → dominant in BJT
  → exponential

MOSFET "square-law" (SL) equation: linear region

[Sedra, 2004]



$$i = \frac{dq}{dt} = \frac{dq}{dx}\frac{dx}{dt}$$

① ②

① $$dq = -C_{ox}(W\,dx)[v_{GS} - v(x) - V_t]$$

② $$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dv(x)}{dx}$$

$$E(x) = -\frac{dv(x)}{dx}$$

$$\rightarrow \quad i = -\mu_n C_{ox} W[v_{GS} - v(x) - V_t]\frac{dv(x)}{dx}$$

$$\rightarrow \quad i_D = -i = \mu_n C_{ox} W[v_{GS} - v(x) - V_t]\frac{dv(x)}{dx}$$

which can be rearranged in the form

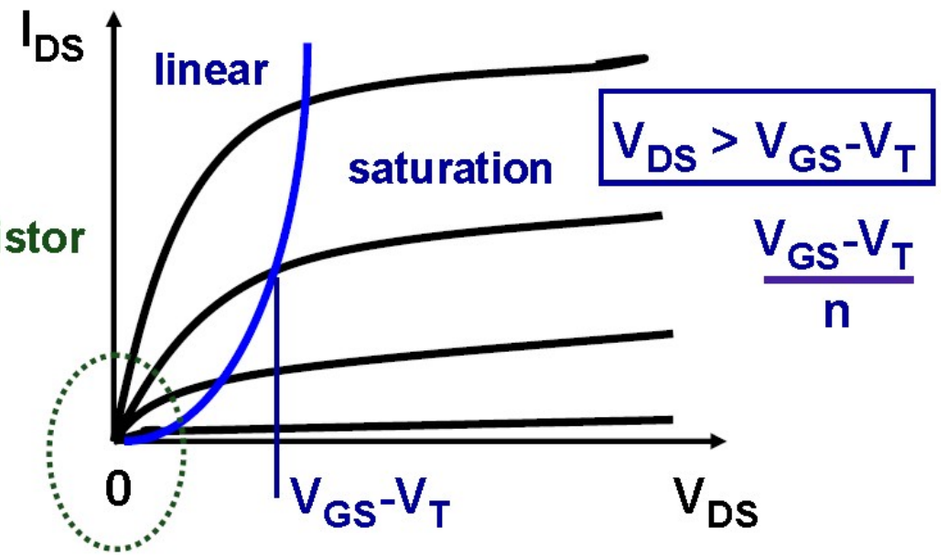
$$i_D\,dx = \mu_n C_{ox} W[v_{GS} - V_t - v(x)]\,dv(x)$$

$$\int_0^L i_D\,dx = \int_0^{v_{DS}} \mu_n C_{ox} W[v_{GS} - V_t - v(x)]\,dv(x)$$

$$i_D = (\mu_n C_{ox})\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

MOSFET “square-law” (SL) equation: linear region

[Sansen, 2006]



Linear resistor

$$R_{on} = \frac{1}{\beta (V_{GS}-V_T)}$$

$$\beta = KP \frac{W}{L}$$

$$KP = \mu C_{ox}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$t_{ox} = \frac{L_{min}}{50}$$

$KP_n \approx 300\ \mu A/V^2$

$C_{ox} \approx 5\ 10^{-7}\ F/cm^2$

$\varepsilon_{ox} = 0.34\ pF/cm$

$\varepsilon_{si} = 1\ pF/cm$

$t_{ox} = 7\ nm$

$L_{min} = 0.35\ \mu m$

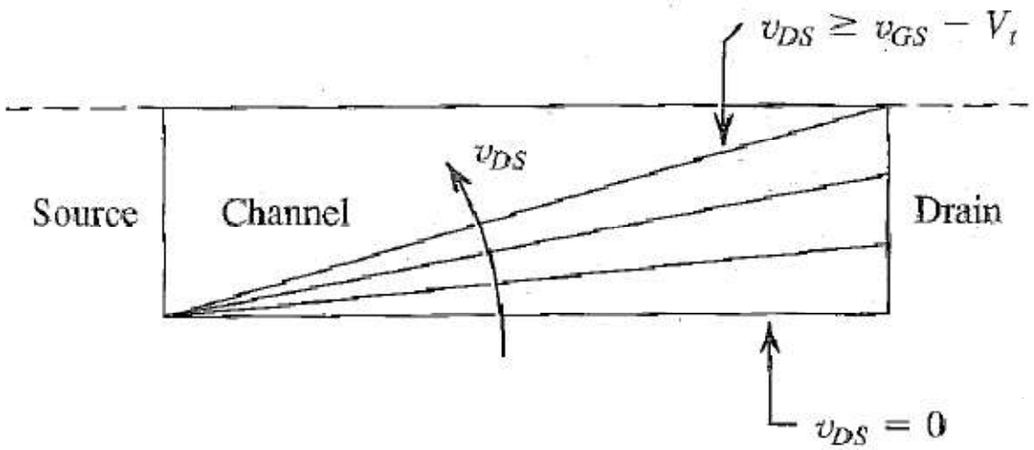
$\mu_p \approx 250\ cm^2/Vs$

$\mu_n \approx 600\ cm^2/Vs$

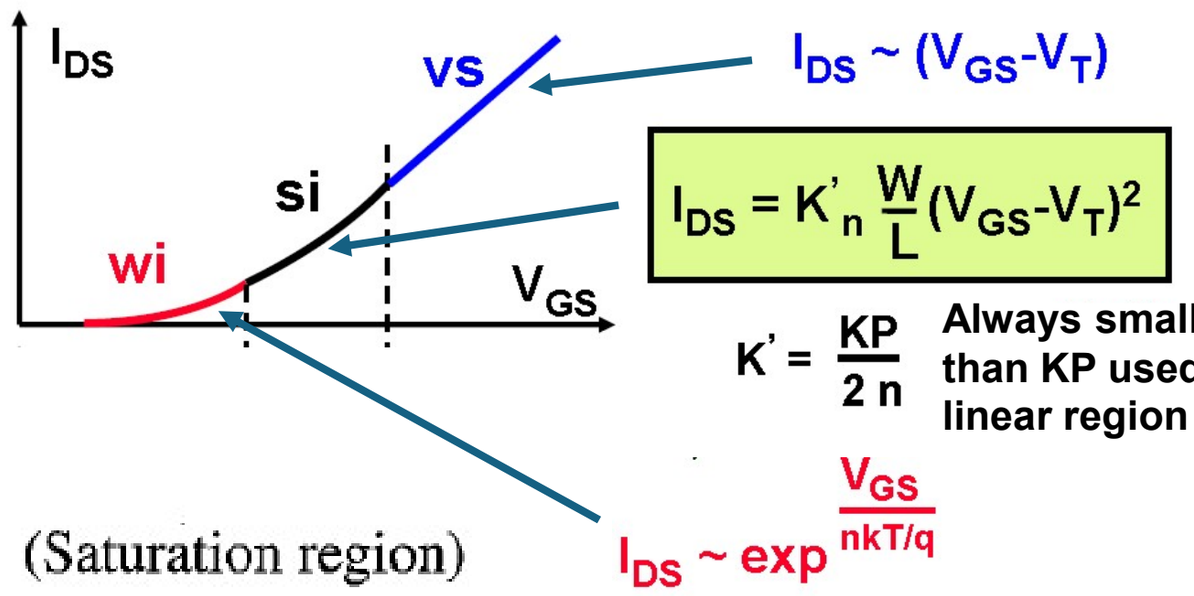
$$i_D = KP \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \quad \text{(Triode region)}$$

MOSFET "square-law" (SL) equation: saturation region

[Sansen, 2006]



$$i_D = \frac{1}{2}\,\frac{KP}{n}\,\frac{W}{L}(v_{GS} - V_t)^2$$

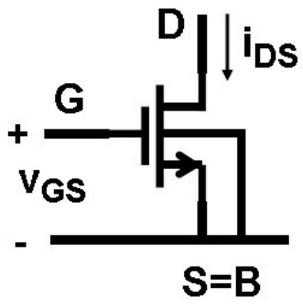


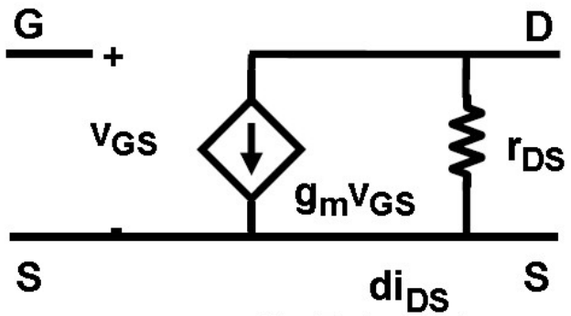
(Saturation region)

- 3 distinctive regions:
  - → **weak inversion (exponential) region → diffusion current**
  - → **strong inversion (square law) region → drift current**
  - → **velocity saturation (linear) region → electron collision**

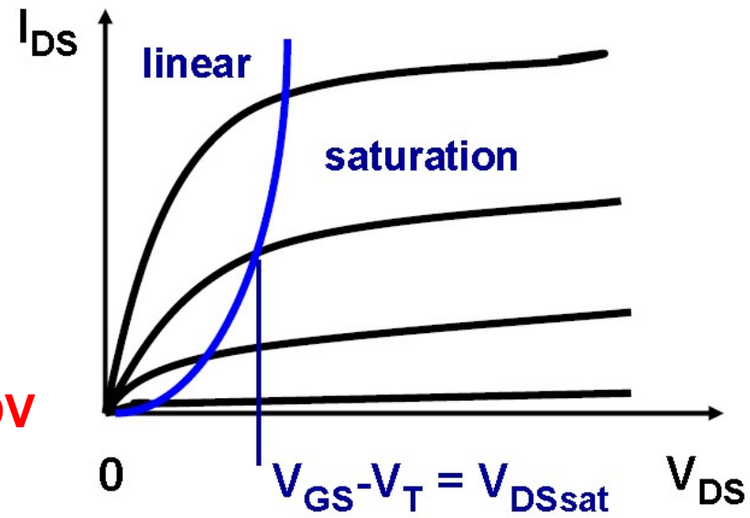
NMOS in saturation region: small-signal model

[Sansen, 2006]





$$g_m = \frac{di_{DS}}{dv_{GS}}$$



$$r_{DS} = r_o = \frac{V_E L}{I_{DS}}$$

$$\lambda = \frac{1}{V_E L}$$

V_{En} = 4 V/μmL

L = 1 μm

I_{DS} = 100 μA

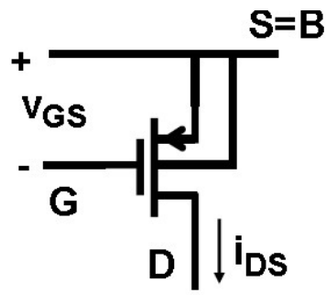
r_o = 40 kΩ

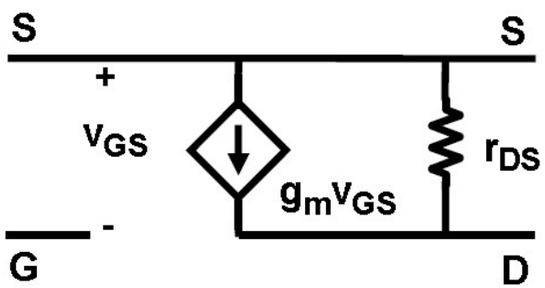
V_{OV}

$$g_m = 2K'_n \frac{W}{L}(V_{GS}-V_T) = 2\sqrt{K'_n \frac{W}{L} I_{DS}} = \frac{2 I_{DS}}{V_{GS}-V_T}$$

$$I_{DS} = K'_n \frac{W}{L}(V_{GS}-V_T)^2(1 + \lambda V_{DS})$$

- I_{DS}: bias current + i_{DS}: small signal (or AC) current
- Four technological parameters:
  → V_T, KP, n and V_E
- Design parameters → W, L and V_{GS} - V_T





PMOS small-signal model

Body effect – parasitic JFET

[Sansen, 2006]

$$V_T = V_{T0} + \gamma \left[\sqrt{|2\Phi_F| + V_{BS}} - \sqrt{|2\Phi_F|} \right]$$

$$n = \frac{\gamma}{\sqrt{|2\Phi_F| + V_{BS}}} = 1 + \frac{C_D}{C_{ox}}$$

$|2\Phi_F| \approx 0.6$ V

$n \approx 1.2 \ldots 1.5$

$\gamma \approx 0.5 \ldots 0.8\ V^{1/2}$

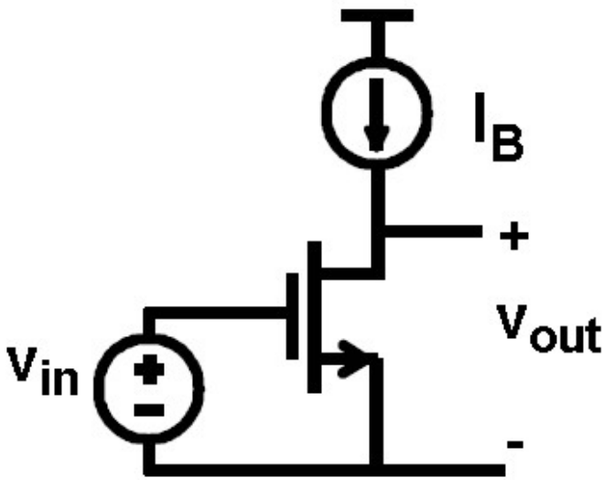
Reverse v_{BS} increases $|V_T|$ and decreases $|i_{DS}|$!!!

$n = 1/\kappa$ subthreshold gate coupling coeff. Tsividis

- γ: junction depletion region parameter, related to parameter n
- ϕ_F: related to Fermi energy → characterizes semiconductor material at certain temperature

MOSFET as amplifier

[Sansen, 2006]



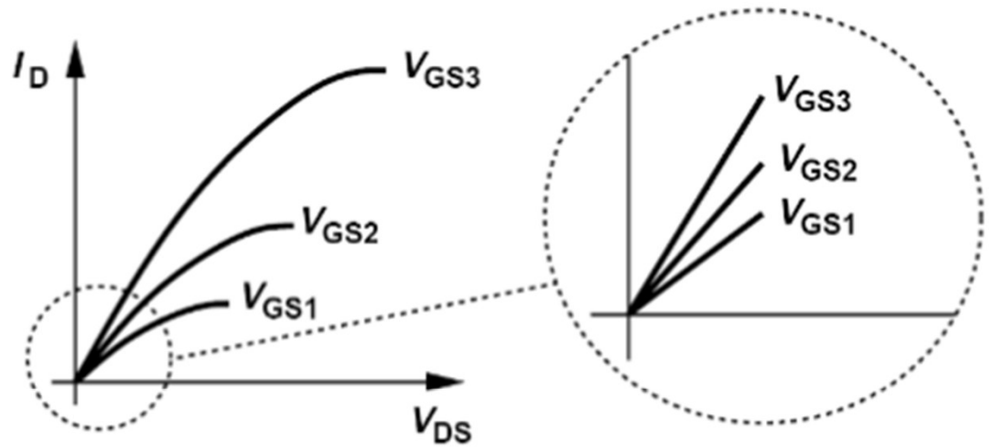
$$A_v = g_m r_{DS} = \frac{2 V_E L}{V_{GS}-V_T}$$

$$A_v \approx 100$$

If $V_E L \approx 10$ V

and $V_{GS}-V_T \approx 0.2$ V

MOSFET as switch

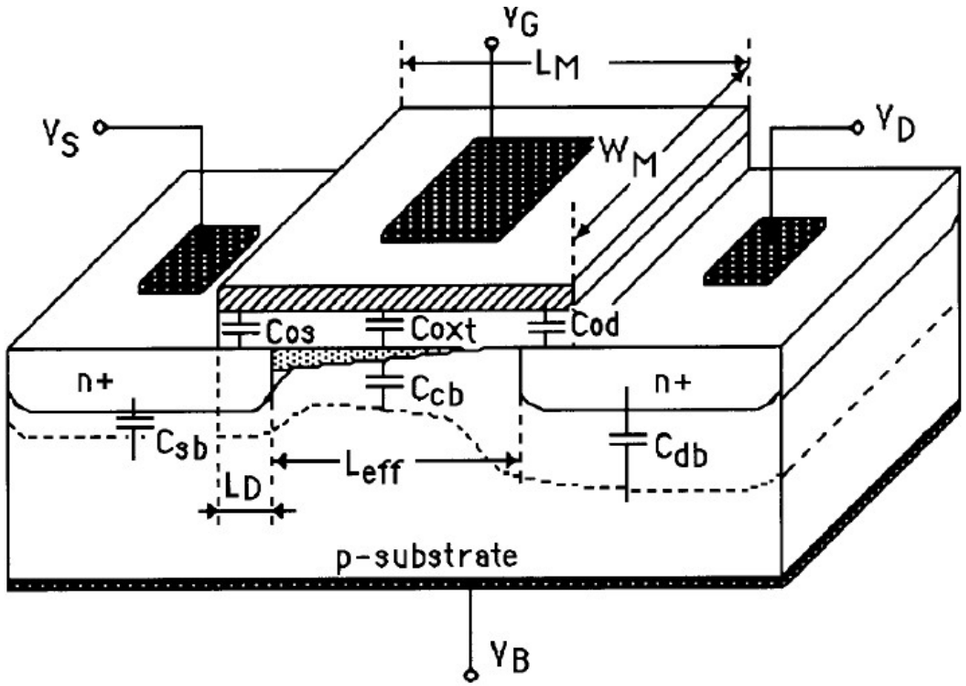


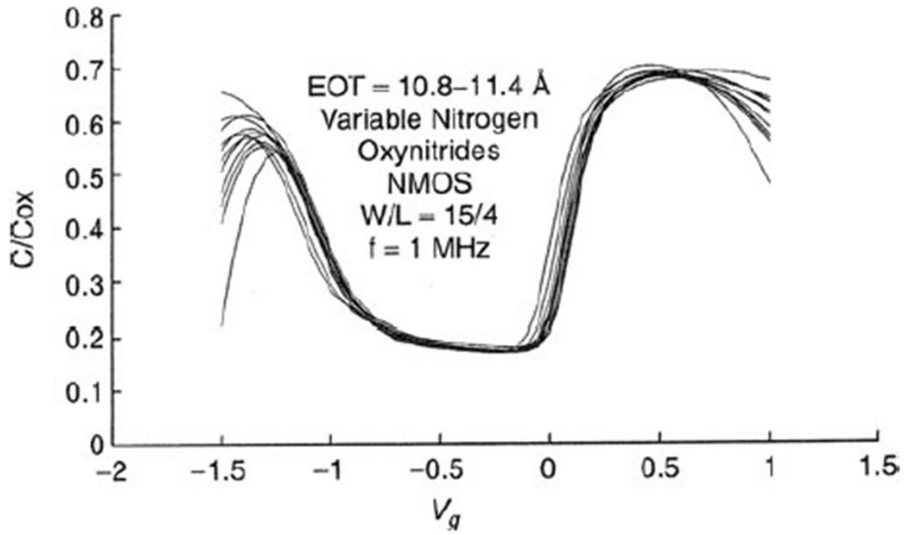
For large channel and small VDS:

$$I_D \approx \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

$$R_{on} \approx \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$

MOSFET as switch





$$A_{Cc} = \frac{C}{C_{ox}} = nWL$$

Need to consider:

- **Overlap capacitance**
- **Routing capacitance**

Transmission gate simulation

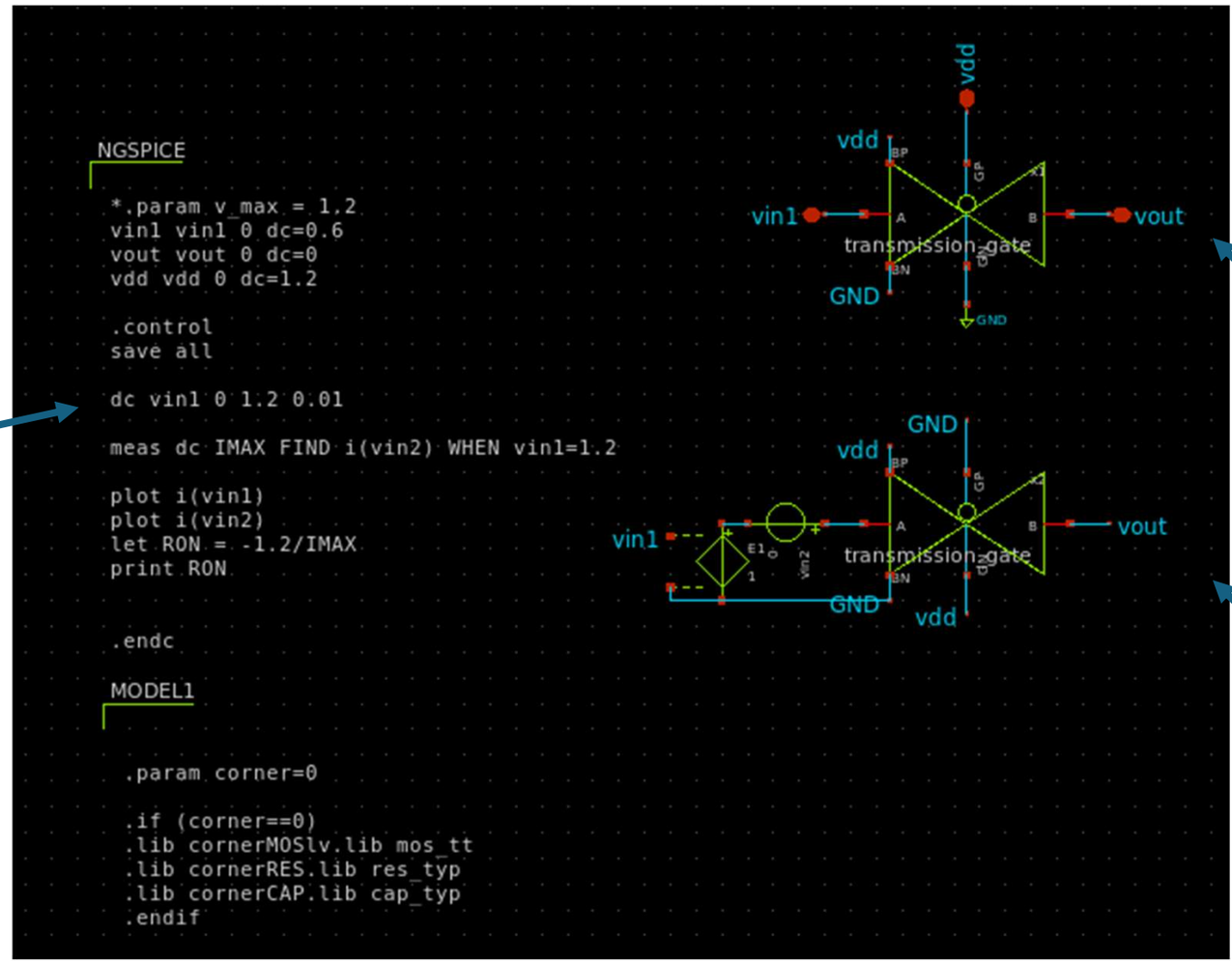
Update Workshop repo

- these slides: OS_AnalogIC_UCU_July2025/Day2/docs
- OUTSIDE Docker:
  - → cd [YOUR_INSTALL_FOLDER]\uniccass-icdesign-tools\shared_xserver\OS_AnalogIC_UCU_July2025
  - → git status
  - → (git restore .)
  - → git pull

Example #1: Basic inverter

- Github link:

→ https://github.com/JorgeMarinN/OS_AnalogIC_UCU_July2025/blob/main/Day2/tb_transmission_gate.sch



DC simulation

ON device

OFF device

Task: tgate + inverter

Task

- Modify the transmission gate block and testbench to include an inverter
  - Option 1: add stdcell
  - Option 2: use custom circuit
- Size the transistors for RON = 100 Ohm, monitoring the leakage current
  - What about 10 Ohm?
- [extra] Design a 4-bit analog MUX

Thank you!
Questions?