Chipathon 2025
AC3E-Chile team

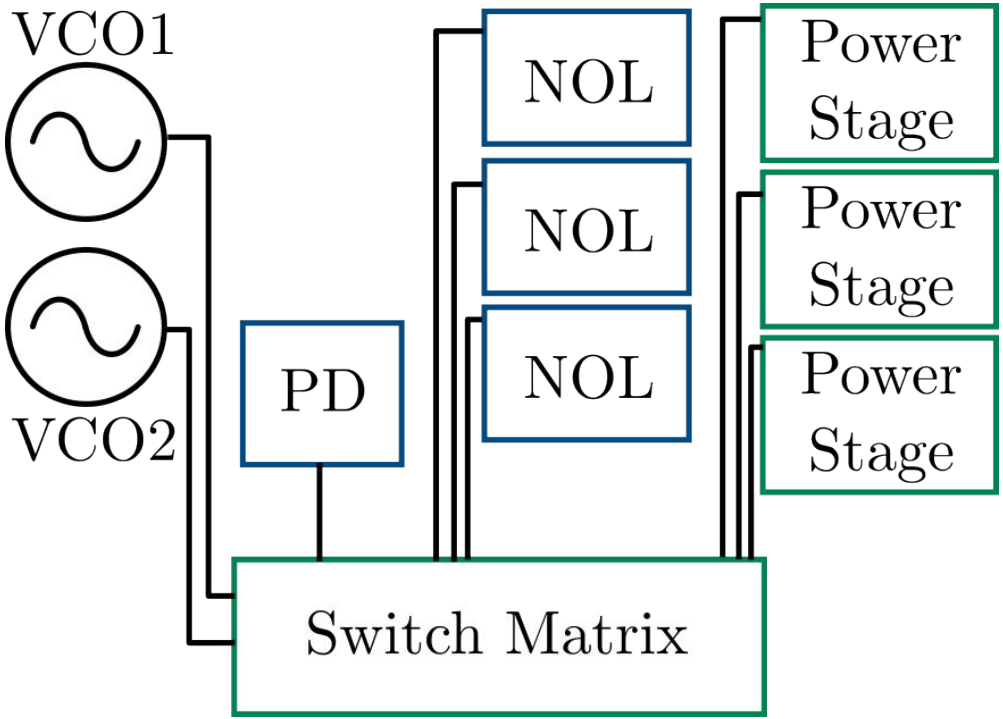
Power MOSBius - Project proposal

Datasheet - Functionality

- Power integrated circuits are a growing topic in the context of energy autonomous and compact electronic systems: IoT, wearables, nanosatellites, etc.
- At AC3E-USM, we have been researching and implementing power management integrated circuits using open source tools for the last 3 years
  - Easy to implement + modular + friendly with older technologies
- Our goal is to implement an educational chip for integrated power electronics - Power MOSBius -, with the following features:
  - Full closed DC-DC buck converter operation test - with digital and time-based control
  - Full 3-phase closed DC-DC buck converter operation test - with digital and time-based control
  - Full closed DC-DC buck converter differential operation test - with digital and time-based control
  - Independent testing of each building block, including: open loop buck operation, VCO characterization and digital circuit testing

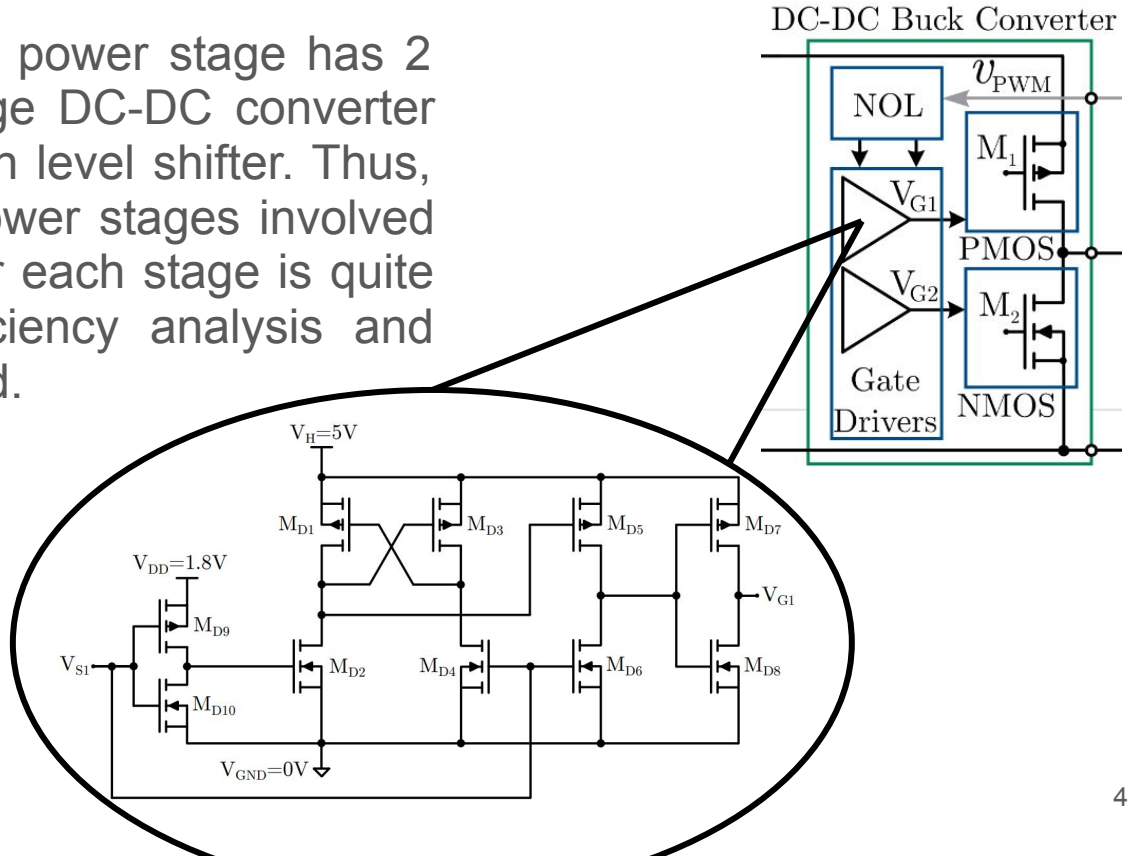
Datasheet - Block diagram

- To achieve this goal, the plan is to have a set of building blocks that, through the usage of the MOSbius switch matrix, will allow the implementation and testing of the different features



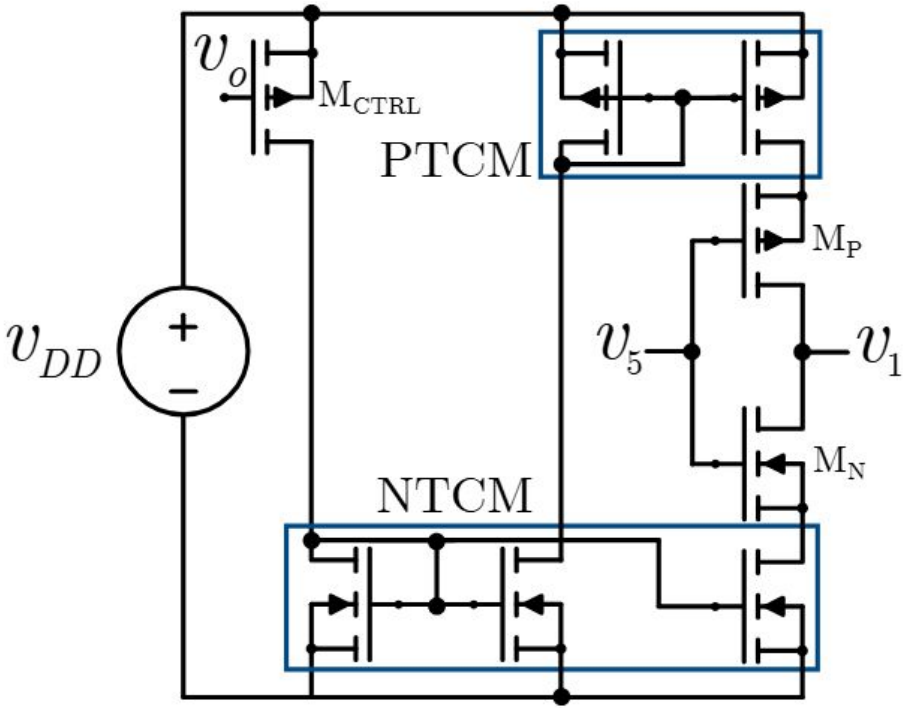
Datasheet - Block diagram (Power Stage)

- Regarding complexity, the power stage has 2 transistors for a half bridge DC-DC converter and 10 transistors for each level shifter. Thus, 66 transistors for the 3 power stages involved in the chip. The design for each stage is quite complex due to the efficiency analysis and maximum current expected.



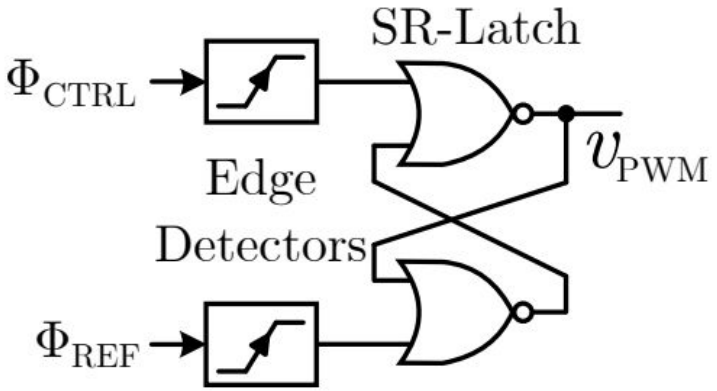
Datasheet - Block diagram (VCO)

- For the ring VCO, each stage will have 8 transistors. Depending on the phases required for the converters, the number stages for the ring will change using the switch matrix. The complexity for this design relays on the central frequency requirement and linearity, which is increases due to the amount of transistor parameters that affect it.

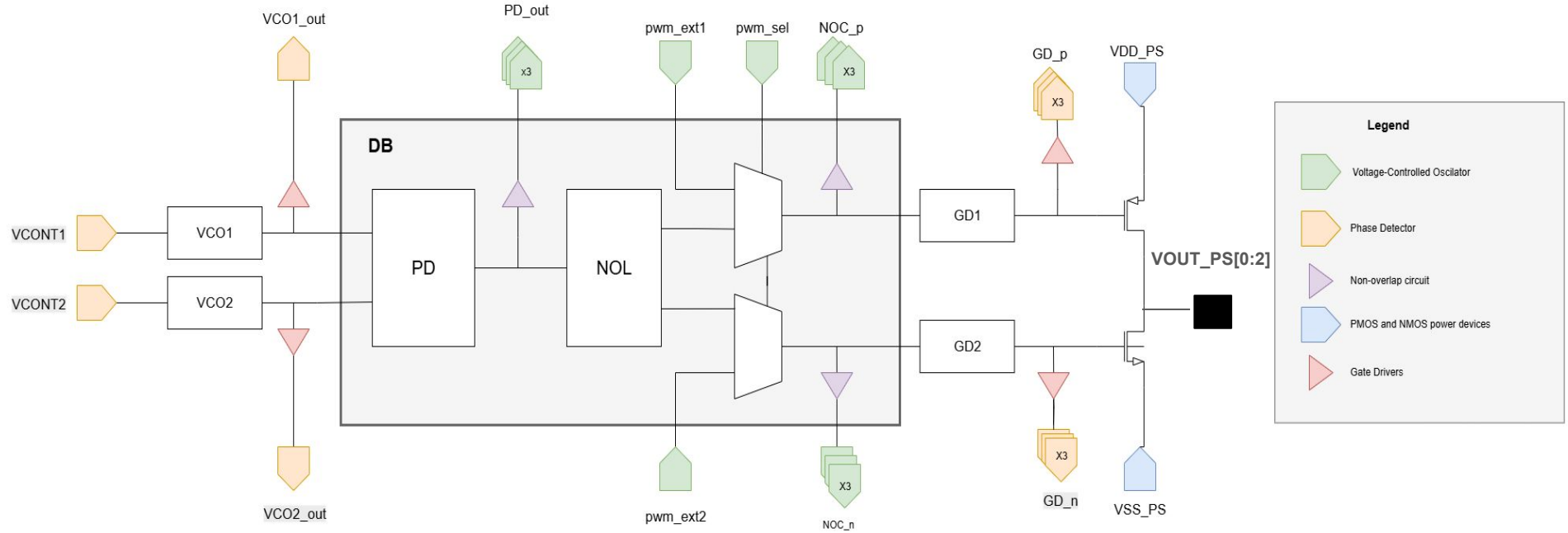


Datasheet - Block diagram (PD, NOL)

- For the Phase Detector (PD) and Non-Overlapping (NOL) blocks, the complexity is low due to the usage of standard cells from the GF180 library. Regarding the number of transistors, it is unknown at the moment as the standard cells haven’t been explored internally.



Datasheet - Pinout



Datasheet - Pinlist

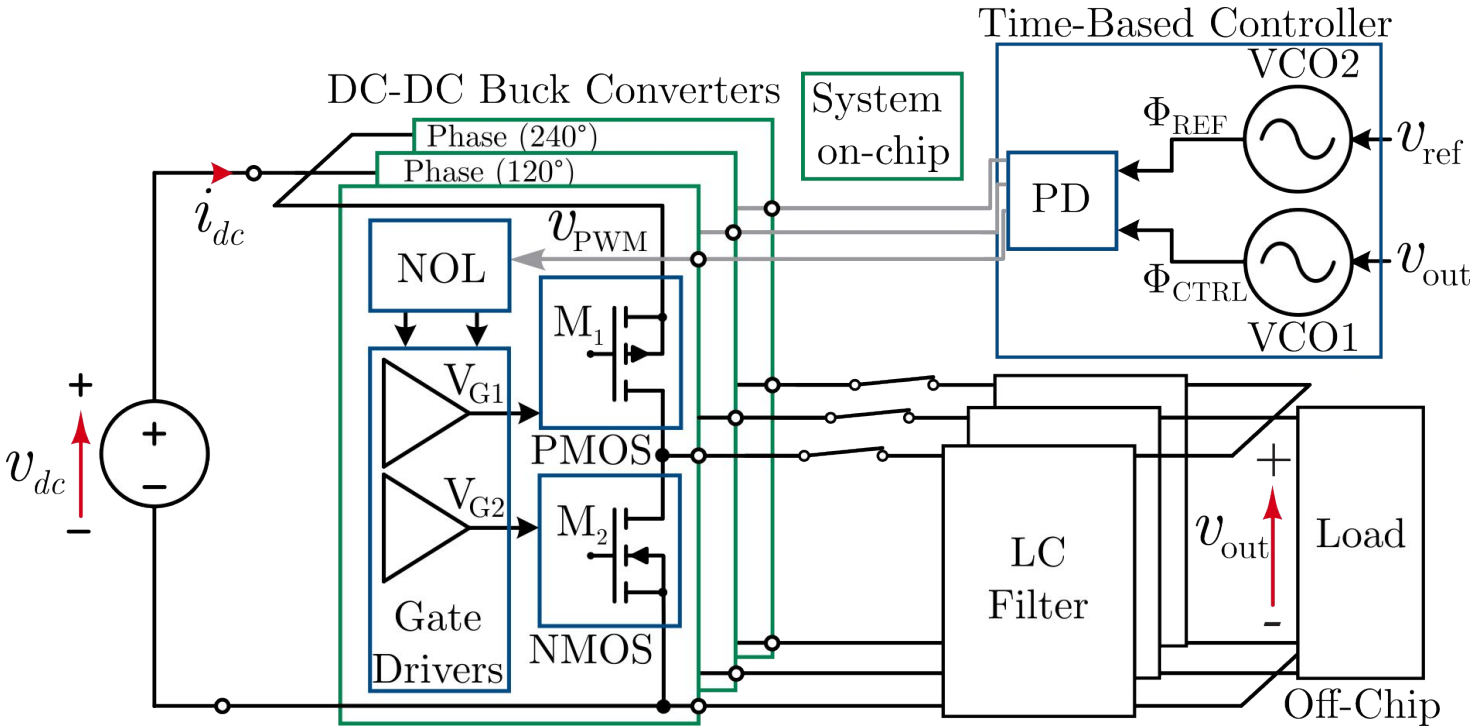
Pin #	Pin name	type	Description
1	VCONT1	Input	Voltage-Controlled Oscillator control voltage
2	VCONT2	Input	Voltage-Controlled Oscillator control voltage
3	VCO1_out	Output	Output of Voltage-Controlled Oscillator
4	VCO2_out	Output	Output of Voltage-Controlled Oscillator
5	PD_out_1	Output	Output of Phase Detector
6	PD_out_2	Output	Output of Phase Detector
7	PD_out_3	Output	Output of Phase Detector

Pin #	Pin name	type	Description
8	pwm_ext1	Input	PWM external input
9	pwm_ext2	Input	PWM external input
10	pwm_sel	Input	PWM mode selection
11	NOC_p_1	Output	Non-Overlapping Circuit control signal- positive side
12	NOC_p_2	Output	Non-Overlapping Circuit control signal- positive side
13	NOC_p_3	Output	Non-Overlapping Circuit control signal- positive side
14	NOC_n_1	Output	Non-Overlapping Circuit control signal- negative side
15	NOC_n_2	Output	Non-Overlapping Circuit control signal- negative side
16	NOC_n_3	Output	Non-Overlapping Circuit control signal- negative side

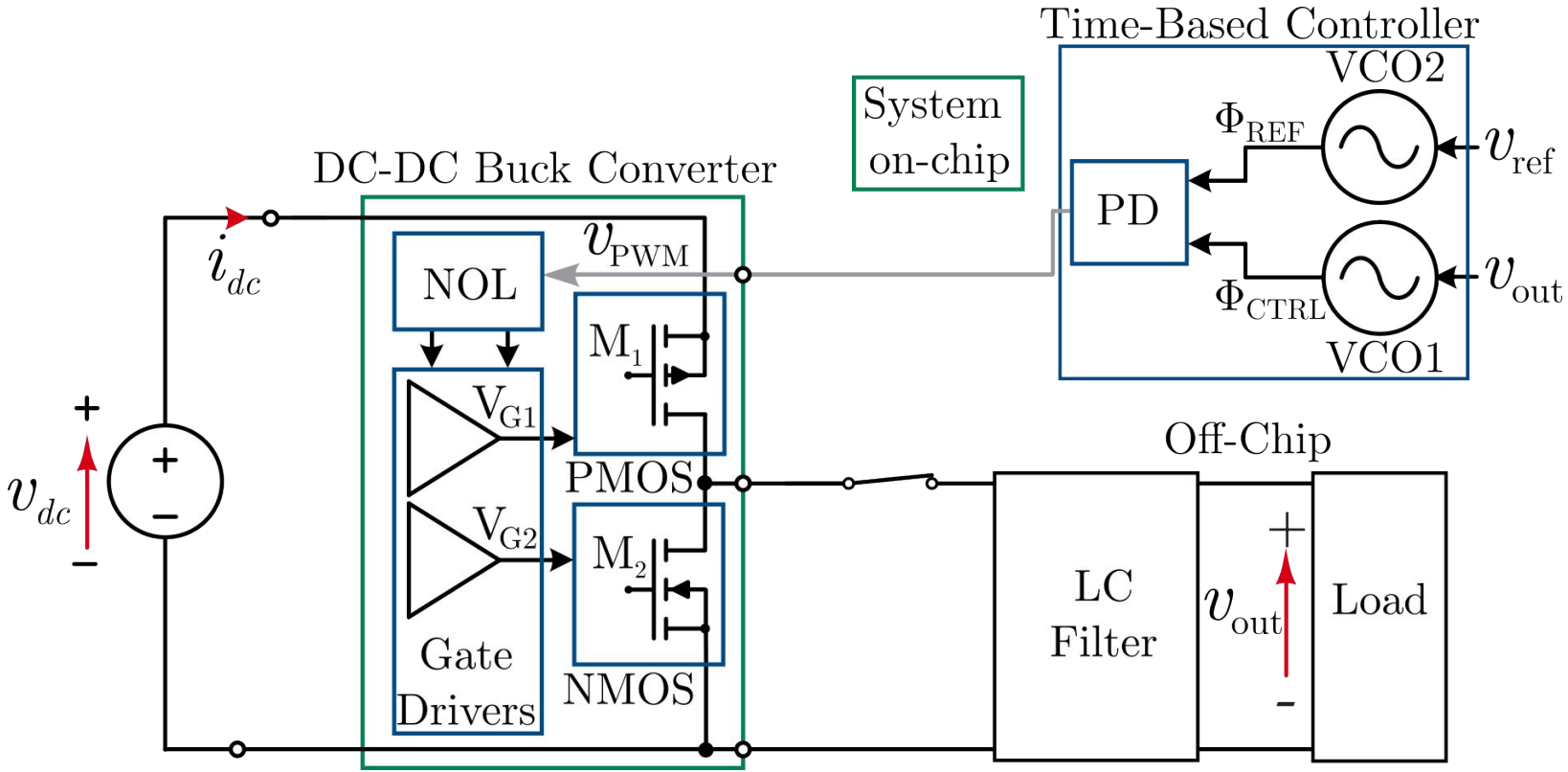
Datasheet - Pinlist

Pin #	Pin name	type	Description
17	GD_p	Output	Gate driver control signal for PMOS (positive side)
18	GD_p	Output	Gate driver control signal for PMOS (positive side)
19	GD_p	Output	Gate driver control signal for PMOS (positive side)
20	GD_n	Output	Gate driver control signal for PMOS (negative side)
21	GD_n	Output	Gate driver control signal for PMOS (negative side)
22	GD_n	Output	Gate driver control signal for PMOS (negative side)
23	VDD_CTRL	Input	Power Supply Voltage for PD,NOL and VCO
24	VDD_PS	Input	Power Supply Voltage for the power stage
25	VSS_PS	Input	Ground reference for the power stage
26	VOUT	Output	Output Voltage
27	CLK	Input	Switch matrix Clock inputl
28	EN	Input	Switch matrix manual enable
29	DT	Input	Switch matrix Data input

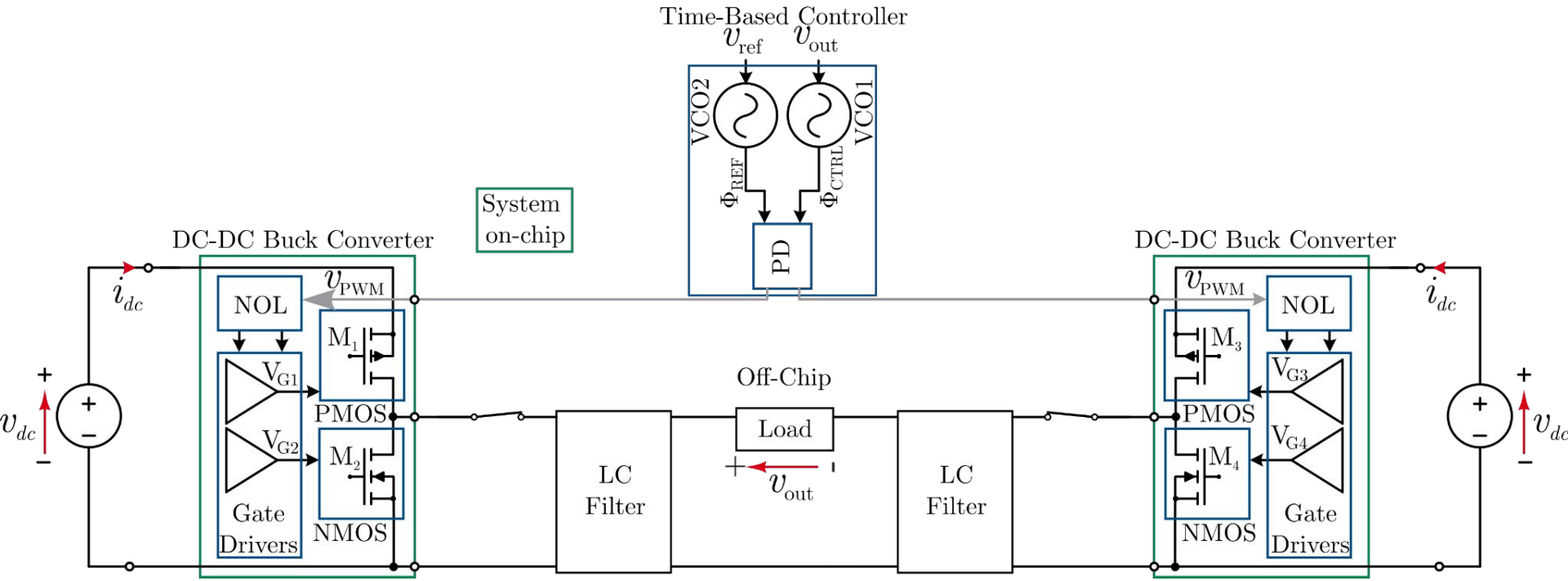
Datasheet - Application diagram: three-phase operation



Datasheet - Application diagram: single-phase operation

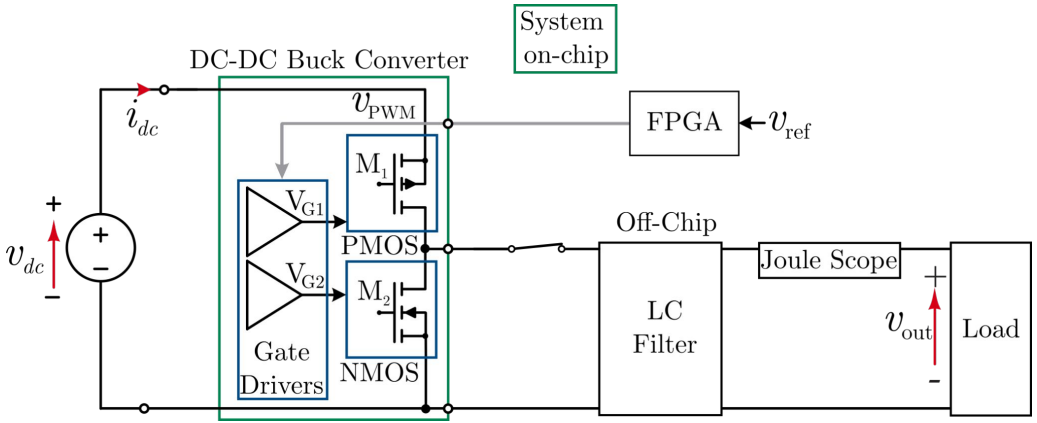


Datasheet - Application diagram: differential operation

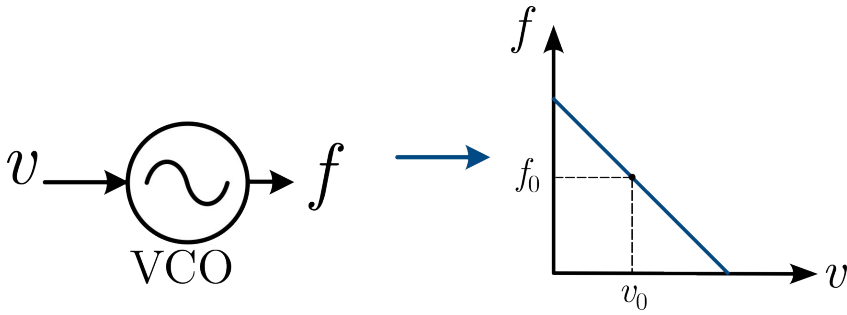


Datasheet - Application diagram: single-block testing

1. Open-loop operation



2. VCO characterisation



3. Testing of digital blocks

NOTES ON FPGA:

- Model: Nexys A7 FPGA (used in previous work)
- Why FPGA? Need short dead time values for open-loop op.
- FPGA will also be used for switch matrix control to avoid several boards

Team members + tasks

- Power stage + gate driver design
  - Maximiliano Jofré + Felipe Rojas
- Switch matrix layout macros
  - Fernanda Quintana + Max Vega
- Digital circuit (phase detector + dead time) design and automated layout
  - Jesus Ávila, Manuel Díaz, Julián Cardozo y Fernando Bonomi
- VCO design, top level simulations and proposal writing
  - Vicente Osorio + Jorge Marín
- Top integration
  - All members

Week-by-week schedule

Chipathon plan	Week	Task group: Power stage + gate driver design	Task group: Switch matrix layout macros	Task group: Digital circuit (phase detector + dead time)	Task group: VCO design + top level simulations	Task group: Top integration
Team Formation and Project Planning	27	N/A	* Preliminary layout scripting in Python	* Preliminary study of sch2gds flow	* Proposal writing * First VCO simulations	* Preliminary block and pin definitions
	28	* PS + GD circuit simulation in GF180	* Switching matrix specification definition	* Preliminary study of sch2gds flow	* VCO optimization + circuit simulation	* Improved block and pin definitions
	29	* PS + GD circuit simulation in GF180	* Transmission gate design	* Migration of PD + NOL from IHP to GF	* VCO optimization + circuit simulation	* Improved block and pin definitions
	30	* Power transistor layout	* Transmission gate layout (scripted)	* Migration of PD + NOL from IHP to GF	* VCO + PD + NOL circuit simulation	* Pad ring initial floorplan
Design and Simulation	31	* Power transistor layout	* Tgate array layout (scripted)	* VCO cell layout		* Pad ring initial floorplan
	32	* Gate driver layout	* Digital switch matrix circuitry definition	* VCO cell layout		* Help in top integration
	33	* Gate driver layout	* Digital switch matrix circuitry design	* VCO top layout		* Help in top integration

Week-by-week schedule

Layout and Verification	**34**	* PS + GD layout	* Integration of Tgate array + digital circuits	* VCO top layout		* Help in top integration
	35	* PS + GD layout	* Integration of Tgate array + digital circuits	* Help in top integration	* Help in top integration	* Help in top integration
	36	* Help in top integration	* Tgate + digital co-simulation	* Help in top integration	* Help in top integration	* Help in top integration
	37	* Help in top integration	* Tgate + digital co-simulation	* Help in top integration	* Help in top integration	* Help in top integration
	38	* Help in top integration	* Help in top integration	* Help in top integration	* Help in top integration	* Help in top integration
	39	* Help in top integration	* Help in top integration	* Help in top integration	* Help in top integration	* Help in top integration
	40	* Help in top integration	* Help in top integration	* Help in top integration	* Help in top integration	* Help in top integration