Homework 4

Re-submit Assignment

Due Mar 15 by 11:59pm **Points** 100 **Submitting** a text entry box or a file upload
Available after Mar 8 at 12am

For this assignment, you will familiarize yourself with the Verilog compiler tool (VCS)

Follow the instructions in the slides: "Homework 4 slides.pdf". It is assumed that you already have an ECS account and have some familiarity with Linux or Unix OS commands.

The Verilog files are already provided to facilitate the process of learning how to use the tool. Nonetheless, you should spend some time understanding the Verilog constructs and the way the testbench interacts with the main circuit.

There are 3 deliverables (all must be submitted online)

1) An output file from your simulation of the full_adder,

2) An executable file "simv" that is generated when you compile the full_adder_wires[_tb].v files.

3) A brief description of how the full_adder_wires[_tb].v Verilog files were able to make the internal signals w1, w2, w3 visible at the top level. For this, you will need to understand what was done differently in these files compared to the simple full_adder[_tb].v.

The following are the slides and Verilog files.

Homework 4 slides.pdf

full_adder.v

full_adder_tb.v

full_adder_wires.v

full_adder_wires_tb.v

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Submission

Submitted!
Mar 13 at 9:15pm
Submission Details
Download HW4_RONGGUANGOU.txt
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Grade: 100 (100 pts possible)
Graded Anonymously: no

Comments:
No Comments