# Project 1

Re-submit Assignment

**Due** Apr 1 by 11:59pm **Points** 100 **Submitting** a file upload

**Project 2: Design a 3-bit Carry Propagate Adder (CPA) Structural Model**

Design and simulate a structural model (not behavioral) of a 3-bit CPA adder. Follow the steps below but make sure you read the entire assignment before you start. Refer to Homework 4 and Chapter 2 for examples of structural models and structural circuit models. You are allowed to work in groups of 2 but you could work alone if you choose to.

**1. Structural model of CPA:**

Design a 3-bit CPA adder as follows:

First, create a structural model of a 1-bit Full Adder (refer to homework 4) and instantiate it 3 times inside your 3-bit CPA module and make the necessary wire connections. To instantiate the Full adder module, you need to add an **`include** line on top of your CPA Verilog module.

Your module ports (inputs and outputs), should be as follow:

```
`include full_adder.v

module adder_3bits

(

input [2:0] a, b,

input cin,

output [2:0] sum,

output co

);
```

**2. Create a test bench to test the following cases:**

a = 3'b001 b = 3'b001 cin = 1'b0
a = 3'b011 b = 3'b010 cin = 1'b1
a = 3'b011 b = 3'b100 cin = 1'b0
a = 3'b111 b = 3'b001 cin = 1'b0

Your test bench should clearly display the inputs and output results.

Refer to Homework 4 and the textbook to create a Verilog testbench module and enter the above test cases as test vectors. Note, you must simulate to get outputs from your Verilog model.

**3. Each student must submit individually to Canvas**

a) Verilog models of Full Adder, Carry Propagate Adder (CPA) and Testbench.

c) The executable created during compilation "simv"

b) The screenshot of your simulation results.

## Submission

**Submitted!**

Apr 1 at 12:36am

Submission Details
Download adder_3bits_tb.v
Download adder_3bits.v
Download fullAdder.v
Download simv-1
Download compile.png
Download outfile_result.png

Grade: 100% (100 pts possible)
Graded Anonymously: no

**Comments:**
No Comments