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**Guidelines**:

* The questionnaire must be answered by editing this Word file.
* Rename it with a name including your first name and the course you are enrolled in (By instance *ICRC\_PepitoPerez.docx or MICROELECTRONICA\_PepitoPerez.docx)*
* Send it through the **Moodle** of the coursebefore **February 10th, 2020**
* You can use all the technical documentation you need but never ask your colleagues or any other person. **This is an individual work!**

**QUESTIONS (Answer Briefly)**

1. In your opinion, which are the main challenges for microelectronic design nowadays and for the years to come? Support your opinion with some bibliographic references (cite doi of the paper or full reference).

**Answer:**

1. The cost and the circuit complexity. The complexity is increasing and with it the cost increase also.
2. Testability. Test the complex circuits is also complex.
3. In 3d the new through silicon vias are complex.
4. Also in the new 3d circuits, the heat dissipation is more complex, some circuits heat, go through others circuits before go outside, so the circuits give heat other circuits.

Reference: Unit 1.5 in class.

1. In space environments, the effects of radiations make electrons being faster and holes being slower. To this respect, which type of gate is more susceptible to suffer more from radiation: a) a 4 input NAND gate, b) a 4 input NOR gate, or c) a 4-input NAND gate made up with several two-input NAND gates as the only constituent element (draw the equivalent schematic diagram).

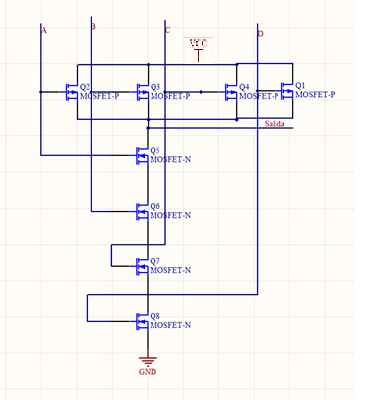


Ilustración 1 4 Input NAND GATE

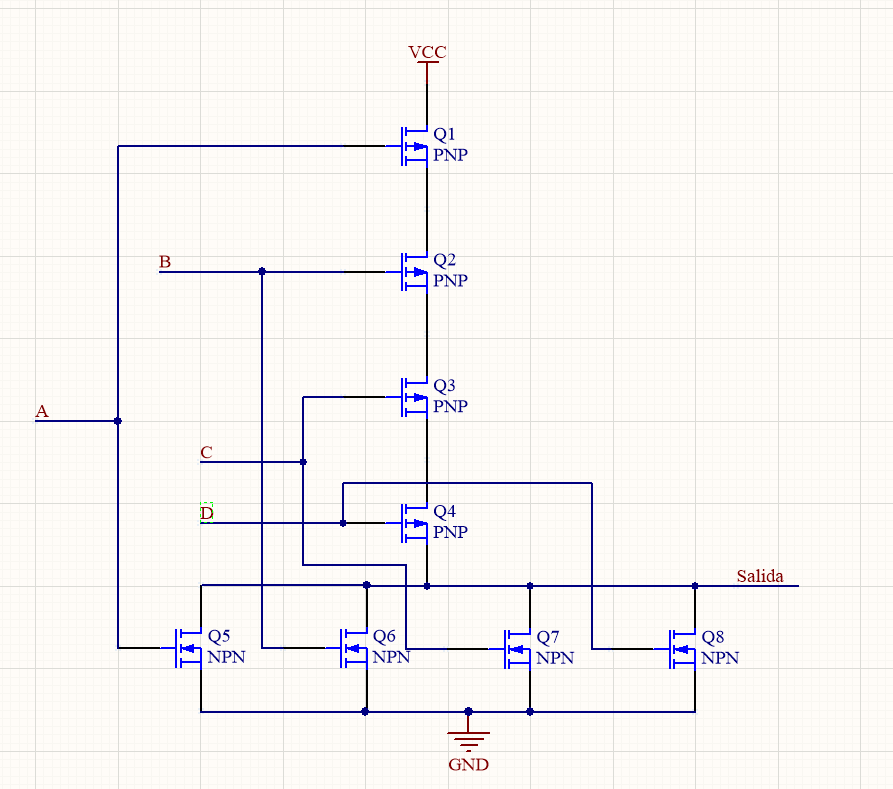


Ilustración 2 4 Input NOR

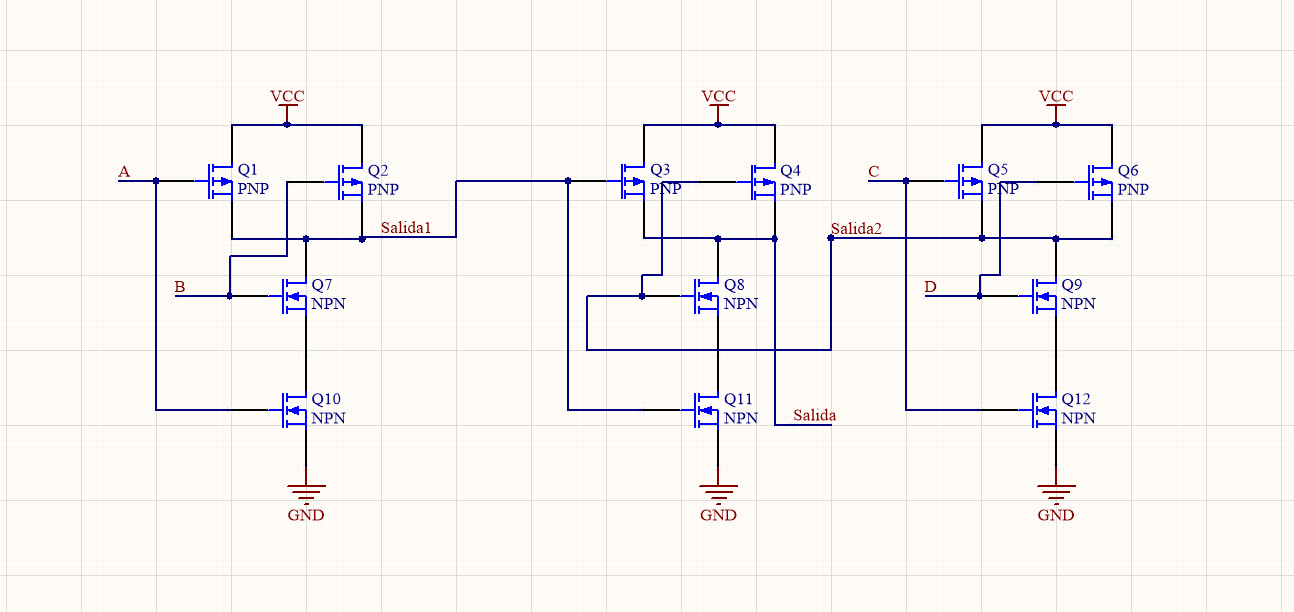
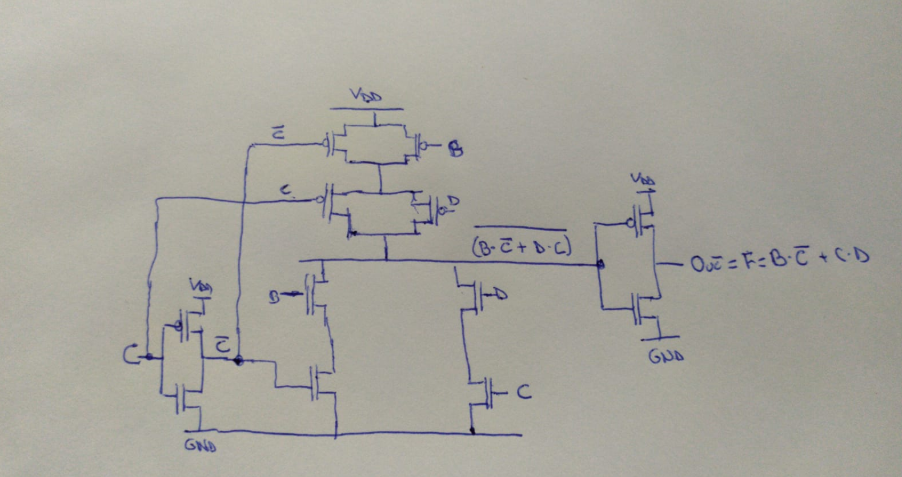
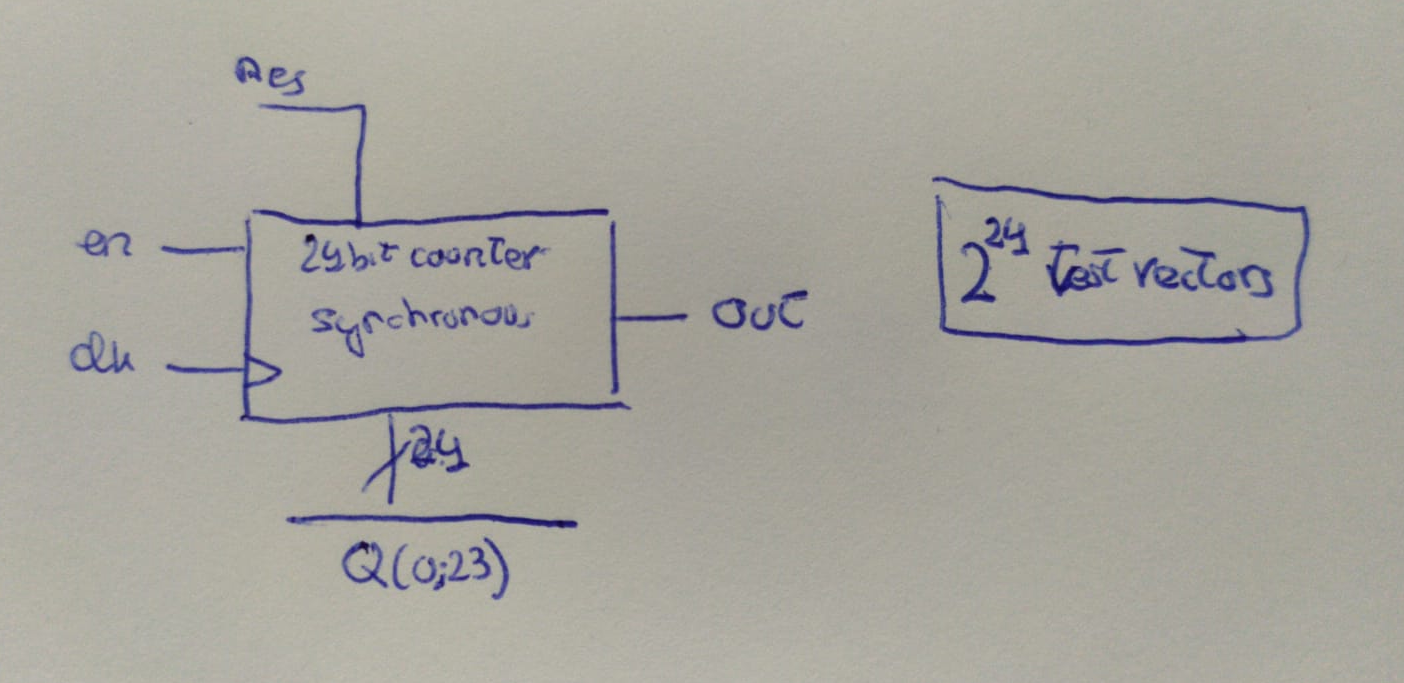


Ilustración 3 NAND 4 INPUTS WITH 2 INPUNTS NANDS

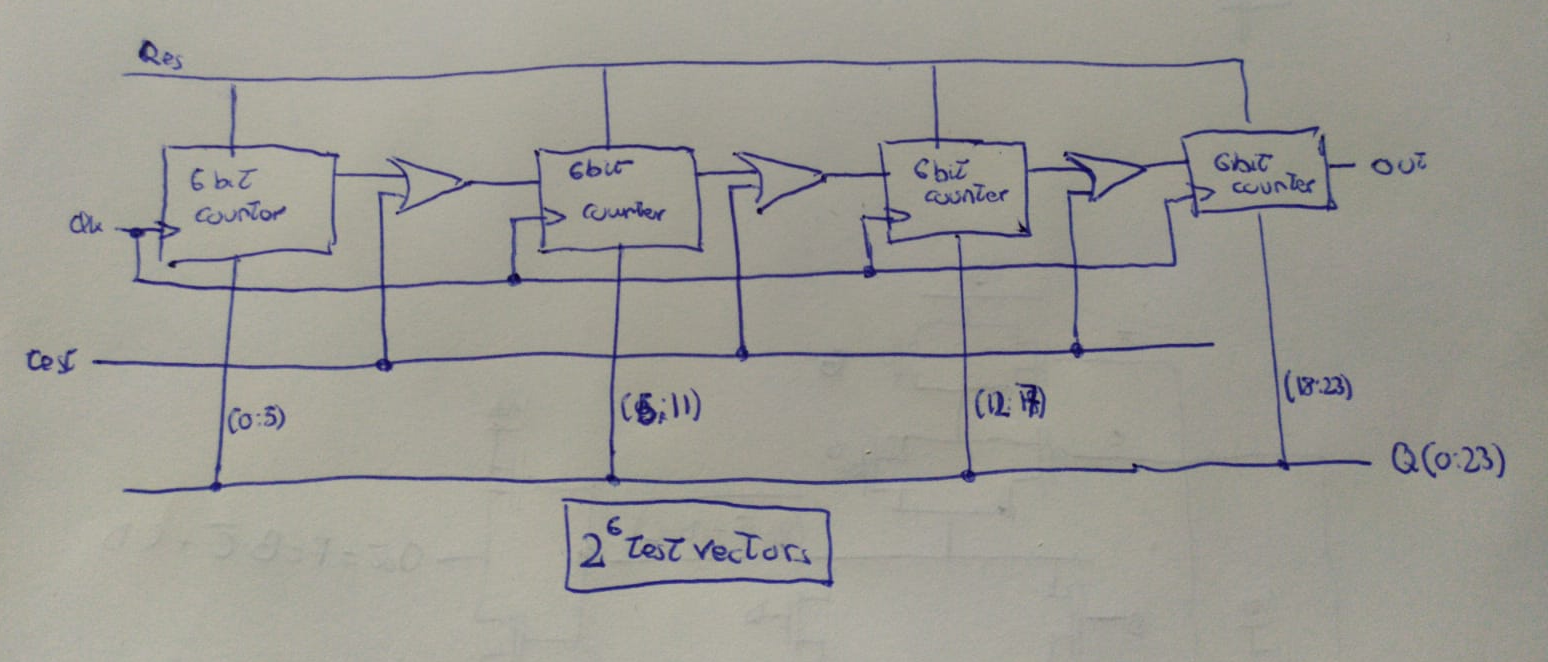
1. Draw a CMOS circuit (at transistor level, not layout) that carries out the logical function with the minimum number of transistors.



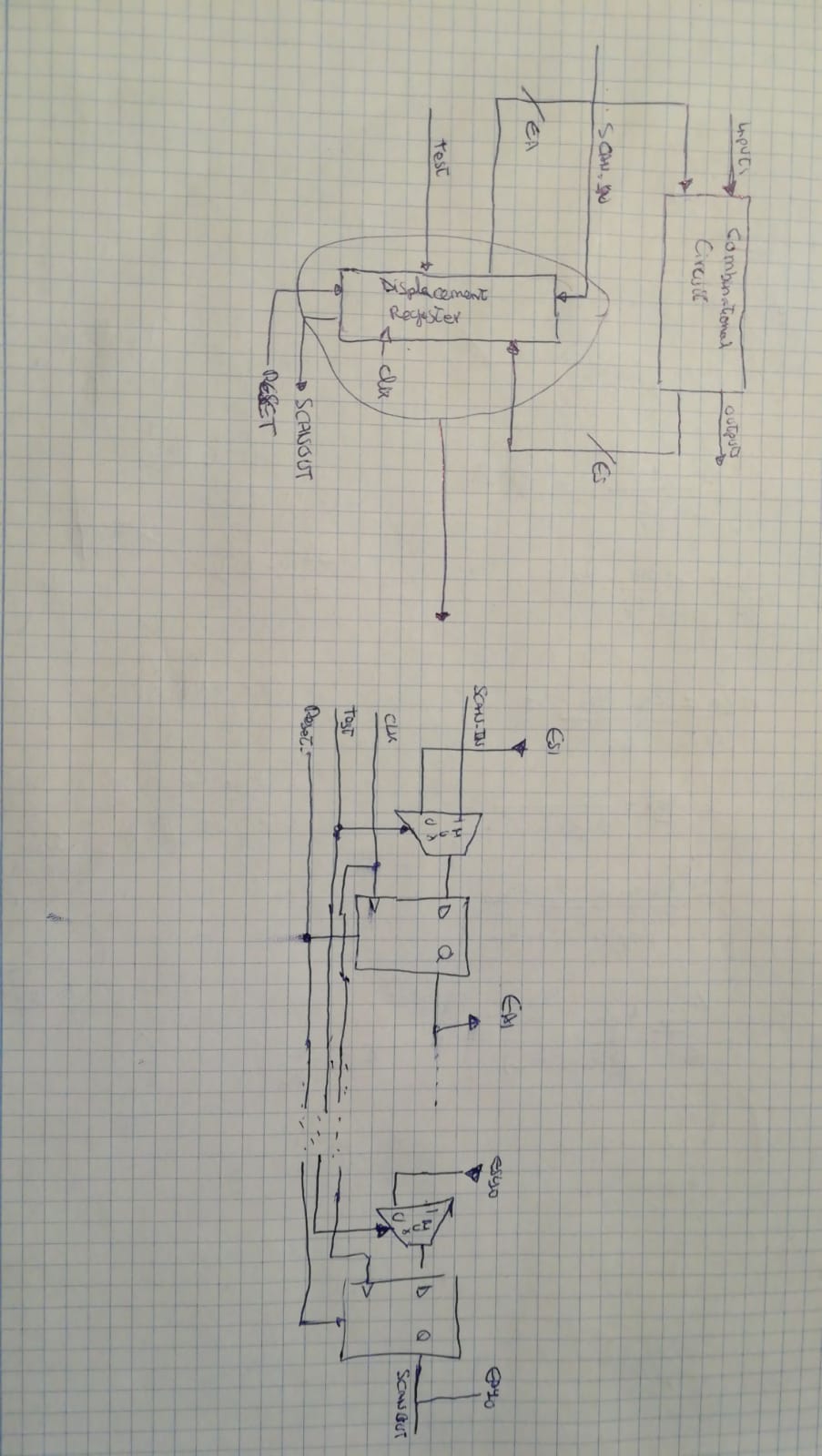
1. A 24 bit synchronous counter needs to be tested for correct manufacturing. Make a rough estimation of how many test vectors are required if the following techniques are planned to be used:
2. No DfT techniques at all



1. A custom counter breakdown, splitting the counter into four equal portions. Draw the resulting circuit



1. A full scan-path approach. Draw the resulting circuit. Consider that all stuck-at-0,1 of the gates around the flip-flops are fully covered with 40 combinational vectors.



1. Enumerate (using a bullet list the application possibilities offered by memristor technology and, for each possible application, suggest a scientific paper (include doi or paper reference) that comments the benefits of such technology.

**Answer:**

1. **Memories:**
   1. <https://www.abc.es/tecnologia/memoria-veces-rapida-llegara-201010180000_noticia.html>
   2. <https://www.muycomputerpro.com/movilidad-profesional/2015/10/12/memristor-hp-sandisk/>
2. **Neurons:**
3. Answer briefly the following questions related with Reconfigurable Systems:
   1. Explain why we say that computation in FPGAs is carried out spatially.
   2. Which is the difference between an Overlay and a Dynamic Partial Reconfigurable Circuit?

**Answer:** Overlays are fixed structures with some reconfiguration capabilities, but they are independent from the FPGA (having portability) and DPR have more reconfigurability but have dependency of the FPGA device.

* 1. What do we mean by granularity? Give some examples of fine grain and coarse grain reconfigurable devices.

**Answer:** The granularity is the size and complexity of the basic computing blocks in and Reconfigurable Device.

Example of fine grain: (Small and simple blocks) 5 bit multiply with a 32-bit processor.

Example of coarse grain: ALUs or small processors.

* 1. Compare CGRAs and FPGAs in terms of their expected reconfiguration times.

**Answer:** CGRAs are faster to reconfigure, less blocks to reconfigure.

1. Answer briefly the following questions related with the design of Dynamic Reconfigurable Systems:
   1. How could be the internal and external fragmentation reduced when designing a dynamic and partial reconfigurable system? Which is the more appropriate virtualization scheme?

**Answer:** Fragmentation reduced using more slots but smaller slots due to avoid to used bigger ones and let a lot of space of an slot unused. The appropriate is the Grid.

* 1. How does the inter-module communication scheme impacts on the relocation of modules?

The modules which will be relocated in the same area have to be similar in the number and type of inputs and outputs.

* 1. What is a Blocker macro? How can a blocker macro be used for the implementation of a Dynamic Reconfigurable System? Which is the alternative to the use of blocker macros?

**Answer:** Blocker Macros are a set of wires included into a design. Blocker Macros are used for avoiding routing conflicts. Alternatives are **Static routes**  and **RM routes fully contained within the RP boundary.**

* 1. Which are the differences between a bus-macro, a proxy logic and a partition pin?

**Answer:** The bus-macro allow Module-Relocation and Independent Design of Modules and the system but not allow Communications Overhead. **Proxy Logic** allow Communications Overhead but not allow Module-Relocation neither Independent Design of Modules and the System.

* 1. What is Out-of-context (OOC) synthesis according to the Xilinx terminology?

1. Answer briefly the following questions related with Operating Systems for Reconfigurable Computing:
   1. Which are typically the main components of a reconfigurable hardware operating system? Which is the impact in the OS when using the 1D versus the 2D area hardware tasks models?

**Answer:** The main components are: Application Layer, Module Layer, Scheduling Layer, Placement Layer, Configuration Layer and HW Layer. In the 2D area task model, HW and SW task communicate with each other at a peer level.

* 1. Compare the Placement and Scheduling services in conventional Operating Systems and Operating Systems for Reconfigurable Computing.

**Answer:** For placement the problem in Conventional OS appears only with Parallelism/multicore systems, while in ReconOs the problem is where to configure de HW tasks.

For Scheduling in Conventional Os is just to see which task is ready to be selected for execution for each scheduling task, while in ReconOs appear the problem of which task has to be configured and after executed.

* 1. Provide the main ideas on the main heuristic algorithms used for the Placement and Scheduling Problems in Operating Systems for Reconfigurable Computing.

**Answer:** For Scheduling problems:

* + - 1. Look for a feasible Temporal Partitioning.
      2. Total execution time must be minimized.

For Placement: Maximize the device occupancy.

* 1. Which are the problems of implementing preemptive multitasking in Operating Systems for Reconfigurable Computing?

1. Discuss how Dynamic and Partial reconfiguration can be applied for increasing reliability in space applications. How can this technique be used for fault injection?

**Answer:** DPR can be used for HW modular redundancy, to increase the reliability of the systems. Having the same module X times, to ensure that the result is OK. Also SCA protection is apply (one positive circuit into negative one). Combined with redundancy can be use if the modules are not doing exactly the opposite, there is a fault.

1. Comment on the differences between a reconfigurable Application-Specific Instruction-set Processor and a Coarse-Grained Reconfigurable Architecture. Provide an in-depth description of one device representative of each class, with some references to the state-of-the-art.

**Answer:** The rASIP processor is one of the more optimized solutions due to the cost and the performance. The reconfigurability allows to point to multiple algorithms. To control the reconfigurable parto f the rASIPS, Para controlar la parte reconfigurable de los rASIP, some special instructions in the instructions set ofthe processors have been added with the aditional needed HW for the interface. The rASIP require less use of area / resource that the traditional systems due to the integrated reconfigurable part with the processor. The logic control is also reduced due to the Flow control is in SW. During the execution, while the reconfigurable part of the rASIP is busy processing the data, the ASIP can manage other apps with less power of calculus.

Although the rASIP are a promising development for the SoC, they consume a lot of energy and a big area.

The **CGRA** have been used for more than10 years. Une of the disadvantages is that a bit area is of some millions of gates is required and it is normally not justified its used. Due to avoid this problem, the CGRA have been designed with a pre-set that can generate accelerators due to solve specifics applications. The CGRA are ideal for processing intensive algorithms for signals, because they offer high performance and parallelism.

Example: The design model of MorphoSys is a SoC of coarse grain oriented for high performance applications, owing to it reconfigurable component to manage parallel operations of data with a huge volume. On the present implementation the reconfigurable component is a matrix of reconfigurable cells. En la implementación actual, el componente reconfigurable es una matriz de celdas reconfigurables (RC) o elementos de procesamiento. The matrix usually are 8x8. The MorphoSys arquitectura is componed of 5 principals components: reconfigurable cell array (RC array), control processor (TinyRISC), context memory, frame buffer and a DMA controller.

* **RC Array.** Due to most applications tend to process data in arrays of 8x8, so the RC array will have 64 cells in a bidimensional matrix. This is selected to maximize the use of the parallelism, improving the performance. The RC Array follow the calculus model SIMD. All the RC in the same row/column share the same configuration data (context). Although, each RC compute with different data. Sharing the contest is usefull for applications with parallel data. The RC array have a big interconnexion network with 3 layers, designed for quick exchange of data. This improve the performance in the cores of applications which ask high data traffic like the transform of a cosene. Each RC include an ALU multiplier, a change unit, Inputs Mux and a Register.
* **Control Processor TinyRISC.** Most of the applications require a secuencial processing, a RISC processor is added in the system, a TinyRISC. It has a 32 bits ALU, a register and a Caché Memory onchip. This processor manage the system performance and it controls also the external interface. This is possible with the addition of special instructions to the TinyRISC ISA. These instructions start data transference between the memory and the other components.
* **Frame Buffer y DMA controller**. Due to take advantage of the high parallelism of the RC array and transferring the data at the appropriate speed rate, a memory interface of high-speed rate with a transmission buffer (Frame Buffer) and a DMA controller are added in the system. Frame Buffer has two complementary signals to allow the superposition of the data transfers with the execution of RC array.
* **Context memory.** It storages many planes of configuration data (context) for the RC array, giving a depth in the programmability. This requires that the system spend less time charging new configuration data. MorphoSys admits the dynamic configuration of 1 cycle.

1. In your opinion, which are the features desired in a device architecture to make it appropriate for partial reconfiguration?

**Answer:** the bus architecture must permit:

* To dispatch data to more than one block
* Make use of burst transactions in order to accelerate.
* To compare and correct several simultaneous transactions in every transaction read
* To collect multiple data and reduce it before going into shared memory.

1. Discuss the main approaches existing in the state-of-the art to reduce reconfiguration time in Xilinx FPGAs. Provide some examples with references to the state-of-the-art.

**Answer:** All the programmable functions by the user inside the Xilinx FPGA and AP SoC are controlled by volatile memory cell that have to be configured at the start. These memories are known as configuration memories and they are there to define the LUTS equations, the signals routing, the IOB voltage standard and the other aspects in the design.

These memories are built in frames, whose height corresponds with a clock region and it will be independent for each family. The reconfigurable frames are based on this configuration frames, and they are the minimum construction blocks due to realize a parcial reconfiguration. [1] Depending on the external or internal ports to use, the minimo of CLBs will be different. On [2], the speed of some different configuration approaches are compared, including the serial configuration, JTAG, SelectMAP and ICAP, it is calculated theoretically the reconfiguration speed (in the ICAP is the faster with 1,64us/frame, where each frame has 41 words of 32 bits).

On [3], different IPs are used, like DMA, Master Burst and BRAM memories due to compare the information transmission to the FPGA when reconfiguring through the ICAP.

The BRAM HWICAP can be near to the ICAP Reconfiguration speed limit, due to using a lot of RAM. Nowadays, the speed is limited artificially by the FPGA manufacturers, but it can be getting bigger speed including ICAP with a personalized logic due to apply and ICAP Hard Macro with overclocking like in [4].

Instead of having a partial bitstream for each RR, having a higher overhead, [5] present the option of using techniques of partial bitstream relocation reducing the overhead, dividing the only one bistream on the different zones, where each one can modify its clock frequency and manage its reconfiguration more efficiently.

**References**

[1] ‘Vivado Design Suite User Guide: Partial Reconfiguration (UG909)’, p. 147, 2018.  
[2] E. J. McDonald, ‘Runtime FPGA Partial Reconfiguration’, in 2008 IEEE Aerospace Conference, 2008, pp. 1–7.  
[3] M. Liu, W. Kuehn, Z. Lu, and A. Jantsch, ‘Run-time Partial Reconfiguration Speed Investigation and Architectural Design Space Exploration’, in In Proc. of the International Conference on Field Programmable Logic and Applications, 2009.  
[4] S. G. Hansen, D. Koch, and J. Torresen, ‘High Speed Partial Run-Time Reconfiguration Using Enhanced ICAP Hard Macro’, in 2011 IEEE International Symposium on Parallel and Distributed Processing Workshops and Phd Forum, 2011, pp. 174–180.  
[5] A. Flynn, A. Gordon-Ross, and A. D. George, ‘Bitstream relocation with local clock domains for partially reconfigurable FPGAs’, in Automation Test in Europe Conference Exhibition 2009 Design, 2009, pp. 300–303.

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X I declare that I have filled this questionnaire alone and that nobody was allowed to copy it