PI3HDMI336

3:1 ActiveEye™ HDMI™ Switch with I²C Control & ARC Transmitter

Features

- HDMI 1.4 compliant with fast video switch among each ports
- I²C control 3:1 HDMI active switch Mux with DC coupled or AC coupled Dual mode DisplayPort signals
  - Output will maintain its DC coupled, current-steering
  - TMDS compliance input can be AC coupled video or DC coupled
- 2.5Gbps data rate for TMDS clock up to 250MHz
- Support up to 36-bits per pixel Deep Color™ modes
- Programmable equalizer, emphasis and amplitude settings to achieve optimized HDMI signal integrity
- Integrated selectable DDC active/ passive switch to connect DDC path
- Idle clock detection function for output squelch
- Programmable TMDS termination control
  - TMDS input pull-up 50 Ohm termination, pull-down >120K Ohm resistor when switch is deselected
  - Double terminated TMDS output
- Integrated ESD protection on I/O pins to connector
  - 8KV contact per IEC61000-4-2, level 3
- Packaging
  - 64 pin LQFP (FB), Pb-free and Green

Description

PI3HDMI336 is an I²C configurable active switch using Pericom's new ActiveEye™ technology to achieve optimized signal integrity for cable or on board transmission.

Through I²C interface, system designer can easily program and adjust equalization, emphasis and output swing settings.

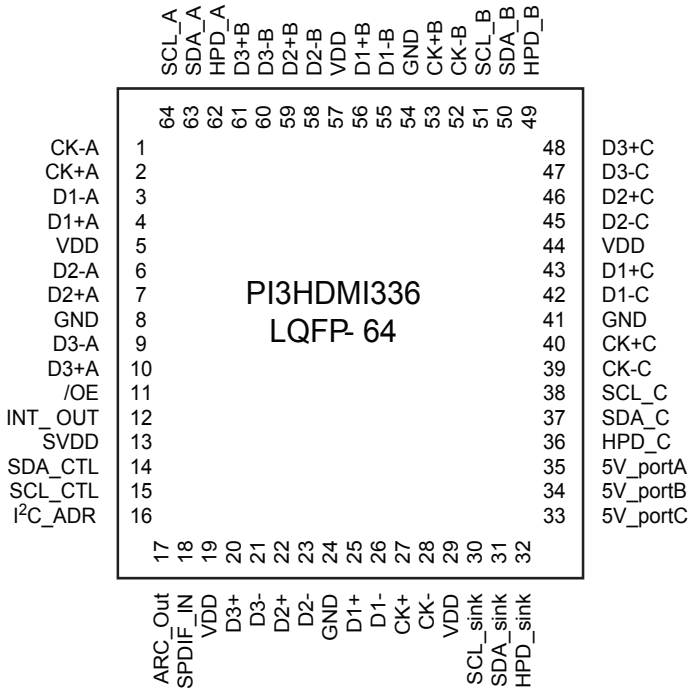
With integrated DDC channel Mux, Hot Plug Detection De-Mux, cable plug-unplug detection and HDMI 1.4 ARC transmitter, PI3HDMI336 saves GPIO control pins, provides optimized trace routing, and reduces BOM cost.

Programmable TMDS input termination settings helps designers to avoid the compatibility issue caused by non standard HDMI source.

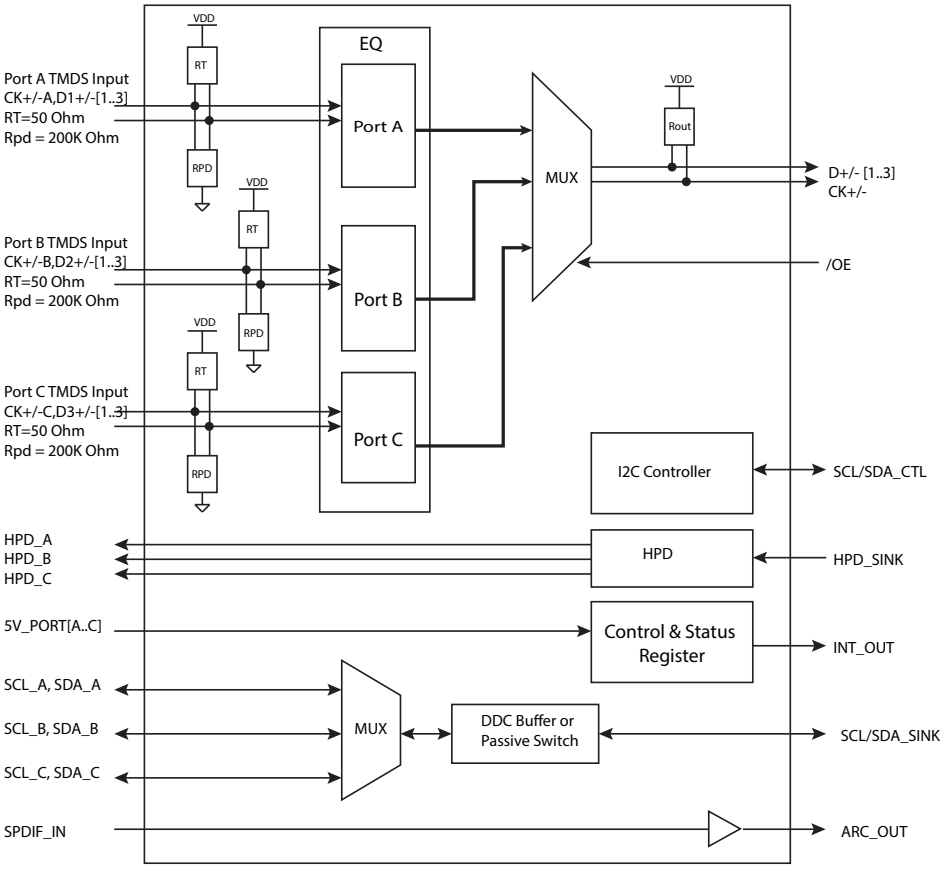
Programmable output termination setting supports double termination option between PI3HDMI336 and the HDMI receiver chip. This feature minimizes the reflection caused by improper impedance matching and reduces the signal jitter.

PI3HDMI336 is HDMI 1.4 compatible with backward compatibility to the DVI 1.0 standard and can be used for the DP++ application devices.

Block Diagram



Block Diagram



Pin Description

Pin #	Pin Name	IO	Descriptions
5, 19, 29, 44, 57	V_{DD}	Power	3.3V power supply. When V_{DD} is off, the TMDS channels and ARC will be powered down.
13	SV_{DD}	Power	3.3V standby power supply. SV_{DD} is for side band signals (HPD, DDC channel and the I²C control register unit).
8, 24, 41, 54	GND	Ground	Ground connection
32	HPD_SINK	I	Sink side hot plug detector input; internal pull-down at 120K Ω.
62	HPD_A	O	Port A HPD output
49	HPD_B	O	Port B HPD output
36	HPD_C	O	Port C HPD output
2	CK+A	I	Port A TMDS inputs. Rt=50ohm; Rpd=200kΩ.
1	CK-A		
4	D1+A		
3	D1-A		
7	D2+A		

Pin Description Cont..

Pin #	Pin Name	IO	Descriptions
6	D2-A	I	Port A TMDS inputs. Rt=50ohm; Rpd=200kΩ.
10	D3+A		
9	D3-A		
53	CK+B	I	Port B TMDS inputs. Rt=50ohm; Rpd=200kΩ.
52	CK-B		
56	D1+B		
55	D1-B		
59	D2+B		
58	D2-B		
61	D3+B		
60	D3-B		
40	CK+C	I	Port C TMDS inputs. Rt=50ohm; Rpd=200kΩ.
39	CK-C		
43	D1+C		
42	D1-C		
46	D2+C		
45	D2-C		
48	D3+C		
47	D3-C		
27	CK+	O	TMDS outputs. Rout=50Ω.
28	CK-		
25	D+1		
26	D-1		
22	D+2		
23	D-2		
20	D+3		
21	D-3		
64	SCL_A	IO	Port A DDC Clock
51	SCL_B	IO	Port B DDC Clock
38	SCL_C	IO	Port C DDC Clock
63	SDA_A	IO	Port A DDC Data
50	SDA_B	IO	Port B DDC Data
37	SDA_C	IO	Port C DDC Data

Pin Description Cont..

Pin#	Name	IO Type	Descriptions
30	SCL_SINK	IO	Sink side DDC Clock
31	SDA_SINK	IO	Sink side DDC Data
15	SCL_CTL	IO	I²C Clock, compatible with I²C-bus specification, up to 400kb/s.
14	SDA_CTL	IO	I²C Data, compatible with I²C-bus specification, up to 400kb/s.
12	INT_OUT	O	Interrupt pin. Logic status output pin of INT Flag. Open drain output, set INT_OUT to high by external pull to SV_{DD} resistor.
11	/OE	I	Output Enable control. Active low. /OE only disables the high speed TMDS channel but not the side band signals and I²C circuitry supplied by SV_{DD}. Internal pull-down at 100k ohm.
16	I²C_ADR	I	I²C Address LSB; internal pull-down at 100K Ω.
35, 34, 33	5V_PORTA, 5V_PORTB, 5V_PORTC	I	Connector 5V port. Internal pull down resistor at 100k when V_{DD} power on.
18	SPDIF_IN	I	Single mode ARC signal input. See page 11 in detail.
17	ARC_OUT	O	Single mode ARC signal output.

I²C Address Byte

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0 (R/W)
Address-Byte	1	0	1	0	1	0	I2C_ADR	1/0 *

I²C Control Register

Byte 0

Bit	Descriptions	Type	Power Up Condition	Logic Settings
7	HDMI input port selection	R/W	0	b[7:6] = 00 Port A b[7:6] = 01 Port B b[7:6] = 10 Port C b[7:6] = 11 no port active See Port Selection truth table
6	HDMI input port selection	R/W	0	
5	TMDS Output Enable	R/W	1	0 = Output Disable Disabled TMDS channel and enter standby mode. Side band signals and I²C circuitry are still alive. 1 = Output Enable See Output Enable control table

Bit	Descriptions	Type	Power Up Condition	Logic Settings
4	HPD Input Selection	R/W	0	0 = HPD_SINK 1 = I²C Register Setting from B0b[0:3] Under I2C register control mode, HPD[A:C] can be individually control by B0b[0:2] for HPD output.
3	HPD Output Stage selection	R/W	0	0 = Open Drain 1 = Output Buffer
2	HPD Port C Logic Setting	R/W	0	I. Byte0 b[4] = 1 When B0b[3] = 0 (open drain mode) B0b[2]=0, set HPD [C] to Low B0b[2]=1, set HPD [C] to High by external pull high resistor When B0b[3] = 1 (output buffer mode) B0b[2]=0, set HPD [C] to High B0b[2]=1, set HPD [C] to Low
	HPD Port B Logic Setting	R/W	0	I. Byte0 b[4] = 1 When B0b[3] = 0 (open drain mode) B0b[1]=0, set HPD [B] to Low B0b[1]=1, set HPD [B] to High by external pull high resistor When B0b[3] = 1 (output buffer mode) B0b[1]=0, set HPD [B] to High B0b[1]=1, set HPD [B] to Low
0	HPD Port A Logic Setting	R/W	0	I. Byte0 b[4] = 1 When B0b[3] = 0 (open drain mode) B0b[0]=0, set HPD [A] to Low B0b[0]=1, set HPD [A] to High by external pull high resistor When B0b[3] = 1 (output buffer mode) B0b[0]=0, set HPD [A] to High B0b[0]=1, set HPD [A] to Low

Byte 1

Bit	Descriptions	Type	Power Up Condition	Logic Settings
7	Port A RT , Rpd on/off control	R/W	1	0 = RT disconnected, Rpd connected 1 = RT connected, Rpd disconnected
6	Port B RT , Rpd on/off control	R/W	1	0 = RT disconnected, Rpd connected 1 = RT connected, Rpd disconnected
5	Port C RT , Rpd on/off control	R/W	1	0 = RT disconnected, Rpd connected 1 = RT connected, Rpd disconnected
4	5V_PortC connect	R	0	0 = Disconnected 1 = Connected INT Flag B1b[1] is set by 5V_PortC edge signal when 5V_PortC changes from 1 to 0, or from 0 to 1.
3	5V_PortB connect	R	0	0 = Disconnected 1 = Connected INT Flag B1b[1] is set by 5V_PortB edge signal when 5V_PortB changes from 1 to 0, or from 0 to 1.
2	5V_PortA connect	R	0	0 = Disconnected 1 = Connected INT Flag B1b[1] is set by 5V_PortA edge signal when 5V_PortA changes from 1 to 0, or from 0 to 1
1	INT Flag	R	0	0 = INT Flag Clear 1 = INT Flag Set INT Flag will be set from logic Low to High, when any 5V_Port has detected plug or unplug transition action. INT Flag is cleared to low after I²C bus reads the register byte 1. See INT Flag flowchart.
0	DDC channel selection	R/W	0	0 = Passive switch 1 = Active switch buffer For power saving operation, passive switch can be selected to further reduce the active power consumption.

Byte 2

Bit	Descriptions	Type	Power Up Condition	Logic Settings
7	TMDS AC swing for CML output setting	R/W	0	b[7:6] = 00 500mV *Note 1
6	TMDS AC swing for CML output setting	R/W	0	
5	TMDS output pull-up resistor Rout control	R/W	0	0 = Disconnect Rout pull-up to V_{DD}, open drain output 1 = Connect Rout pull-up to V_{DD} (3.3V), double termination output
4	Output squelch control	R/W	1	0 = Output squelch disable 1 = Output squelch enable *Note 2, 3
3	TMDS output pre-emphasis setting	R/W	0	See OCx truth table
2	TMDS output pre-emphasis setting	R/W	0	See OCx truth table
1	TMDS input equalization setting	R/W	1	See EQx truth table
0	TMDS input equalization setting	R/W	0	See EQx truth table

Note:

1. B2[7:6] : internal use only

2. Output squelch control is used to control TMDS D+/-[0:3], which are set to 'high impedance /or pull-up to V_{DD} by internal 50Ω resistor' when Output squelch is enable if there is no TMDS input signal. When squelch is disable, TMDS D+/-[0:3] will be unknown if there is no TMDS input signal.

3. squelch control is using CLK channel signal detection. When TMDS input clock frequency is low or swing is small, it will show no input signal.

Equalizer (EQx) Truth Table

TMDS data channel only. TMDS clock channels is 3db fixed

B2b[1]	B2b[0]	EQ value on TMDS data channels
0	0	3dB
0	1	6dB
1	0	12dB (default)
1	1	16dB

OCx truth table (Swing setting B2b[7:6]=00, 500mv as default)

TMDS output pre-emphasis setting			Setting Value		Note
B2b[5]	B2b[3]	B2b[2]	Single-end Vswing (mV)	Pre-emphasis (dB)	Default Setting
0	0	0	500	0	Open drain
0	0	1	500	1.5	Open drain
0	1	0	500	2.5	Open drain
0	1	1	500	3.5	Open drain
1	0	0	500	0	Double termination
1	0	1	500	1.5	Double termination
1	1	0	500	2.5	Double termination
1	1	1	500	3.5	Double termination

Port selection truth table

B0b[7]	B0b[6]	TMDS port	DDC port
0	0	CK+/-A, D1+/-A,D2+/-A,D3+/-A	SCL_A/SDA_A
0	1	CK+/-B, D1+/-B,D2+/-B,D3+/-B	SCL_B/SDA_B
1	0	CK+/-C, D1+/-C,D2+/-C,D3+/-C	SCL_C/SDA_C
1	1	No port active	No port active

Data Channel TMDS input termination resistor RT, Rpd Control

Pull-down resistor Rpd active conditions:

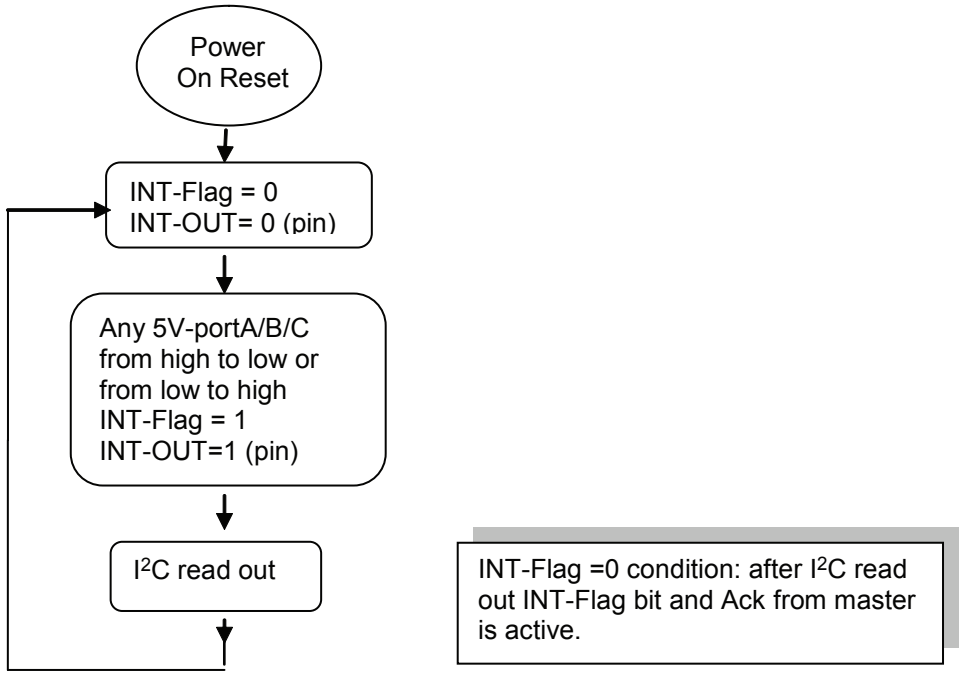
1. The Data Channel RT is disconnected controlled by Byte 1 bit[7:5]
2. Output enable control /OE is disable(/OE=High), pull down all channels
3. No normal operation voltage input (but standby voltage SV_{DD} is still On), pull down all channels

Output Enable Control

/OE	I2C B0b[5]	Operation
Low	High	Output Enable
X	Low	Output Disable
High	X	Output Disable

Note: Output disable condition: TMDS channel shut down, output high impedance.

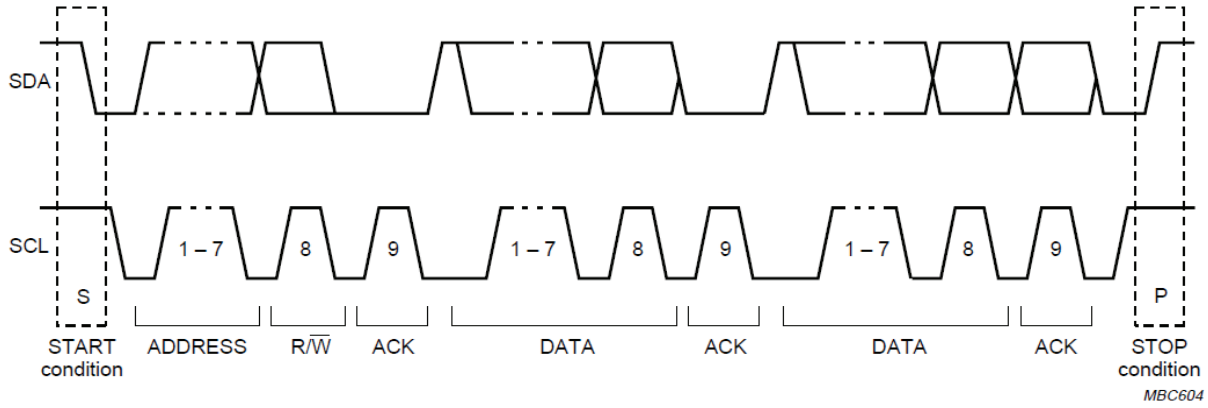
INT-Flag flowchart



I²C Bus transactions

Data transfers follow the format shown in Fig.1. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

Figure 1: A complete data transfer



Data is transmitted to the PI3HDMI336 registers using the Write mode as shown in Figure 2. Data is read from the PI3HDMI336 registers using the Read mode as shown in Figure 3

Figure 2 : Write to Control Register

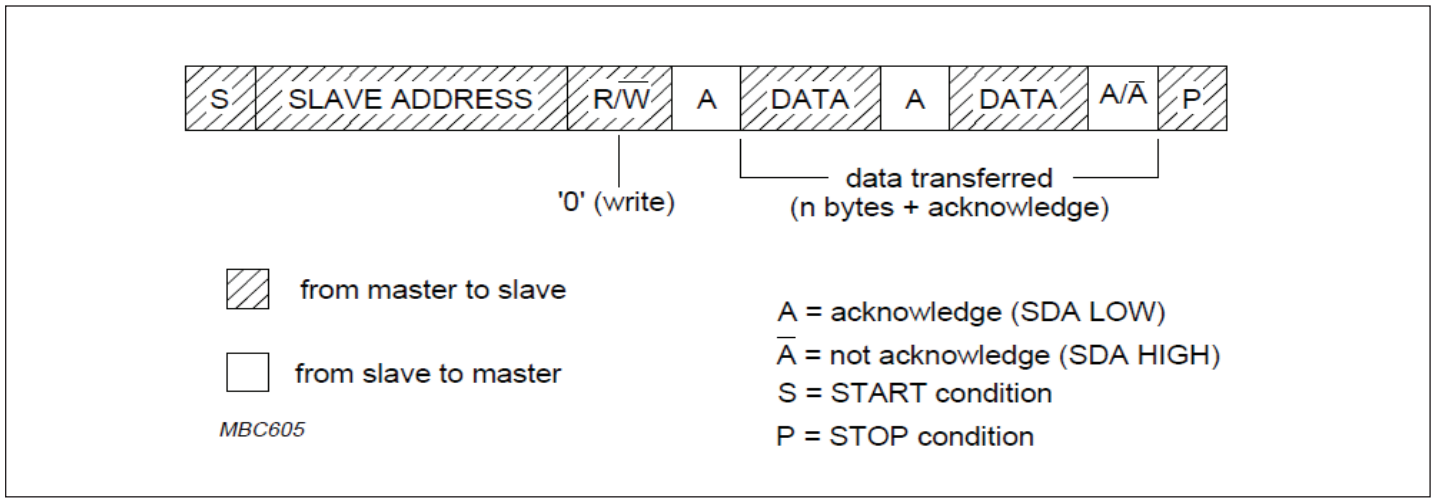
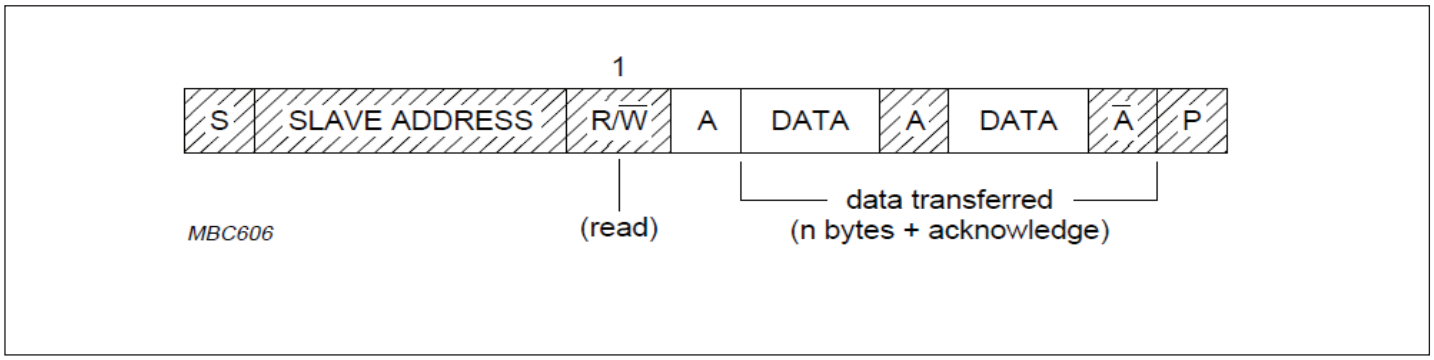


Figure 3 : Read from Control Register



Audio Return channel

There are two ARC input modes. They're 'Common mode input' and 'single mode input' but HDMI336 supports 'single mode input' only.

Figure 1: ARC single mode input and output

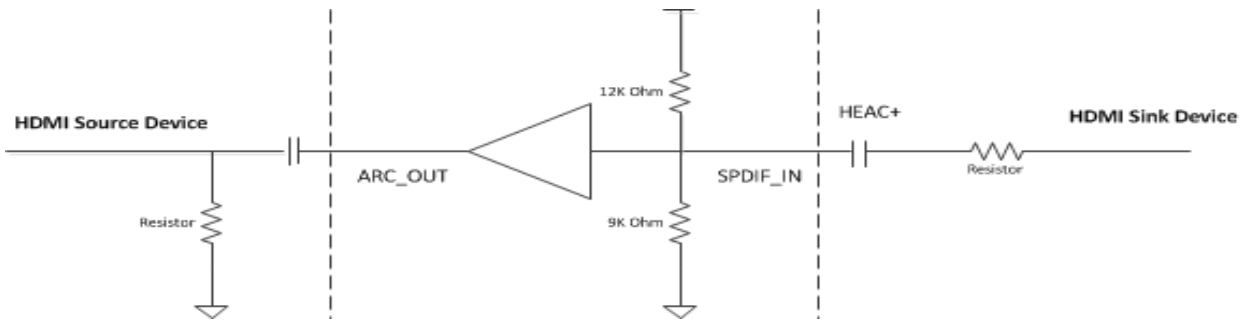
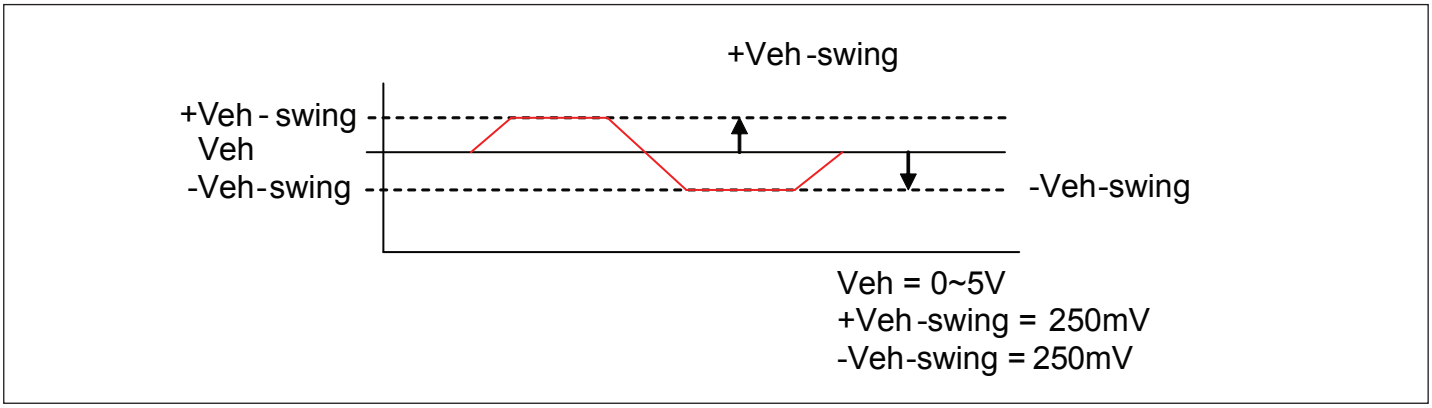
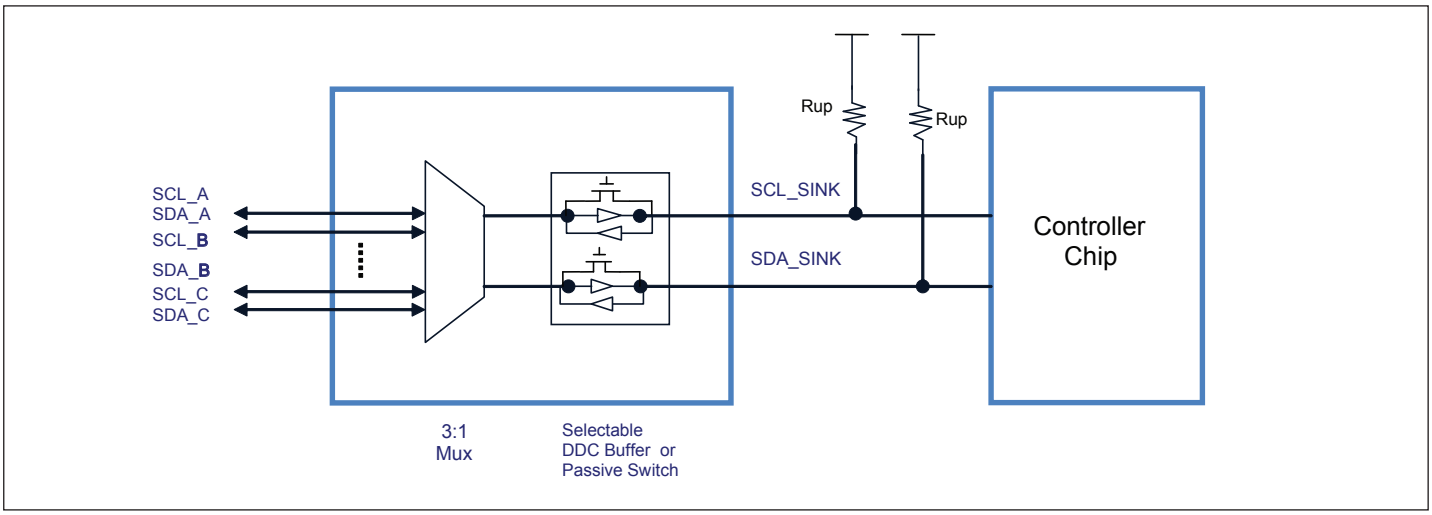
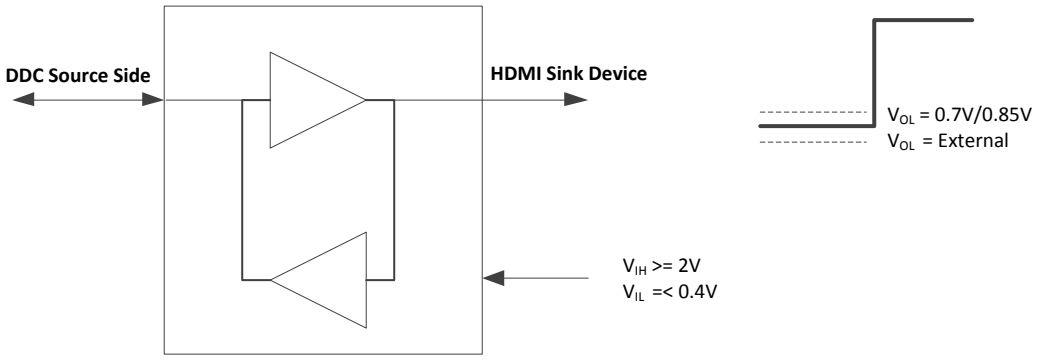


Figure 2: ARC single mode signal output waveform



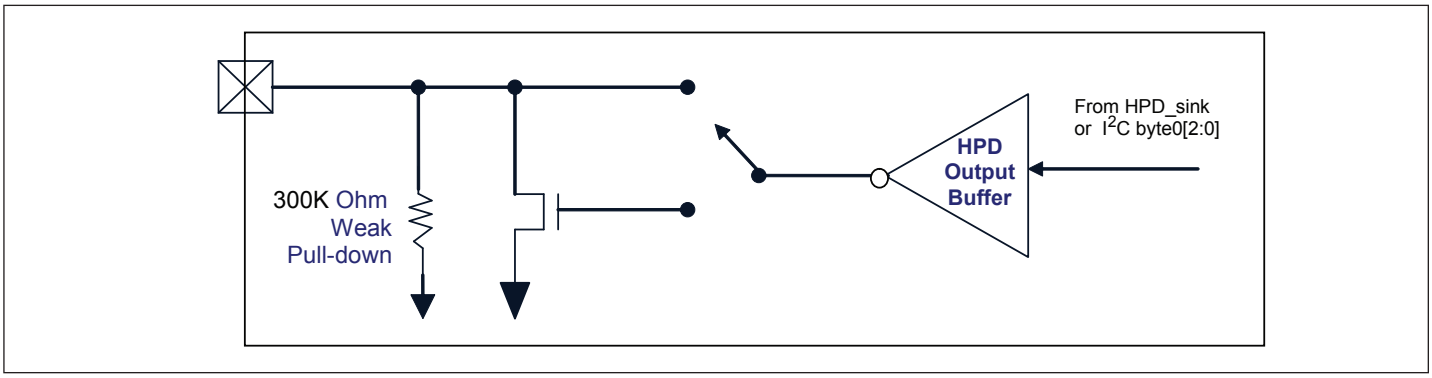
DDC Channel Application Diagram





I2C block uses "low V_{IL} <= 0.4V and 0.7V <= 0.85V" to define the signal direction, exit from system lock

HPD[A:C] Output Diagram



Note:

1. HPD output block support by SV_{DD} power.
2. During normal or standby mode, the HPD block is active. HPD signal output is programmed by the control register.
3. Open drain buffer is recommended with a 1Kohm pull-up resistor to 5V. If HPD output buffer is selected, external buffer transistor is required to avoid 5V to 3.3V leakage.

HPD[A:C] truth table:

B0b[4]=0, HPD_Sink input; B0b[3]=0, HPDx open drain output

Port selection	HPD input select B0b[4]=0	HPD output select B0b[3]=0	HPDA	HPDB	HPDC
Port A	HPD_Sink	Open drain	HPD_Sink	L	L
Port B	HPD_Sink	Open drain	L	HPD_sink	L
Port C	HPD_Sink	Open drain	L	L	HPD_sink
No port active	HPD_Sink	Open drain	L	L	L

B0b[4]=0, HPD_Sink input; B0b[3]=1, HPDx inverter output

Port selection	HPD input select B0b[4]=0	HPD output select B0b[3]=1	HPDA	HPDB	HPDC
Port A	HPD_Sink	Buffer	/HPD_Sink	H	H
Port B	HPD_Sink	Buffer	H	/HPD_sink	H
Port C	HPD_Sink	Buffer	H	H	/HPD_sink
No port active	HPD_Sink	Open drain	H	H	H

B0b[4]=1, I²C register input; B0b[3]=0, HPDx open drain output

Port selection	HPD input select B0b[4]=1	HPD output select B0b[3]=0	HPDA	HPDB	HPDC
B0b[3]=0	HPDA	HPDB	HPDC		
Port [A:C]	B0b[2:0]	Open drain	B0b[0]	B0b[1]	B0b[2]
No port active	B0b[2:0]	Open drain	B0b[0]	B0b[1]	B0b[2]

B0b[4]=1, I2C register input; B0b[3]=1, HPDx inverter output

Port selection	HPD input select B0b[4]=1	HPD output select B0b[3]=1	HPDA	HPDB	HPDC
Port [A:C]	B0b[2:0]	Buffer	/B0b[0]	/B0b[1]	/B0b[2]
No port active	B0b[2:0]	Buffer	/B0b[0]	/B0b[1]	/B0b[2]

Absolute Maximum Ratings

Supply Voltage to Ground Potential 5.5V
All Inputs and Outputs .....-0.5V to V_{DD}+0.5V
Ambient Operating Temperature .....-20 to +85°C
Storage Temperature .....-65 to +150°C
Junction Temperature .....150°C
Soldering Temperature .....260°C

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-20		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Specification

V_{DD} = 3.3V ±10%,

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
I_{DD}	V_{DD} Supply Current	Output Enable (open drain 500mv signal-end 0dB pre-emphasis)		80	92	mA
		Output Enable (double termination, 500mv signal-end 0dB pre-emphasis)		170	210	mA
I_{DDQ}	V_{DD} Quiescent Supply Current	TMDS Output Disable, ARC_OUT=0		3		mA
Istb	Standby mode	V_{DD}=0V, SV_{DD}=3.6V, DDC passive switch, HPD_x=0		1		mA
V_{IH}_5V_A, V_{IH}_5V_B, V_{IH}_5V_C	Input High Voltage of 5V ports		0.7*SV_{DD}			V
V_{IL}_5V_A, V_{IL}_5V_B, V_{IL}_5V_C	Input Low Voltage of 5V ports				0.3*SV_{DD}	V

DC Specification Cont..

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OL_HPD}	Buffer Output Low Voltage	I_{OL} = 4 mA			0.4	V
	Open Drain Output Low Voltage	I_{OL} = 4 mA	0		0.4	V
V_{OH_HPD}	Buffer Output High Voltage	I_{OH} = 1 mA	SV_{DD}-1.1			V
I_{OFF_HPD}	Off leakage current	V_{DD}=0, SV_{DD}=0, V_{IN}=3.6V			10	uA
		V_{DD}=0, SV_{DD}=0, V_{IN}=5.5V			20	
I_{OZ_HPD}	Open drain Output leakage current	S_{VDD}=3.6, V_{IN}=3.6V			25	
		S_{VDD}=3.6, V_{IN}=5.5V			35	
HPD_sink						
I_{IH}	High level digital input current	V_{IH} =V_{DD}	-10		40	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-10		10	µA
V_{IH}	High level digital input voltage	SV_{DD}=3.3v	2.0			V
V_{IL}	Low level digital input voltage		0		0.8	V
Control pin (/OE)						
I_{IH}	High level digital input current	V_{IH} =V_{DD}	-10		40	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-10		10	µA
V_{IH}	High level digital input voltage		2.0			V
V_{IL}	Low level digital input voltage		0		0.8	V
INT_OUT						
$V_{OL\_INT\_OUT}$	Output open drain Low Voltage	I_{OL} = 4 mA			0.4	V
$V_{OH\_INT\_OUT}$	High impedance, depended on external pull high resistor and power supplier	External pull-up Rup to V_{DD} from 1.5kΩ to 5kΩ	V_{DD}-1			V
$I_{OFF\_INT\_OUT}$	Off leakage current	V_{DD}=0, SV_{DD}=0, V_{IN}=3.6V			10	uA
		V_{DD}=0, SV_{DD}=0, V_{IN}=5.5V			20	

DDC Channel Block						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$V_{IH\_DDC(source)}$	Source Side DDC Buffer Input High Voltage		0.7*SV_{DD}			V
$V_{IL\_DDC(source)}$	Source Side DDC Buffer Input Low Voltage				0.3*SV_{DD}	V
$V_{OL\_DDC(source)}$	Source Side DDC Buffer Output Low Voltage,	External pull-up Rup to V_{DD} from 1.5kΩ to 5kΩ			0.4	V
$V_{OL\_DDC(sink)}$	Sink Side DDC Buffer Output Low Voltage,	External pull-up Rup to V_{DD} from 1.5kΩ to 5kΩ	0.7		0.85	V
$V_{IH\_DDC(sink)}$	Sink Side DDC Buffer Input High Voltage,		2.0			V
$V_{IL\_DDC(sink)}$	Sink Side DDC Buffer Input Low Voltage,				0.4	V
I_{LK}	Input leakage current	DDC switch is off	-10		10	uA
C_{IO}	Input/Output capacitance when passive switch on	VI peak-peak = 1V, 100 KHz		10.5		pF
R_{ON}	Passive Switch resistance	IO = 3mA, V_O = 0.4V		30	50	Ω
Vpass	Switch Output voltage	V_I=3.3V, II=100uA SV_{DD}=3.3V	1.5	2.0	2.8	V
CI(source)	Source side DDC capacitance When active switch on or passive switch off.	V_I peak-peak = 1V, 100 KHz		4.0		pF
CI(sink)	Sink side DDC capacitance when active switch on or passive switch off.	V_I peak-peak = 1V, 100 KHz		6.0		pF
V_{OH_DDC} (source/sink)	DDC Switch Output High Voltage	V_{IN}=3.3V. External pull-up Rup to V_{DD} from 1.5kΩ to 5kΩ	V_{DD} - 1			V

AC Characteristics (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
TMDS Differential Pins						
t_{pd}	Propagation delay	V_{DD} = 3.3V, Rout = 50Ω			2000	ps
t_r	Differential output signal rise time (20% - 80%)			150		
t_f	Differential output signal fall time (20% - 80%)			150		
$t_{sk(p)}$	Pulse skew			10	50	
$t_{sk(D)}$	Intra-pair differential skew			23	50	
$t_{sk}(o)$	Inter-pair differential skew(2)				100	
$t_{jit}(pp)$	Peak-to-peak output jitter CLK residual jitter	Data Input = 1.65 Gbps HDMI data pattern CLK Input = 165 MHz clock		15	30	ps
$t_{jit}(pp)$	Peak-to-peak output jitter DATA Residual Jitter			18	50	ps
t_{SX}	Select to switch output				10	ns
t_{en}	Enable time				600	ns
t_{dis}	Disable time				10	ns
DDC I/O Pins (SCL, SCL_SINK, SDA, SDA_SINK)						
t_{pd}	Propagation delay from SCLn to SCL_SINK or SDAn to SDA_SINK or SDA_SINK to SDAni in passive or active SW.	C_L = 10pF, in passive switch		1.5	2.5	ns
		C_L = 10pF, in active switch, SVDD=3.3v, Rup=2k		7.5		
DDC I/O Pins (HPD_SINK, HPD inverter output) *Note 1						
t_{pd}(HPD)	Propagation delay (from HPD_SINK to the active port of HPD)	C_L = 10pF		2	6.0	ns
t_{sx}(HPD)	Switch time (from port select to the latest)			3	6.5	

Note:

1. t_{plh} time of HPD open drain output, depends on external pull high resistor and load capacitor.

TMDS differential pins						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
V_{OH}	Single-ended high level output voltage	V_{DD} = 3.3V, Rout=50Ω	V_{DD}+10		V_{DD}-10	mV
V_{OL}	Single-ended low level output voltage		V_{DD}-600		V_{DD}–400	mV
Vswing	Single-ended output swing voltage		400		600	mV
$V_{OD(O)}$	Overshoot of output differential voltage				180 [1]	mV
$V_{OD(U)}$	Undershoot of output differential voltage				200 [2]	mV
$V_{OC(SS)}$	Change in steady-state common- mode output voltage between logic states				5	mV
I_{OS}	Short Circuit output current		-12		12	mA
	Short Circuit output current at double termination mode		-24		24	mA
VI(open)	Single-ended input voltage under high impedance input or open input	I_I = 10uA	V_{DD}-10		V_{DD}+10	mV
R_T	Input termination resistance	V_{IN} = 2.9V	45	50	55	Ohm
I_{OZ}	Leakage current with Hi-Z I/O	V_{DD} = 3.6V, SV_{DD} = 3.6V			10	µA

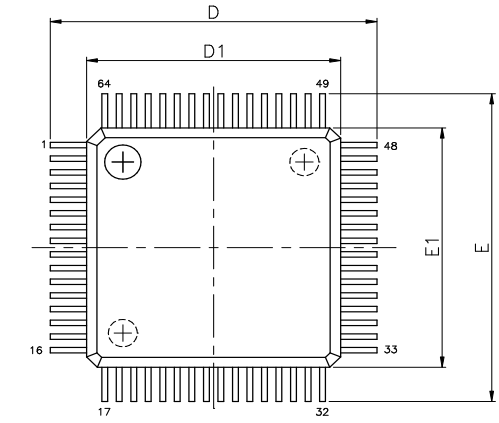
Note:

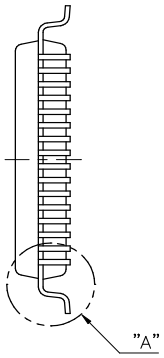
1. Overshoot of output differential voltage $V_{OD}(O)$ = (VSWING(MAX) * 2) * 15%,

2. Undershoot of output differential voltage $V_{OD}(O)$ = (VSWING(MIN) * 2) * 25%

SPDIF & ARC Pins, See ARC single mode waveform						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
I_{IH}_SPDIF	High level input current	V_{DD}=3.6V, V_{IH} =3.6V		500		uA
I_{IL}_SPDIF	Low level input current	V_{DD}=3.6V, V_{IL} = GND		350		uA
Vel	Single mode input/output Vel DC voltage level		0		5.0	V
Vel swing SPDIF	Single mode input swing		0.2		0.6	V
Vel swing ARC_ OUT	Single mode ARC output swing		0.4	0.5	0.6	V
Ro	Output resistance of ARC output stage			55		Ohm
t_r	ARC output rise time (10% to 90%)	< 0.4UI (f_{clock} = 6.144MHz) **			25	ns
tf	ARC output fall time (10% to 90%)	< 0.4UI (f_{clock} = 6.144MHz) **			25	ns
TJpp	ARC signal peak to peak jitter	< 0.05UI (f_{clock} = 6.144MHz)			3	ns

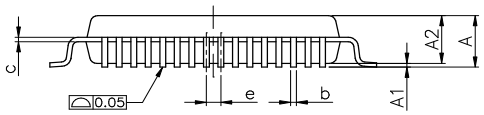
Packaging Mechanical: 64-Pin LQFP (FB)

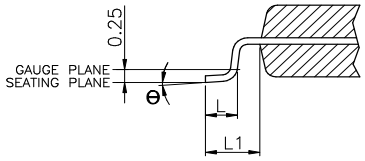




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D		9.00 BSC	
D1		7.00 BSC	
e		0.40 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°





DETAIL "A"

Notes:

1. JEDEC OUTLINE: MS-026 BBD
2. Dimensions D1 and E1 Do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm.

PERICOM Enabling Serial Connectivity

DATE: 05/18/11

DESCRIPTION: 64-contact, Low Profile Quad Flat Package (LQFP)

PACKAGE CODE: FB (FB64)

DOCUMENT CONTROL #: PD-2099 **REVISION: --**

11-0064

Related Products

Part Number	Product Description
PI3HDMI1201	DisplayPort 1.2 Re-driver with built-in AUX listener
PI3VDP1430	Dual Mode DisplayPort to HDMI Level Shifter and Re-driver
PI3HDMI511	3.4G HDMI1.4 Re-driver for Source-side application, supporting Dual Mode DisplayPort
PI3HDMI611	3.4G HDMI1.4 Re-driver for Sink-side application, supporting Dual Mode DisplayPort
PI3VDP3212	2-Lane DisplayPort1.2 Compliant Switch
PI3VDP12412	4-Lane DisplayPort1.2 Compliant Switch
PI3HDMI412AD	1:2 Active 3.4Gbps HDMI1.4 compliant Splitter/Re-driver
PI3HDMI521	2:1 3.4Gbps HDMI1.4 Switch/Re-driver with built-in ARC and Fast Switching support for Sink Application
PI3HDMI621	2:1 3.4Gbps HDMI1.4 Switch/Re-driver with built-in ARC and Fast Switching support for Sink Application
PI3HDMI336	3:1 Active 3.4Gbps HDMI Switch/Re-driver with I²C control and ARC Transmitter

Reference Information

Document	Description
VESA	VESA DisplayPort Standard Version 1 Revision 2, Video Electronics Standards Association, January 5, 2010 VESA DisplayPort Dual-Mode Standard Version 1, Video Electronics Standards Association, February 10, 2012 VESA DisplayPort Interoperability Guideline Version 1.1a, Video Electronics Standards Association, February 5, 2009
HDMI	High-Definition Multimedia Interface Specification Version 1.4, HDMI Licensing, LLC, June 5, 2009

Ordering Information

Ordering Code	Package Code	Package Type
PI3HDMI336FBE	FB	Pb-free & Green, 64-pin LQFP

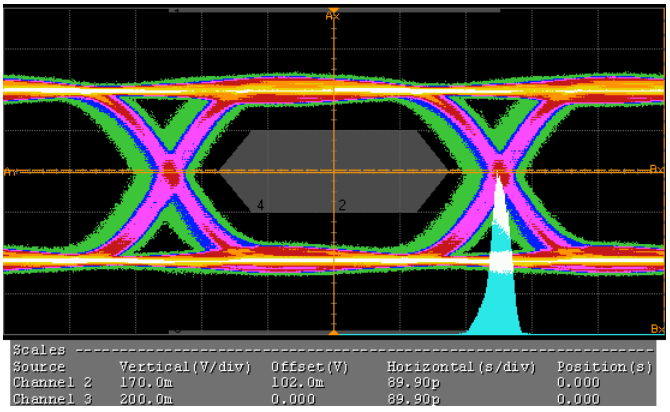
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

Revision History

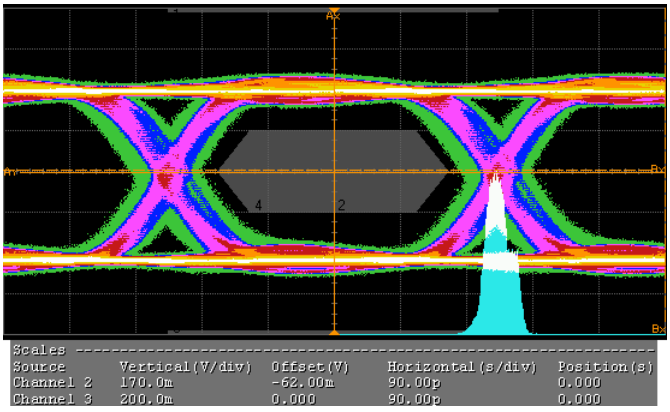
Date	Changes
7/28/2012	Block diagram, Reference Schematic

Appendix: Eye Diagram at 1920x1080p

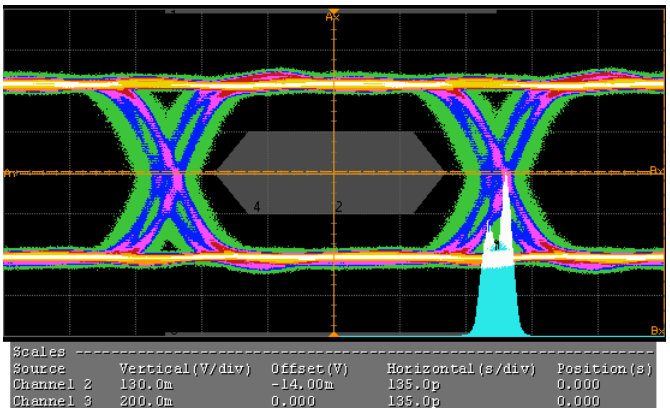
Input: Quantum Data + HDMI Cable
DUT Setting: Selected Port = Port C; HPD = Open Drain; TMDS = Open Drain/CML, RT connected, 500mV, 0dB Pre-emphasis
Output: HDMI-SMA Test Fixture + Agilent 54855A DSO



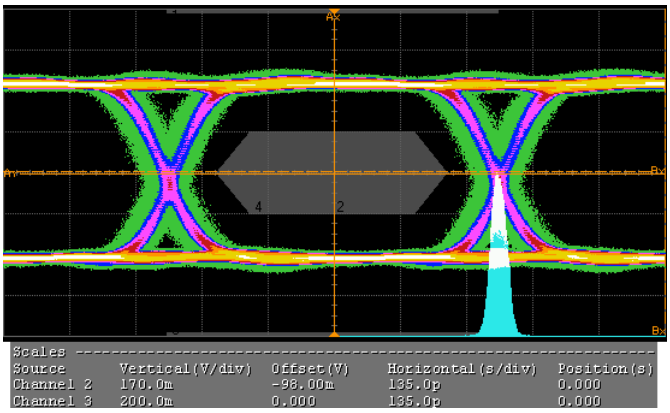
D1 Eye at 1920x1080p 12bit, 12dB EQ, 2m Cable, Open Drain



D1 Eye at 1920x1080p 12bit, 12dB EQ, 10m Cable, Open Drain

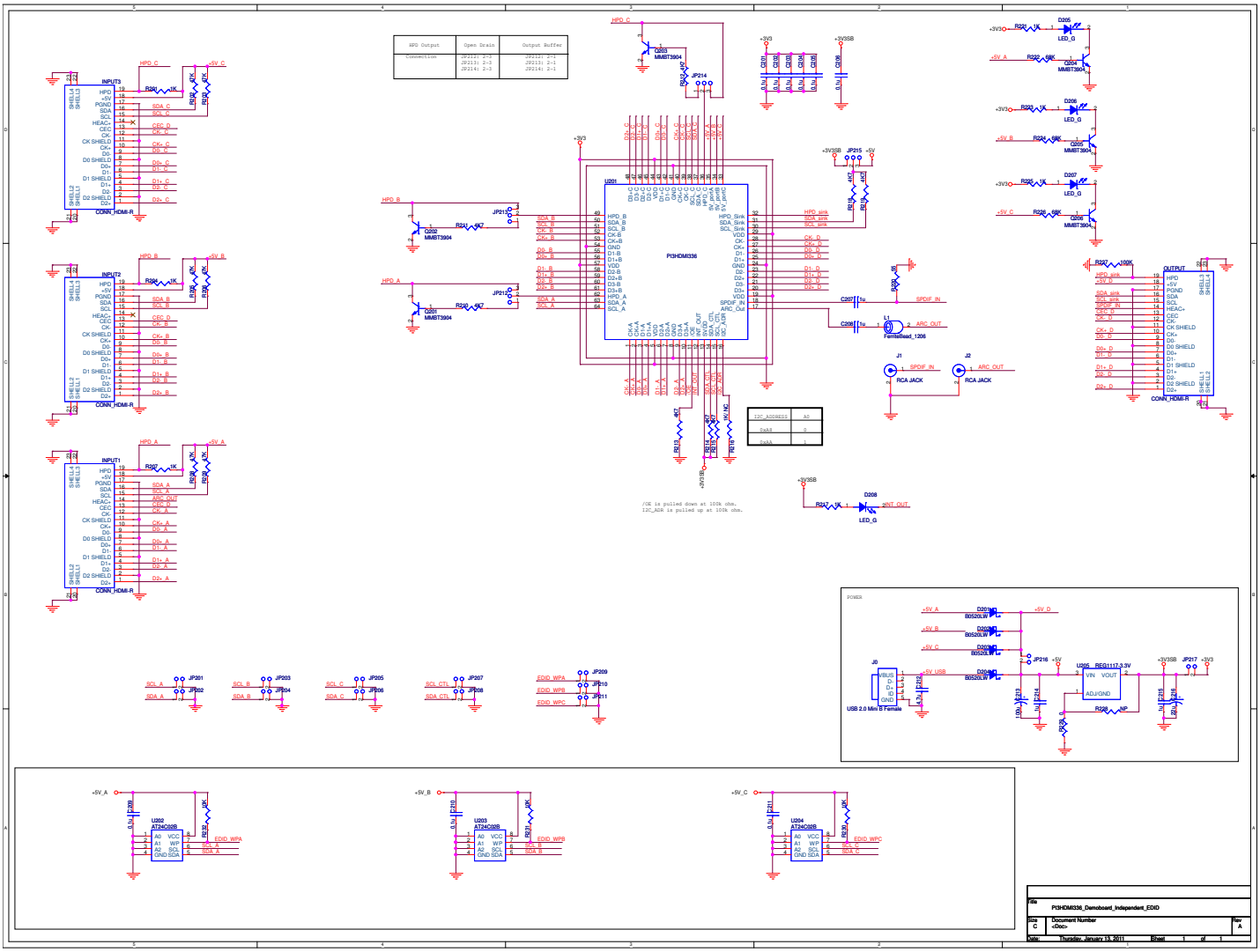


D1 Eye at 1920x1080p 8bit, 12dB EQ, 20m Cable, Open Drain



D1 Eye at 1920x1080p 8bit, 16dB EQ, 30m Cable, Open Drain

Appendix: Reference Schematic



Appendix: Evaluation Board Image