

File: dacon.sch
Sheet: /dacony

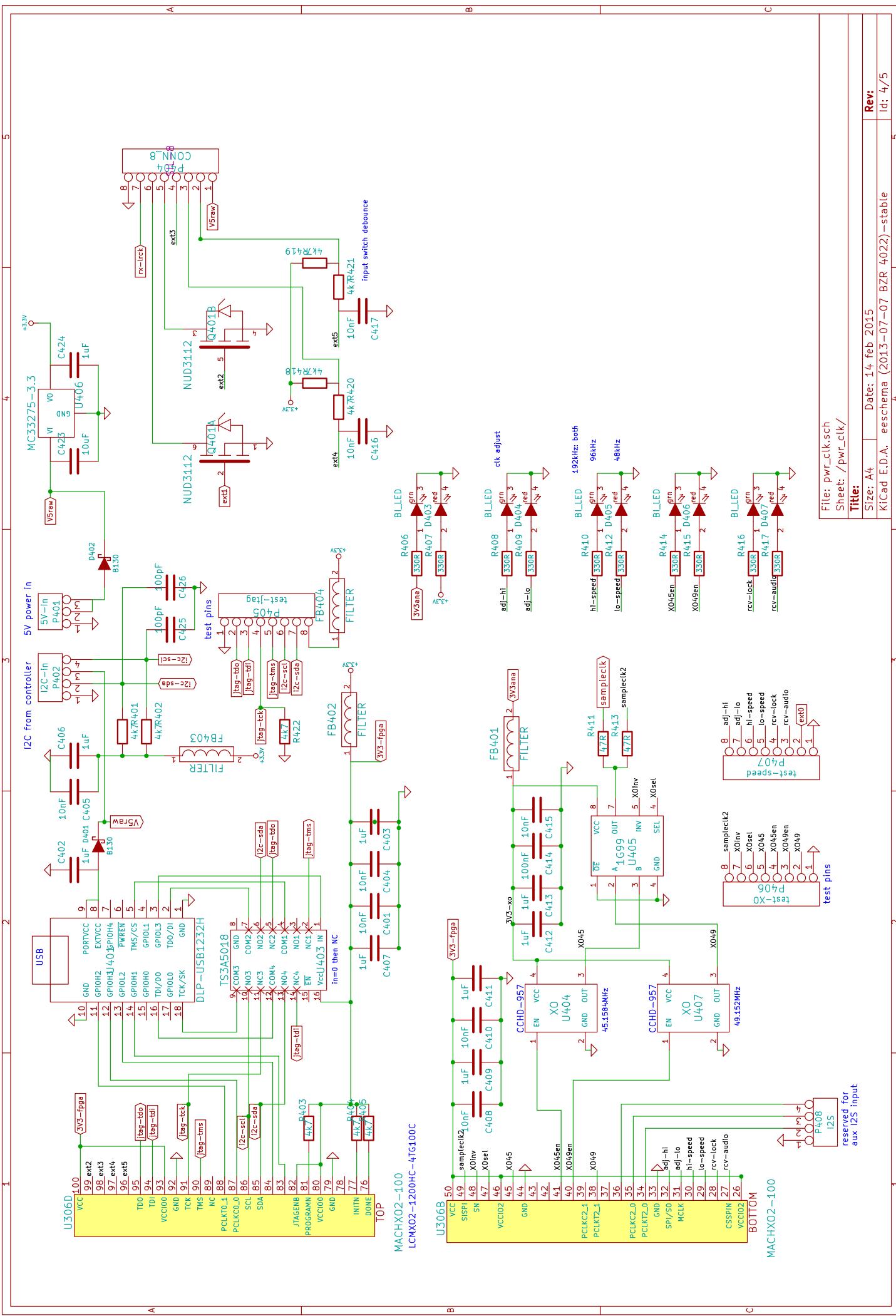
Title:

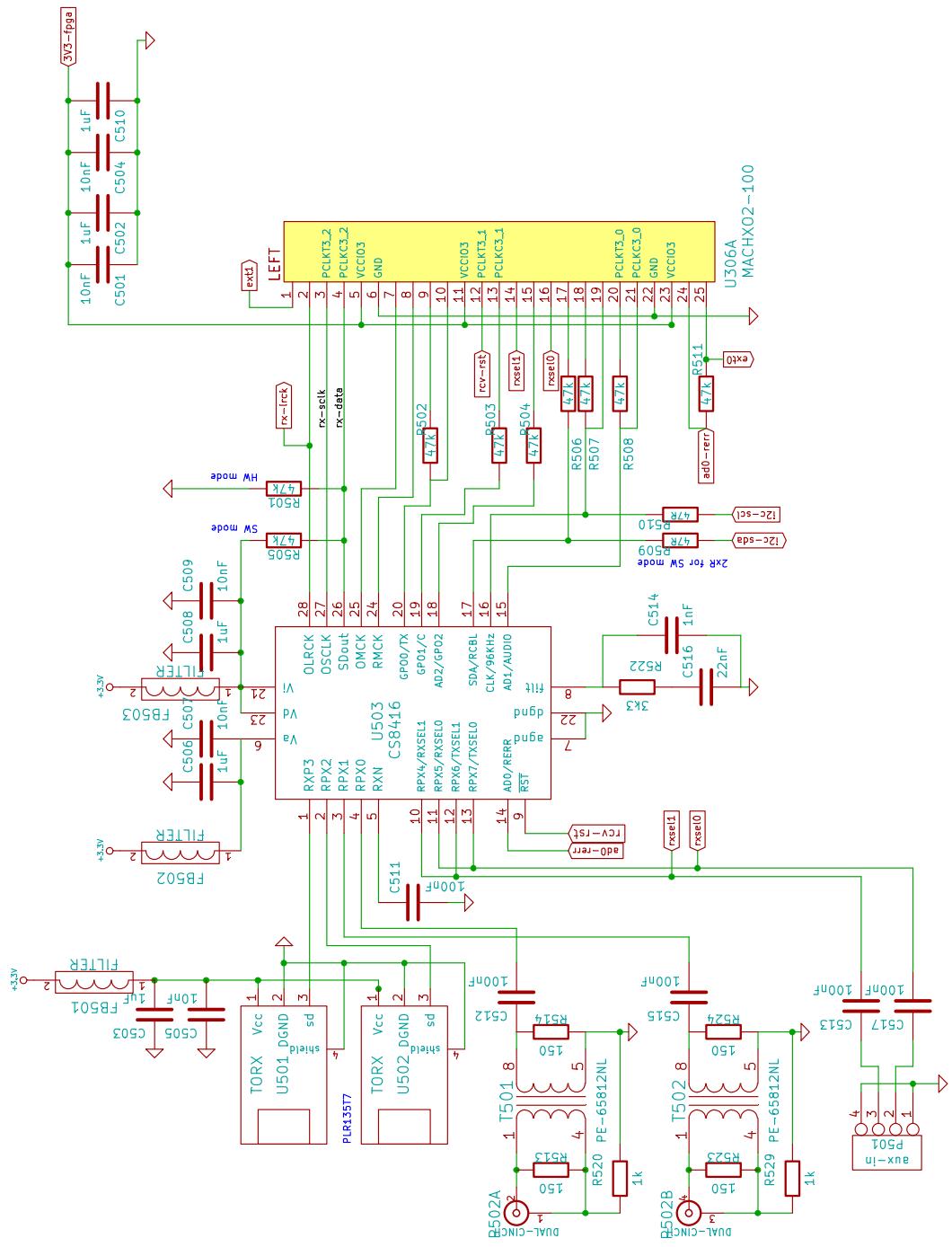
Size: A4 Date: 14 feb 2015

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12S format: MSB first, tick low means left audio, 2x32 bit/s in a wck period.
wck and data change at falling edge of bitck, are sampled at rising edge of bitck.
MSB bit transferred at 2nd rising edge of bitck after wck transient.





P4[28] and P4[29] are still avail for UART3 TXD and RXD,
are connected to daughterboard pins PD15 and PD16.
(Maybe some UART should be routed to mainboard IO in next rev.)

File: recvr.sch
Sheet: /recvr/
Title:

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Rev: 4 Id: 5/5