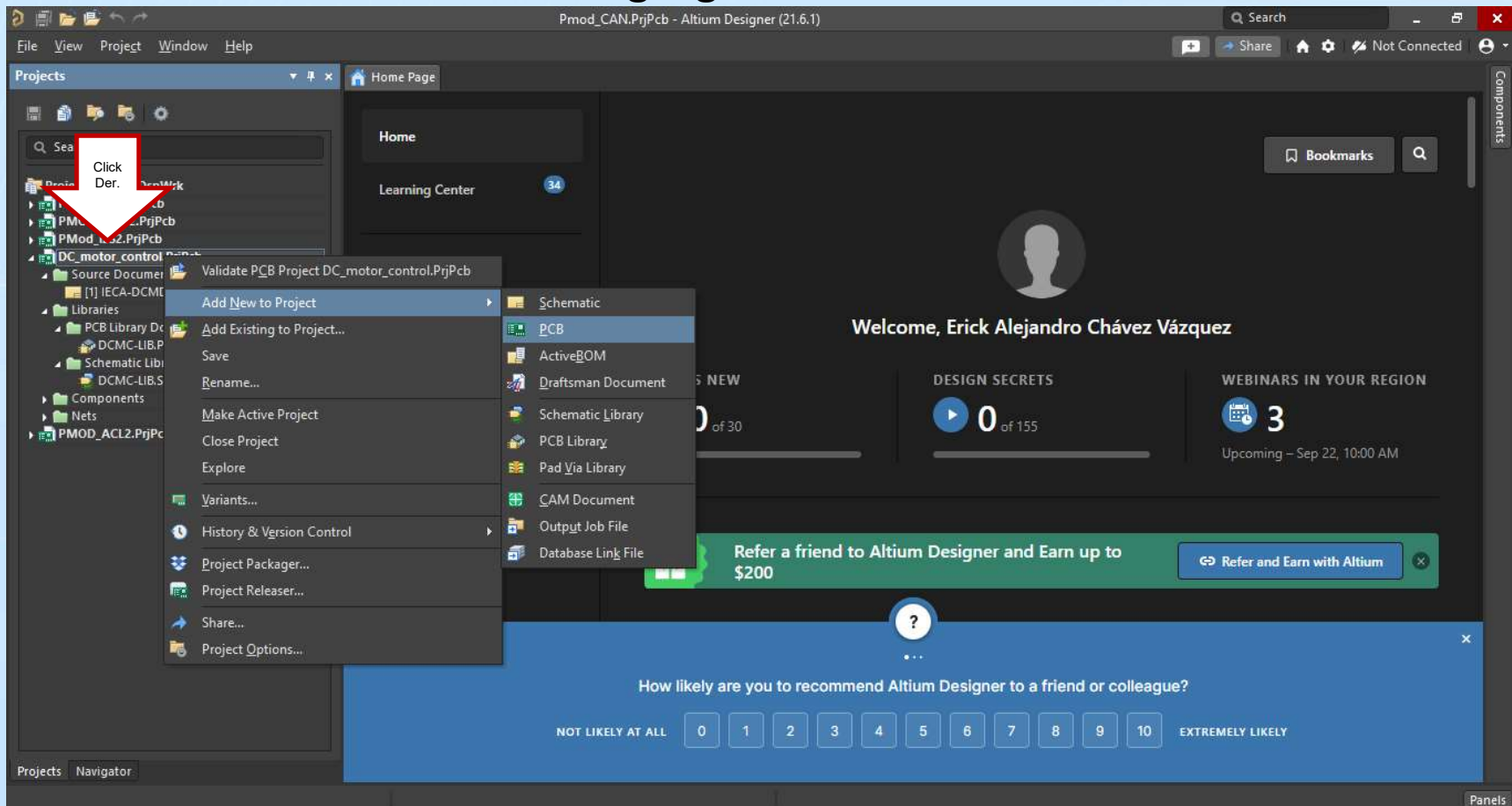


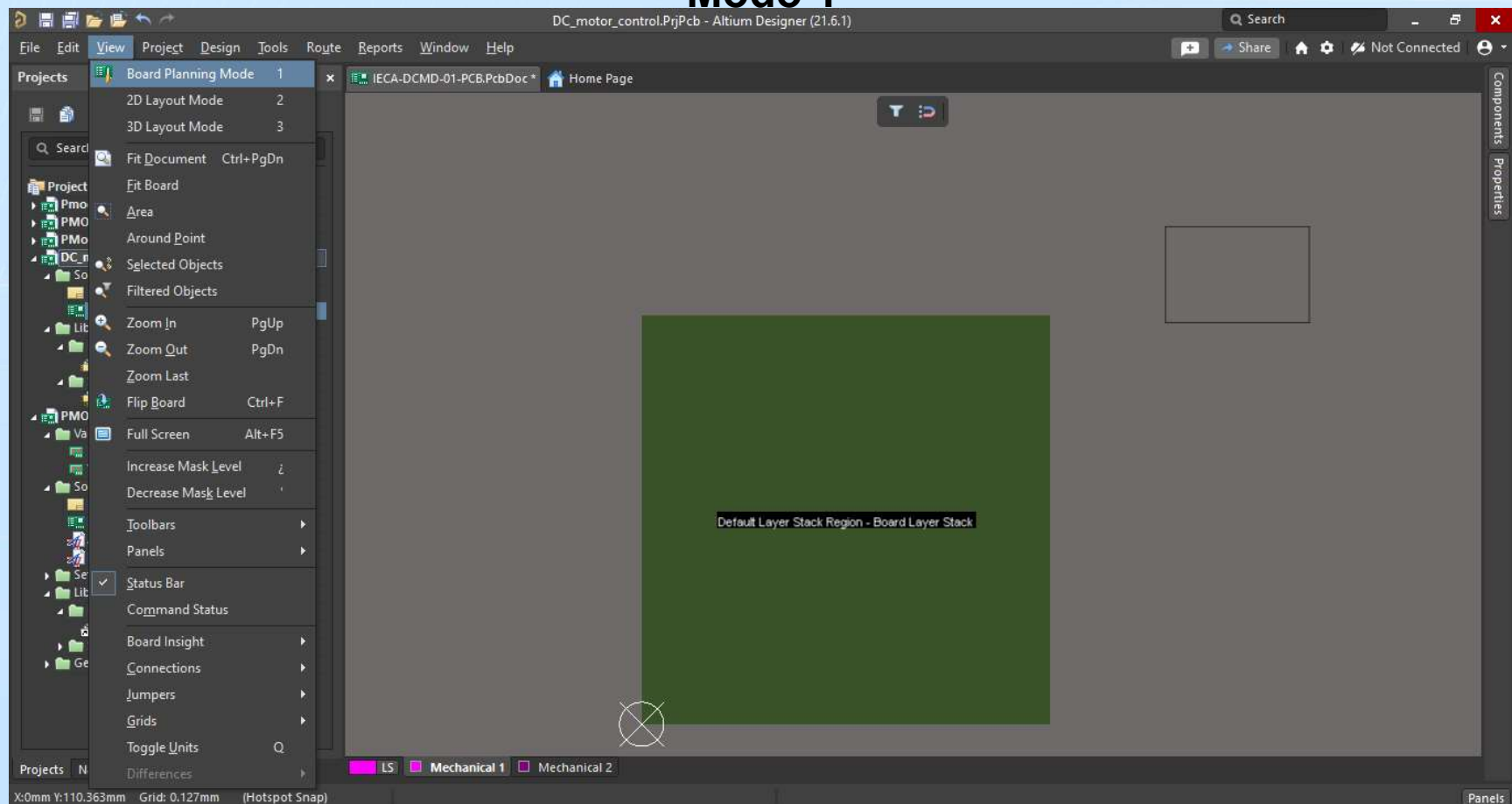
## Agregar un PCB



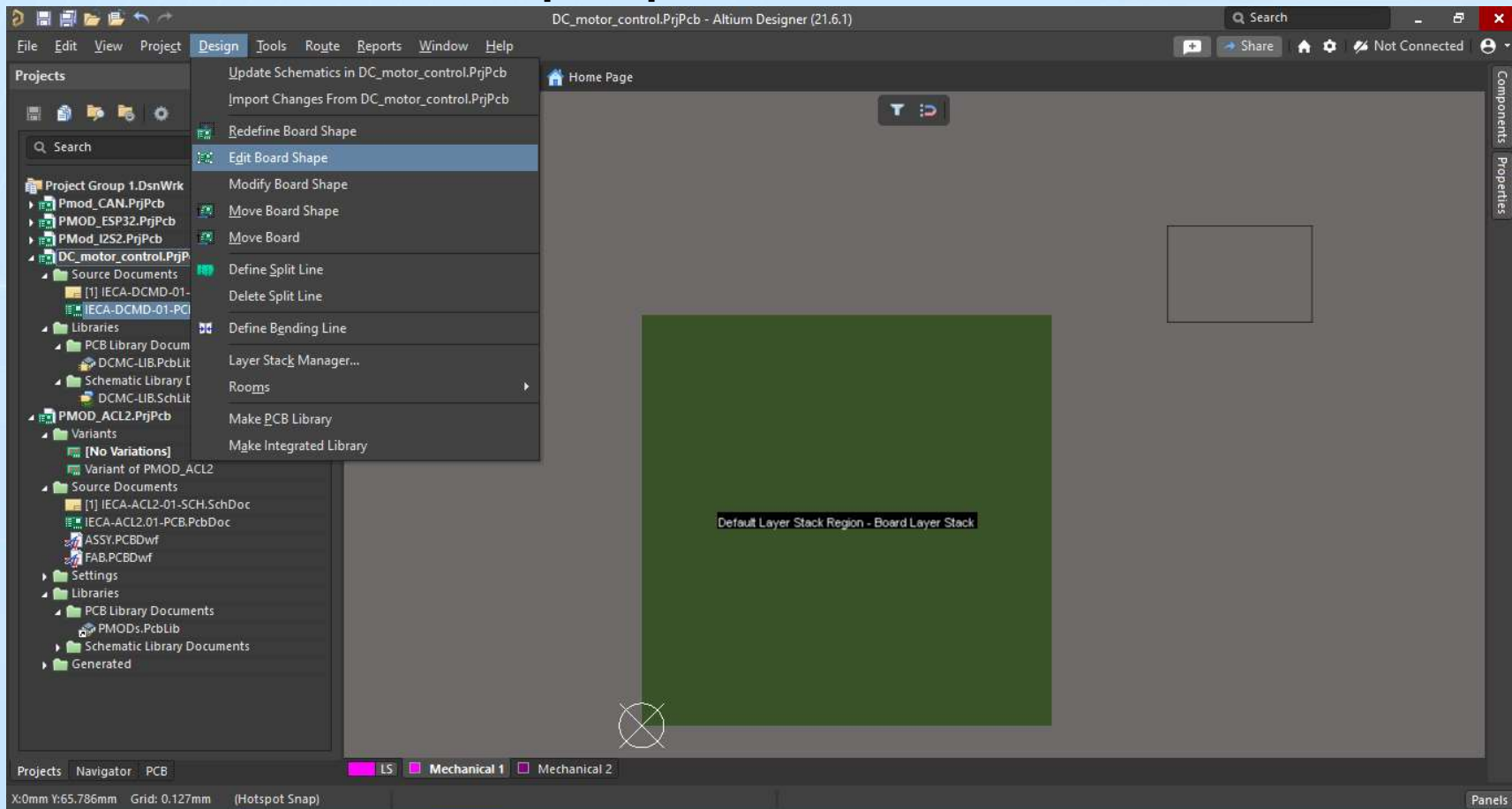
The screenshot displays the Altium Designer 21.6.1 software interface. The title bar indicates the project is 'Pmod\_CAN.PrjPcb'. The 'Projects' panel on the left shows a tree view of the project structure, including folders for 'Source Documents', 'Libraries', 'Components', 'Nets', and 'PMOD\_ACL2.PrjPcb'. A red arrow points to the 'Add New to Project' option in the context menu, with the text 'Click Der.' next to it. The context menu is open, showing options like 'Add New to Project', 'Add Existing to Project...', 'Save', 'Rename...', 'Make Active Project', 'Close Project', 'Explore', 'Variants...', 'History & Version Control', 'Project Packager...', 'Project Releaser...', 'Share...', and 'Project Options...'. The 'Add New to Project' sub-menu is also visible, listing options such as 'Schematic', 'PCB', 'ActiveBOM', 'Draftsman Document', 'Schematic Library', 'PCB Library', 'Pad Via Library', 'CAM Document', 'Output Job File', and 'Database Link File'. The main workspace shows a 'Welcome' message for 'Erick Alejandro Chávez Vázquez' and a 'Refer a friend' banner. At the bottom, there is a survey question: 'How likely are you to recommend Altium Designer to a friend or colleague?' with a scale from 0 to 10.

## Dentro del PCB tenemos 3 Modos

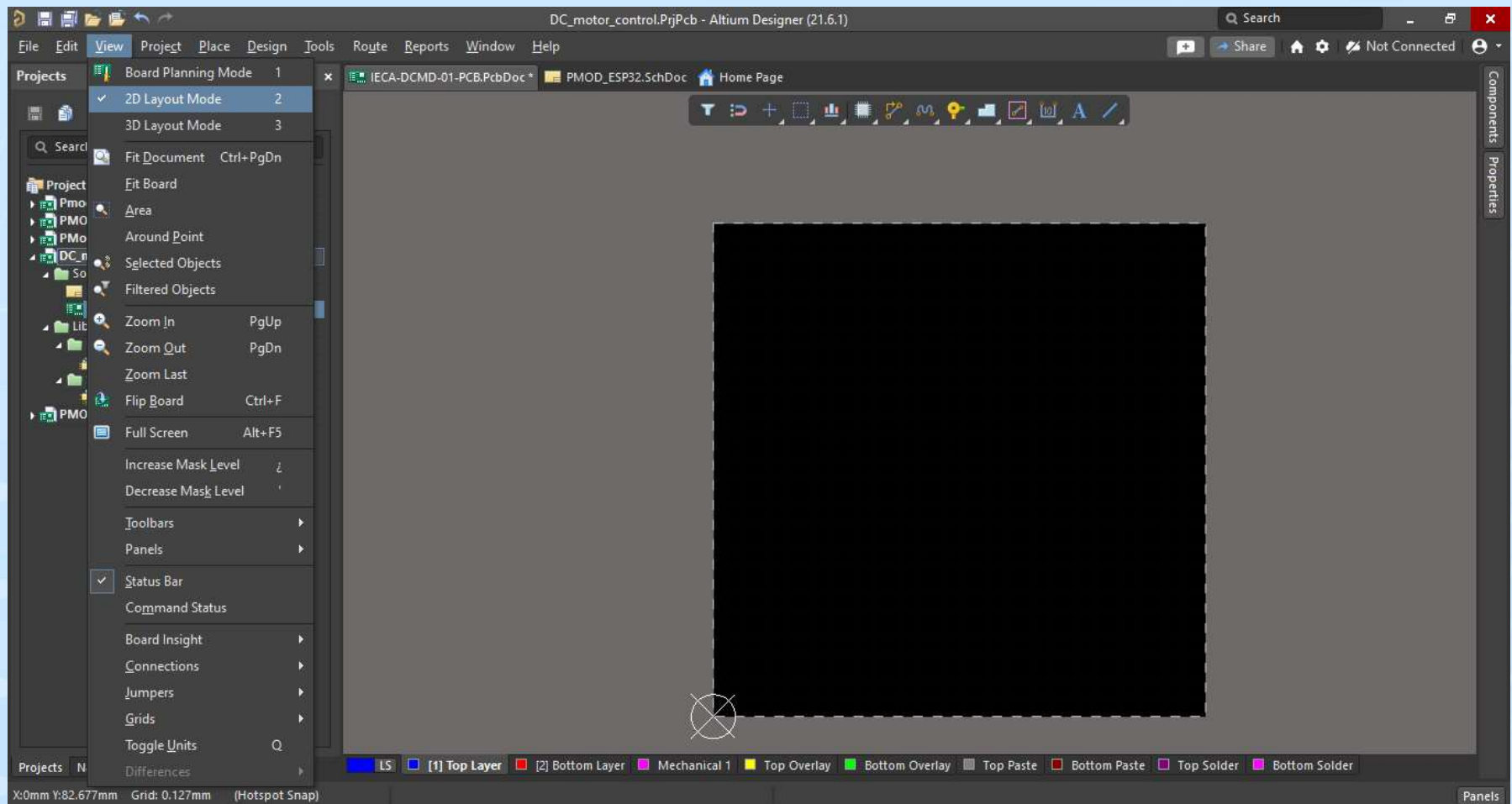
### Modo 1



## Herramientas para planear nuestro Board Outline

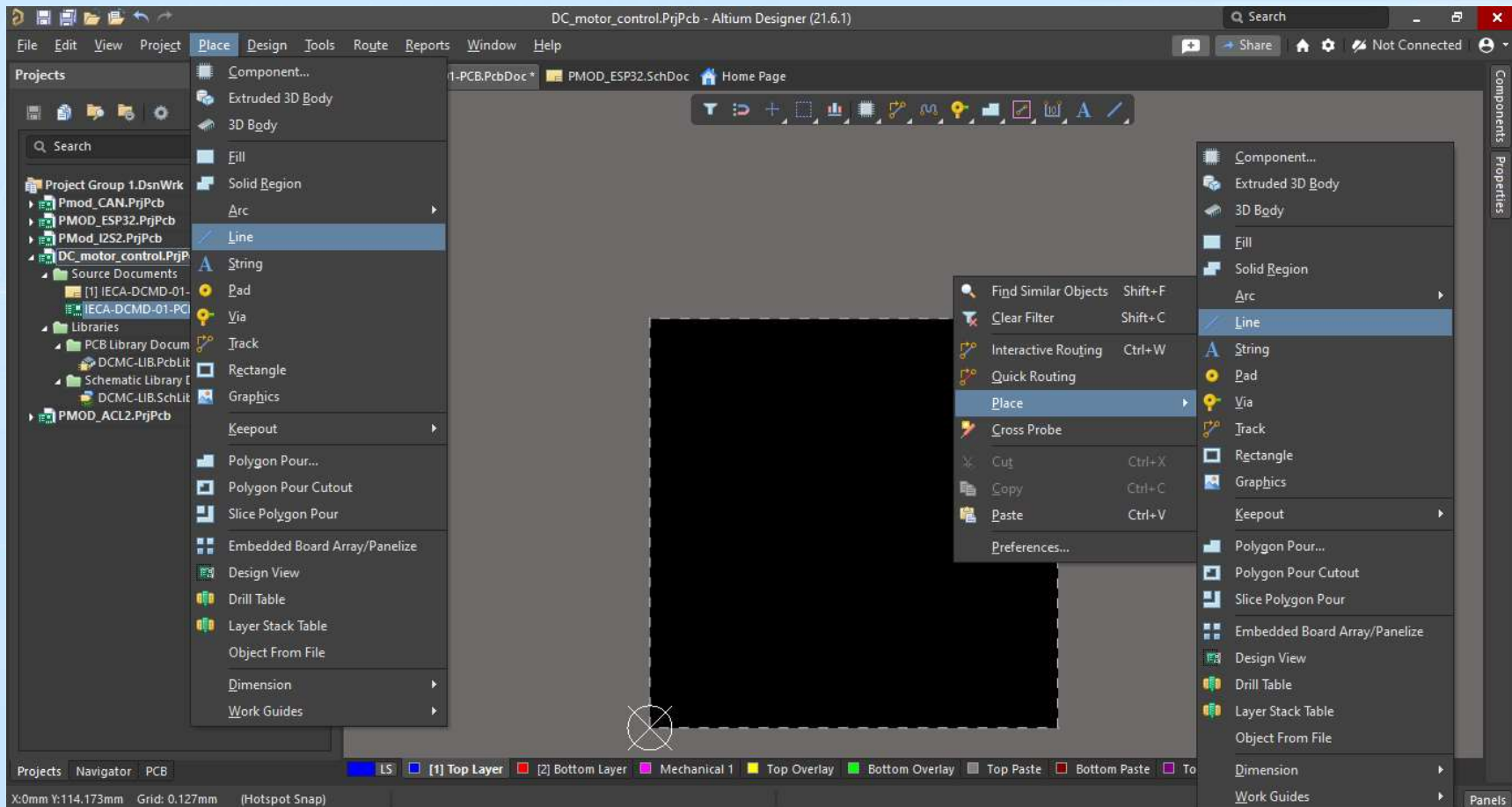


## Modo 2

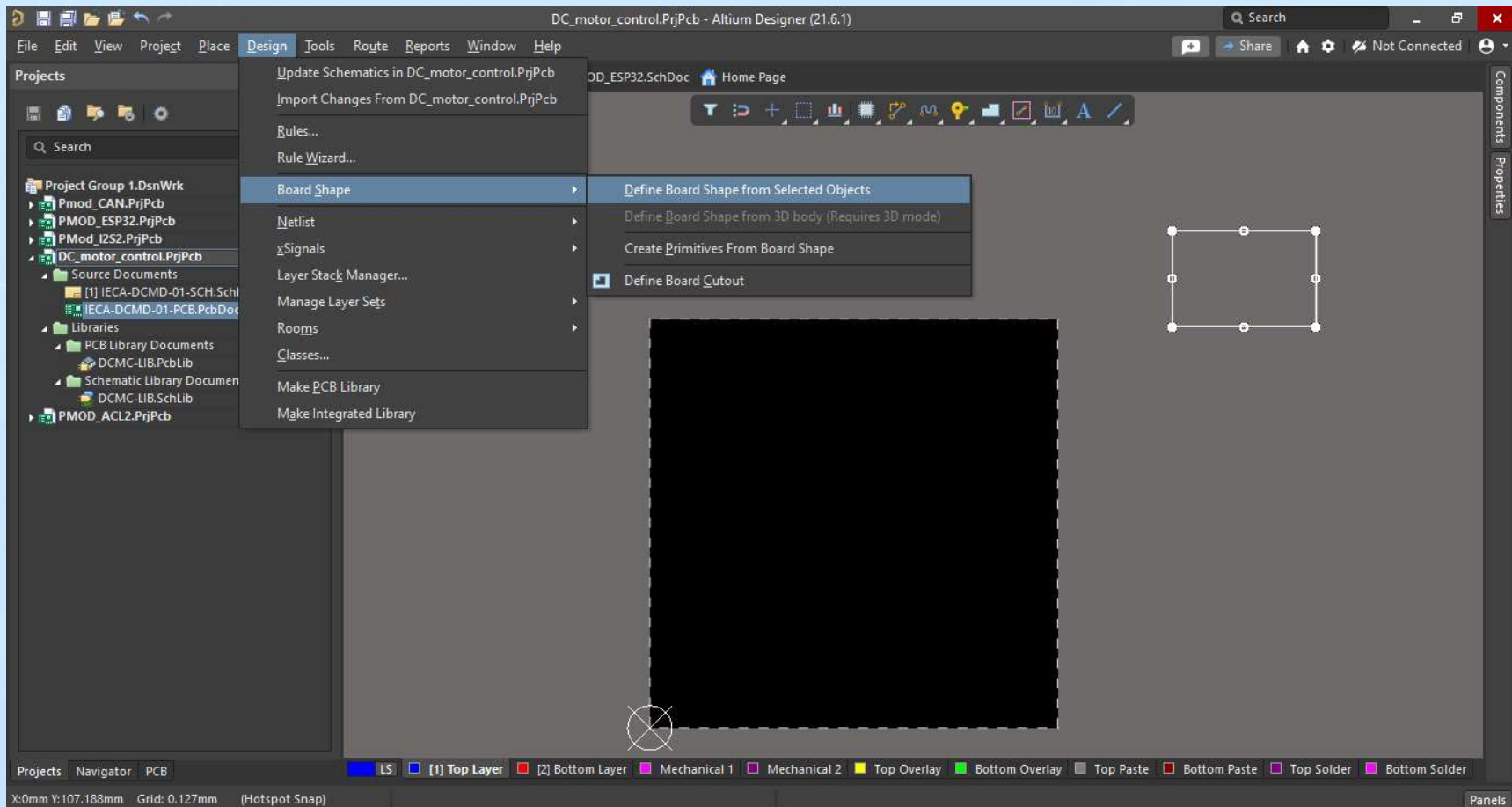




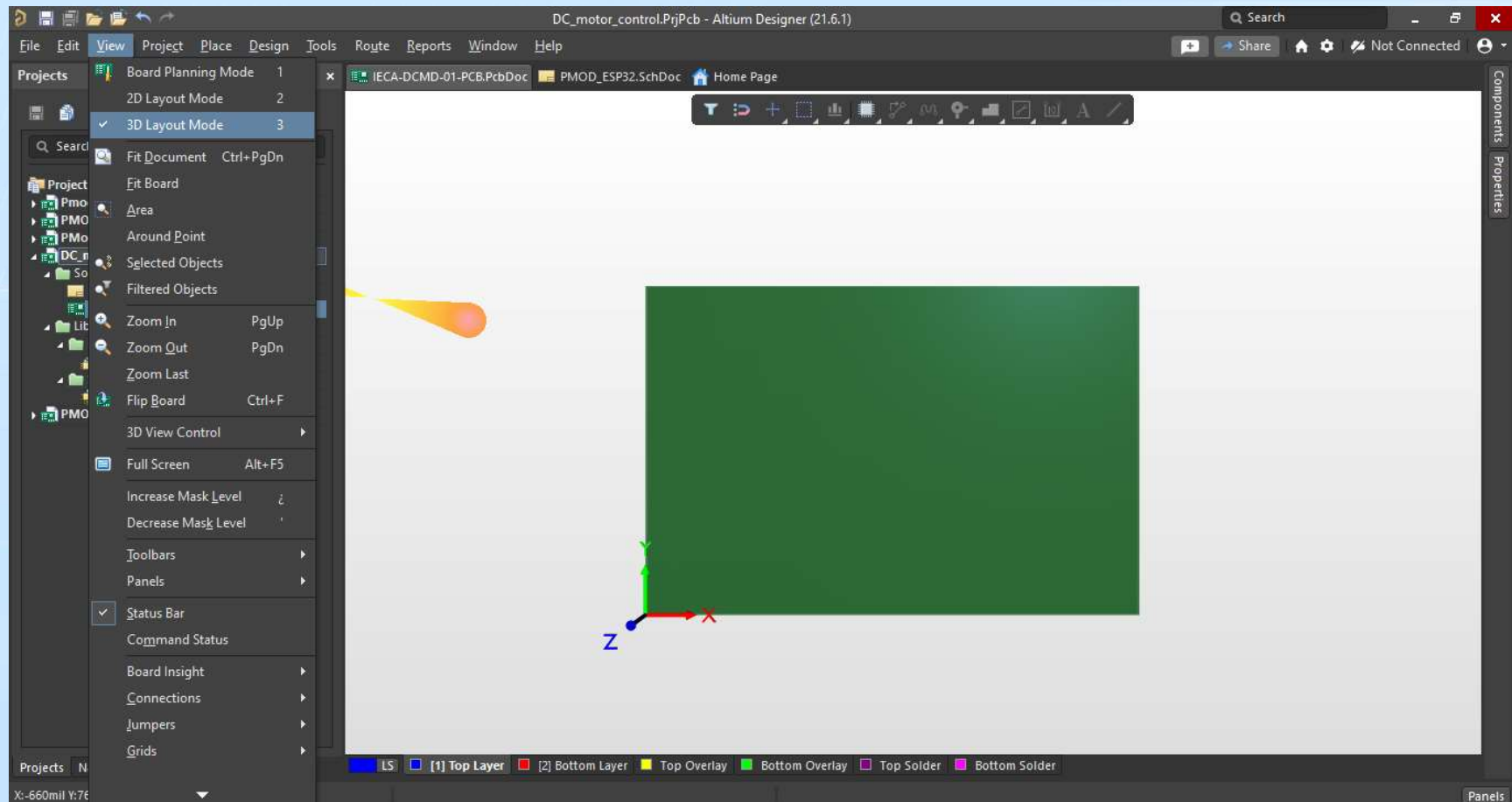
## Herramientas para la edición del Board Outline



## El PCB toma la forma de los objetos seleccionados



## Modo 3





# Compilación hacia el PCB

The screenshot shows the Altium Designer interface. The 'Design' menu is open, and the 'Update PCB Document IECA-ACL2.01-PCB.PcbDoc' option is highlighted. The main workspace displays a schematic diagram for 'PMOD ALC2'. The diagram includes a power supply section with a transformer (T1) and a rectifier bridge (BR1). It also features a microcontroller (U1) with various pins connected to resistors (R1-R10), capacitors (C1-C4), and a sensor (ADXL56HCZ-RL). A red arrow points to the 'Design' menu, and another red arrow points to the 'Update PCB Document' option.

Revisions

Rev	Description	Date	Checked by
0.1	Initial design		Jorge de la Torre

NOTES:  
ALL COMPONENTS MUST COMPLY WITH THE NOTES  
UNLESS OTHERWISE SPECIFIED.

PMOD\_I2S2.PrjPcb - Altium Designer (21.6.1)

File Edit View Project Place Design Tools Reports Window Help

Projects: IECA-ACL2.01-PCB.PcbDoc (5) IECA-I2S2-1-SCH.SchDoc PMODs.SchLib Home Page DCMC-LIB.SchLib Libreria\_EACHV.SchLib (3) PCB Library Document

### Engineering Change Order

Modifications		Affected Object	Affected Document	Status
Enable	Action			Check Done Message
Remove Net Class Members(2)				
<input checked="" type="checkbox"/>	Remove	NetC1_2 from POWER	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Remove	NetC12_2 from POWER	In IECA-I2S2-1-PCB.PcbDoc	
Change Source Component Designators(30)				
<input checked="" type="checkbox"/>	Modify	C1 -> C3	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	C3 -> C19	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	C4 -> C8	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	C6 -> C7	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	C7 -> C9	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	C8 -> C6	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	C9 -> C4	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	C12 -> C21	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	C13 -> C16	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	C16 -> C13	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	C17 -> C18	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	C18 -> C17	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	C19 -> C12	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	C21 -> C1	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	R4 -> R11	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	R5 -> R6	In IECA-I2S2-1-PCB.PcbDoc	
<input checked="" type="checkbox"/>	Modify	R6 -> R9	In IECA-I2S2-1-PCB.PcbDoc	

3 4 5

Validate Changes Execute Changes Report Changes... Only Show Errors Close

Projects Navigator Editor IECA-I2S2-1-SCH

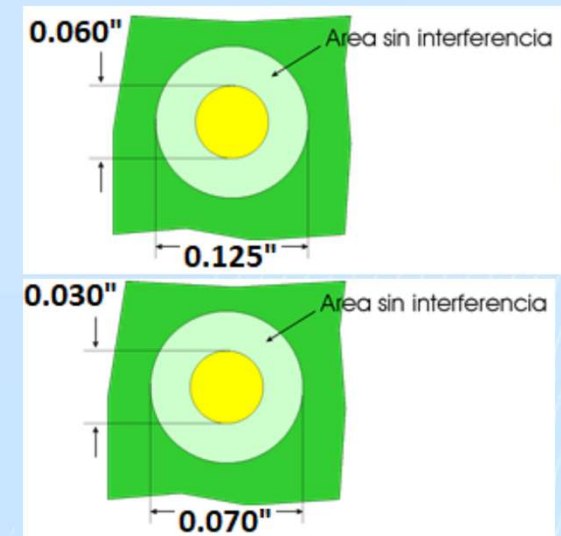
X:14050.000mil Y:1950.000mil Grid:50mil

Altium Designer (21.6.1)

## Fiducial

Un fiducial es un círculo o una cruz de cobre libre de máscara de soldadura que es usado por las máquinas de ensamble automático como referencia para colocar los componentes. Hay de dos tipos:

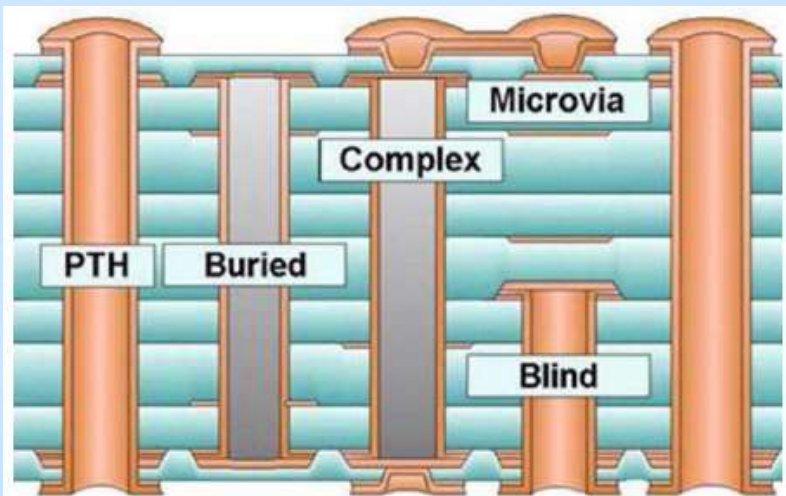
- Para tarjetas normalmente se agregan tres en las esquinas de la tarjeta a unas doscientas milésimas del borde El pad es circular de 0.060" de diámetro y debe de estar libre de cobre, solder mask y silkscreen en un radio de 0.030" alrededor del pad
- Para componentes Se requieren al menos dos fiducials para cada QFP con separación menor a 0.025" Un fiducial se centra en el componente y el otro en la misma esquina que el pin 1 El pad de cobre es de 0.030" de diámetro y debe de estar libre de cobre, solder mask y silkscreen en un radio de 0.020" alrededor del pad





## Vías

- Una vía sirve para conectar una señal de una capa a otra.
- Entre más pequeña una vía más cara
- El tamaño mínimo de la perforación de una vía esta dado por la relación largo/diámetro.
- Usualmente una relación arriba de 8 resulta muy difícil de fabricar (plateado).
- Ejemplo: una tarjeta de 0.062" de espesor con vías de diámetro 0.012" tienen una relación de 5.
- Generalmente 0.008 es el mínimo orificio para una vía Si se requiere menos, se tiene que migrar a perforación por laser
- Hay tres tipos de vías 'through hole', 'blind', 'buried', 'microvias' y 'via on pad'



Cost	Standard	Standard	+\$	++	+++	+++
Duration	Standard	Standard	+⌚	+⌚	+⌚⌚⌚	+⌚⌚⌚
Type	Through Via	Tented Via	Blind Via	Buried Via	Stacked Via	Via In Pad

## Definición de clases

1

Click Der.

2

The screenshot shows the Altium Designer interface. The 'Design' menu is open, and the 'Classes...' option is highlighted. The 'Object Class Explorer' dialog box is also open, showing a tree view of object classes. A red arrow labeled '1' points to the 'Design' menu. A red arrow labeled '2' points to the 'Classes...' option in the 'Design' menu. A red arrow labeled 'Click Der.' points to the 'Add Class' button in the 'Object Class Explorer' dialog box.

Object Class Explorer

Name	Class Type
POWER	Net Class
All Nets	Net Class

Component Class Generator...

OK Cancel



## Definición de capas para enrutado

1

2

3

The screenshot shows the Altium Designer (21.6.1) interface. The **Design** menu is open, showing options like **Rules...**, **Rule Wizard...**, **Board Shape**, **Netlist**, **Netlist**, **Signals**, **Layer Stack Manager...**, **Manage Layer Sets**, **Rooms**, **Classes...**, **Make PCB Library**, and **Make Integrated Library**. The **Rules** tree in the center shows a hierarchy of rules, with **RoutingLayers** selected. The **RoutingLayers** rule is configured in the **PCB Rules and Constraints Editor [mil]** panel on the right. The **Name** is **RoutingLayers**, **Comment** is empty, **Unique ID** is **XBOFVVEG**, and **Test Queries** is empty. The **Where The Object Matches** dropdown is set to **All**. The **Constraints** section is empty. The **Enabled Layers** section shows a table with two rows: **Allow Routing** and **Layer**. The **Allow Routing** column has checkboxes for **Top Layer** and **Bottom Layer**, both of which are checked.

Allow Routing	Layer
<input checked="" type="checkbox"/>	Top Layer
<input checked="" type="checkbox"/>	Bottom Layer

Switch to Document View Rule Wizard... Priorities... Create Default Rules OK Cancel Apply

Projects Navigator PCB [1] Top Layer X:-414mil Y:1574mil Grid: 1mil (Hotspot Snap) Panels

## Definir reglas para vías

1

2

3

The screenshot shows the Altium Designer (Z1.6.1) interface. The 'Design' menu is open, and the 'Rules...' option is selected. The 'PCB Rules and Constraints Editor [mil]' dialog is displayed, showing the 'RoutingVias' rule. The 'Where The Object Matches' dropdown is set to 'All'. The 'Constraints' section shows 'Min/Max preferred' for 'Via Diameter' with values: Minimum 20mil, Maximum 30mil, Preferred 21mil. A diagram of a via is shown with dimensions. The 'Via Hole Size' section shows: Minimum 10mil, Maximum 20mil, Preferred 11mil. The 'RoutingVias' rule is highlighted in the 'Design Rules' tree.

PCB Rules and Constraints Editor [mil]

Name: RoutingVias

Comment:

Unique ID: YOCNEPKT

Test Queries:

Where The Object Matches: All

Constraints: Min/Max preferred

Via Diameter: Minimum 20mil, Maximum 30mil, Preferred 21mil

Via Hole Size: Minimum 10mil, Maximum 20mil, Preferred 11mil

RoutingVias

Switch to Document View Rule Wizard... Priorities... Create Default Rules

OK Cancel Apply

Projects Navigator PCB

X: -262mil Y: 1261mil Grid: 1mil (Hotspot Snap)

## Definición de reglas de ancho de línea para las 'Nets'

1

2

3

PCB Rules and Constraints Editor [mil]

Name: Width\_POWER Comment: Unique ID: QKIAHIRX Test Queries

Where The Object Matches

Net Class: POWER

Constraints

Preferred Width: 10mil

Min Width: 7mil Max Width: 20mil

Check Tracks/Arcs Min/Max Width Individually

Check Min/Max Width for Physically Connected

Use Impedance Profile

Min Width	Preferred Width	Max Width	Layer Name
7mil	10mil	20mil	1 - Top Layer
7mil	10mil	20mil	2 - Bottom Layer

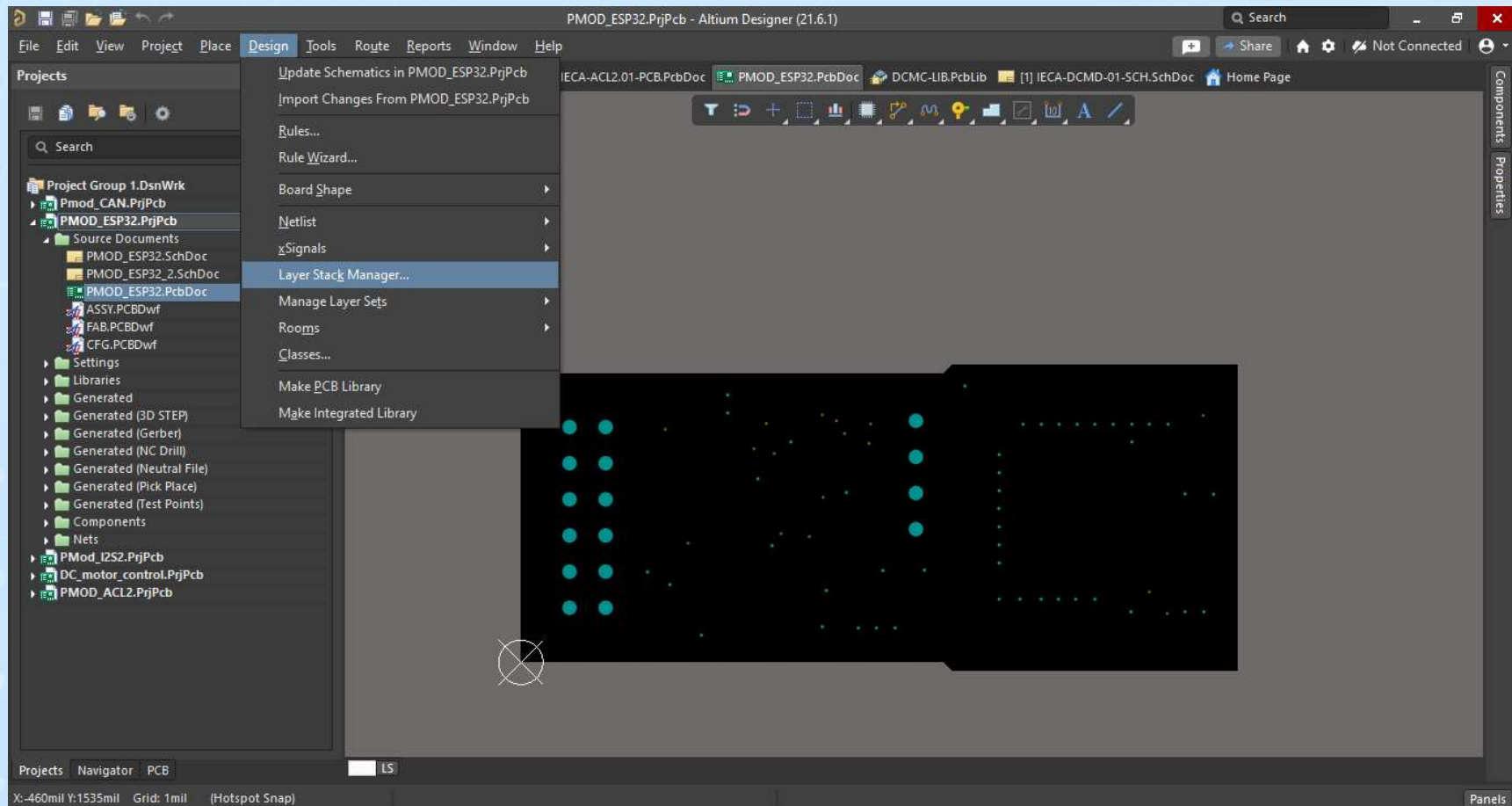
Switch to Document View Rule Wizard... Priorities... Create Default Rules OK Cancel Apply

Projects Navigator PCB LS

X: -262mil Y: 1261mil Grid: 1mil (Hotspot Snap)

Panels

## Definir Stack-up





## Editor de Stack-up

PMOD\_ESP32.PrjPcb - Altium Designer (21.6.1)

File Edit View Project Tools Window Help

Projects (3) PCB Document PMOD\_ESP32.PcbDoc [Stackup] DCMC-LIB.PcbLib [1] IECA-DCMD-01-SCH.SchDoc Home Page

Search

Project Group 1.DsnWrk

- Pmod\_CAN.PrjPcb
- PMOD\_ESP32.PrjPcb
  - Source Documents
    - PMOD\_ESP32.SchDoc
    - PMOD\_ESP32\_2.SchDoc
    - PMOD\_ESP32.PcbDoc
    - PMOD\_ESP32.PcbDoc [Stackup]
  - ASSY.PCBDwf
  - FAB.PCBDwf
  - CFG.PCBDwf
  - Settings
  - Libraries
  - Generated
    - Generated (3D STEP)
    - Generated (Gerber)
    - Generated (NC Drill)
    - Generated (Neutral File)
    - Generated (Pick Place)
    - Generated (Test Points)
  - Components
  - Nets
- PMod\_I2S2.PrjPcb
- DC\_motor\_control.PrjPcb
- PMOD\_ACL2.PrjPcb

Stackup

#	Name	Material	Type	Thickness	Dk	Weight	Df
	Top Overl		Overlay				
	Top S	Resist	Solder Mask	0.4mil	3.5		
1	Top Layer		Signal	1.4mil		1oz	
	Dielectric 1	FR-4	Dielectric	58.4mil	4.8		
2	Bottom Layer		Signal	1.4mil		1oz	
	Bottom So		Plane		3.5		
	Bottom O		Core				
			Prepreg				
			Surface Finish				
			Solder Mask				
			Overlay				

Click Der.

Insert layer above

Insert layer below

Move layer up

Move layer down

Delete layer

Cut Ctrl+X

Copy Ctrl+C

Paste Ctrl+V

Signal

Plane

Core

Prepreg

Surface Finish

Solder Mask

Overlay

Projects Navigator Stackup Impedance Via Types

X: -261mil Y: 1577mil Grid: 1mil (Hotspot Snap)

Components Properties

Search

Share

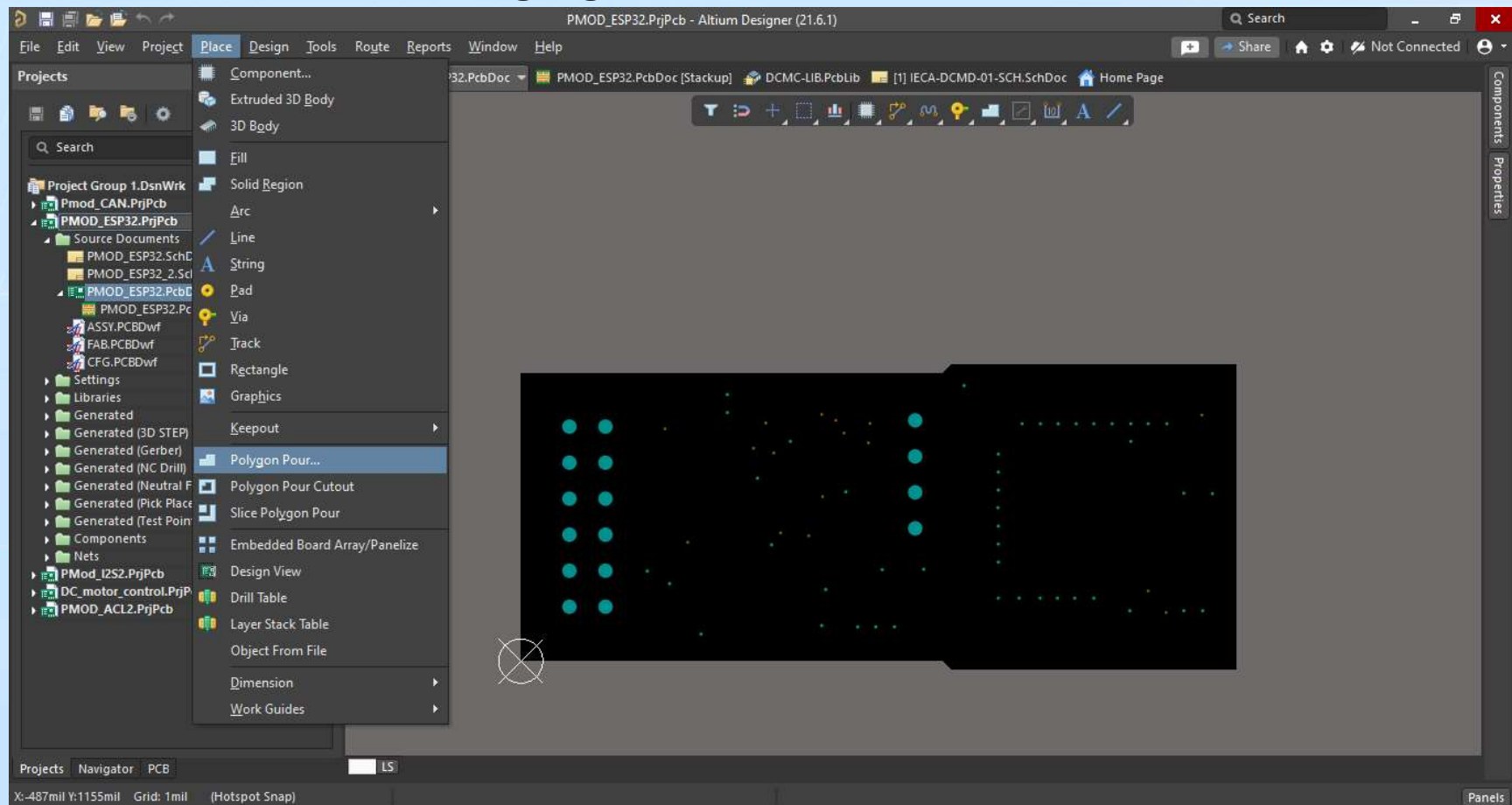
Not Connected

Features

Panels



## Agregar Fill Areas de cobre



## Agregar Fill Areas de cobre

PMOD\_ESP32.PrjPcb - Altium Designer (21.6.1)

Properties

Polygon Pour

Components (and 12 more)

Search

(X/Y) 30mil 770mil

Solid Hatched None

Hide preview

☒ Remove Islands Less Than 2500 sq.mil

Arc Approx. 0.5mil

☒ Remove Necks Less Than 5mil

Pour Over Same Net Polygons Only

☐ Remove Dead Copper

☐ Optimal Void Rotation

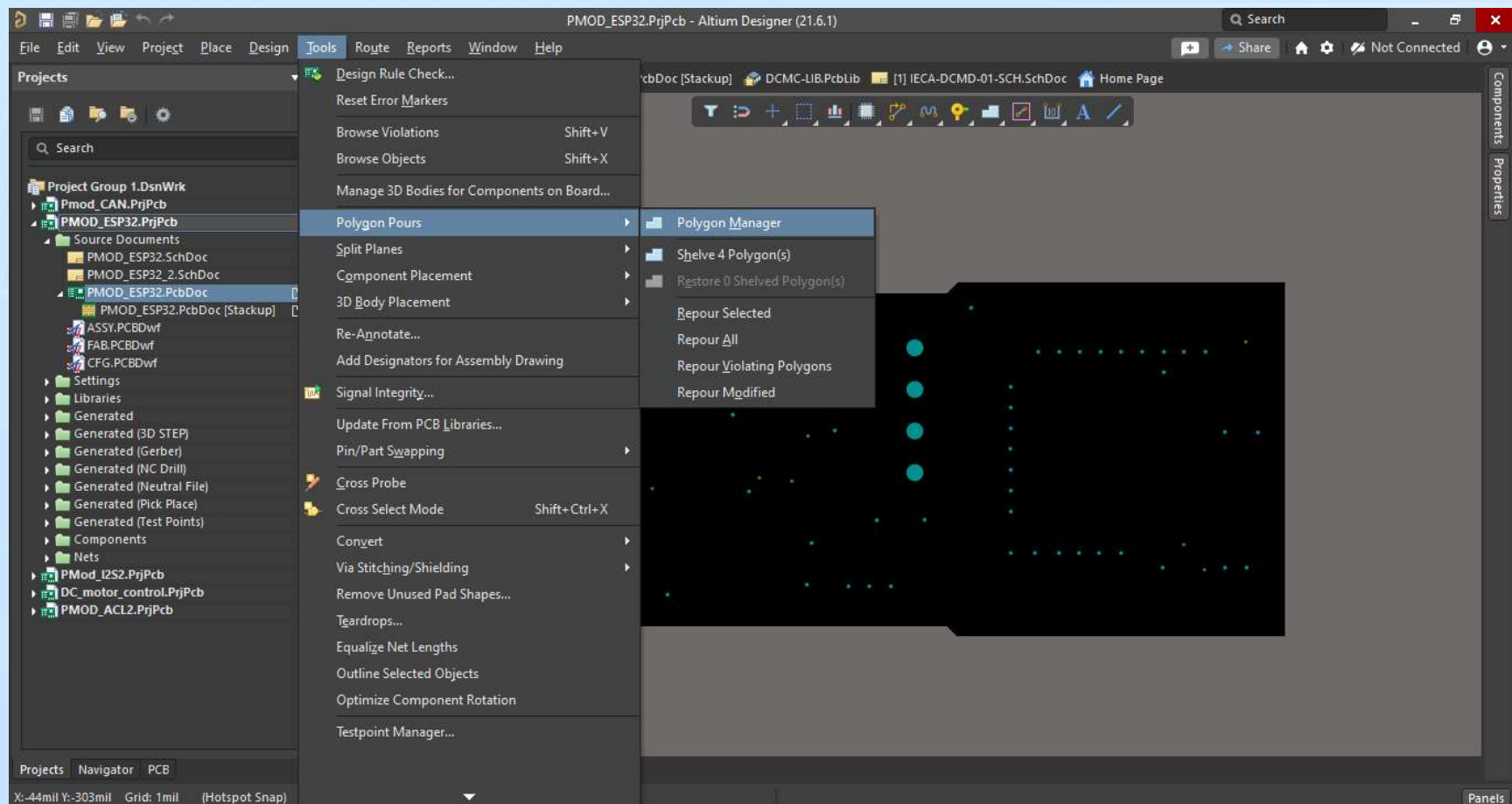
Outline Vertices

Index	X	Y	Arc Angle (Neg=CW)
0	30mil	770mil	
1	1170mil	770mil	
2	1200mil	795mil	
3	1955mil	795mil	

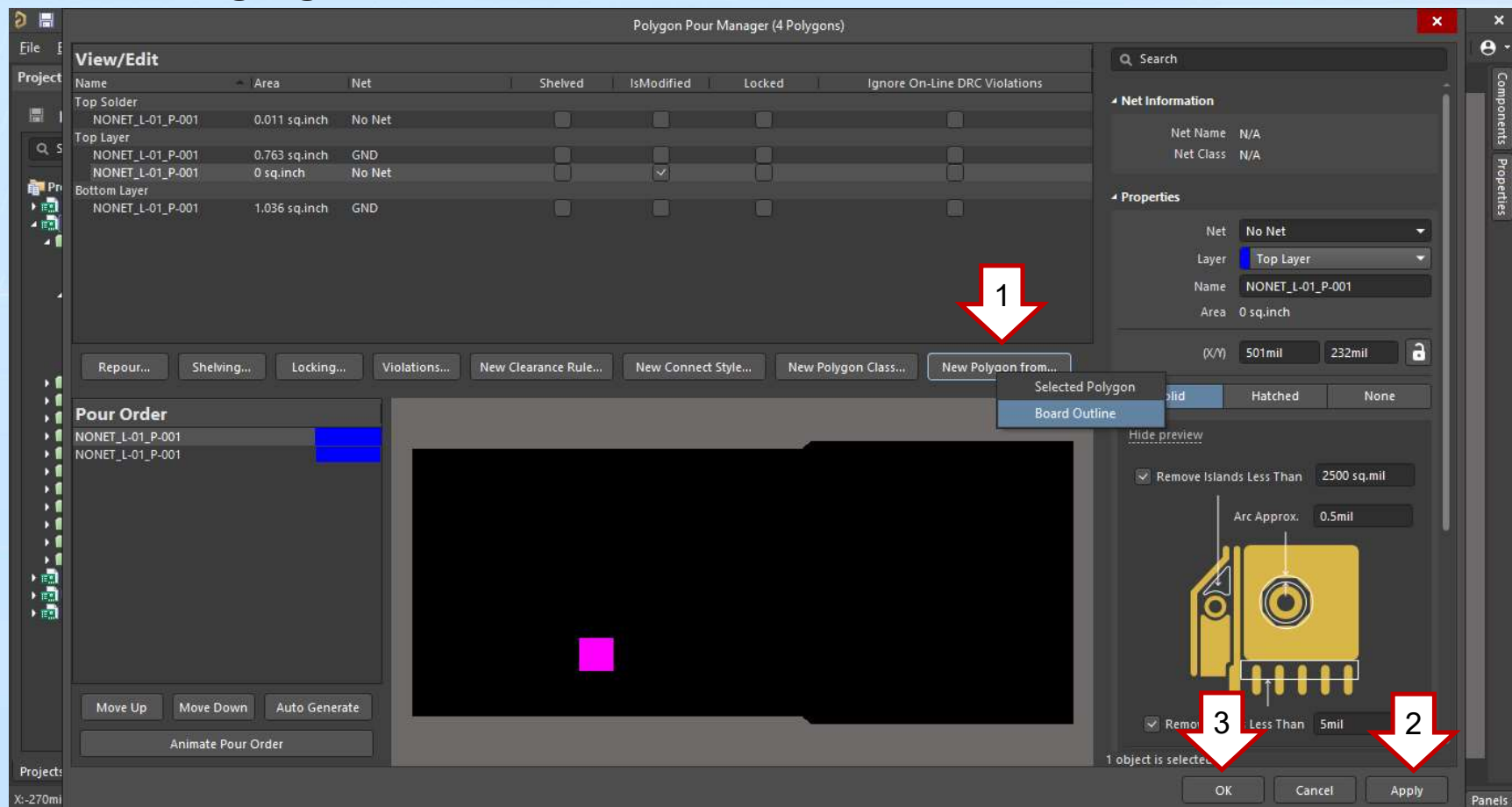
Projects Navigator PCB

X: 466mil Y: 1051mil Grid: 1mil (Hotspot Snap)

## Creación de un PIN



## Agregar un Fill de forma automática al tamaño del PCB



## Placement

La colocación de componentes debe de hacerse visualizando el futuro enrutado de los componentes, muchas veces es necesario rotar, cambiar de cara o hasta redefinir las conexiones en partes tanto como sea posible para lograr un enrutado mas limpio, corto y directo

Hay varias formas de colocar componentes, pero podemos hablar de 2 principales

- ✓ Automáticamente usando la herramienta
- ✓ Manualmente por características de las partes

Al hacer la colocación se pueden hacer las siguientes cosas

- Rotar componentes
- Cambiar de lado
- Intercambiar componentes
- Intercambiar pines
- Intercambiar compuertas
- Iluminar conexiones
- Proteger componentes



## Placement

Orden de colocación de componentes:

- Colocar primero los componentes que tienen localización fija (conectores, LEDs, etc.)
- Colocar componentes principales (circuitos con muchos pines, componentes sensibles al ruido, temperatura o altura, osciladores, cristales)
- Revisar junto con el ingeniero de hardware esta primera colocación de componentes
- Colocar capacitores de desacoplo, terminadores y otros pasivos sensibles
- Colocar el resto de los componentes
- Colocar los puntos de prueba

La colocación de componentes se hace siguiendo:

- ✓ Las guías de diseño
- ✓ Las reglas de diseño para manufactura
- ✓ Que resulte el enrutado más sencillo
- ✓ Estética

## Enrutado

### Orden de enrutado

- Definir y asignar reglas para las 'nets'
- Señales críticas ( pares diferenciales, etc
- Alimentación
- Buses
- Resto de las señales

El enrutado se hace siguiendo

- Las guías de diseño

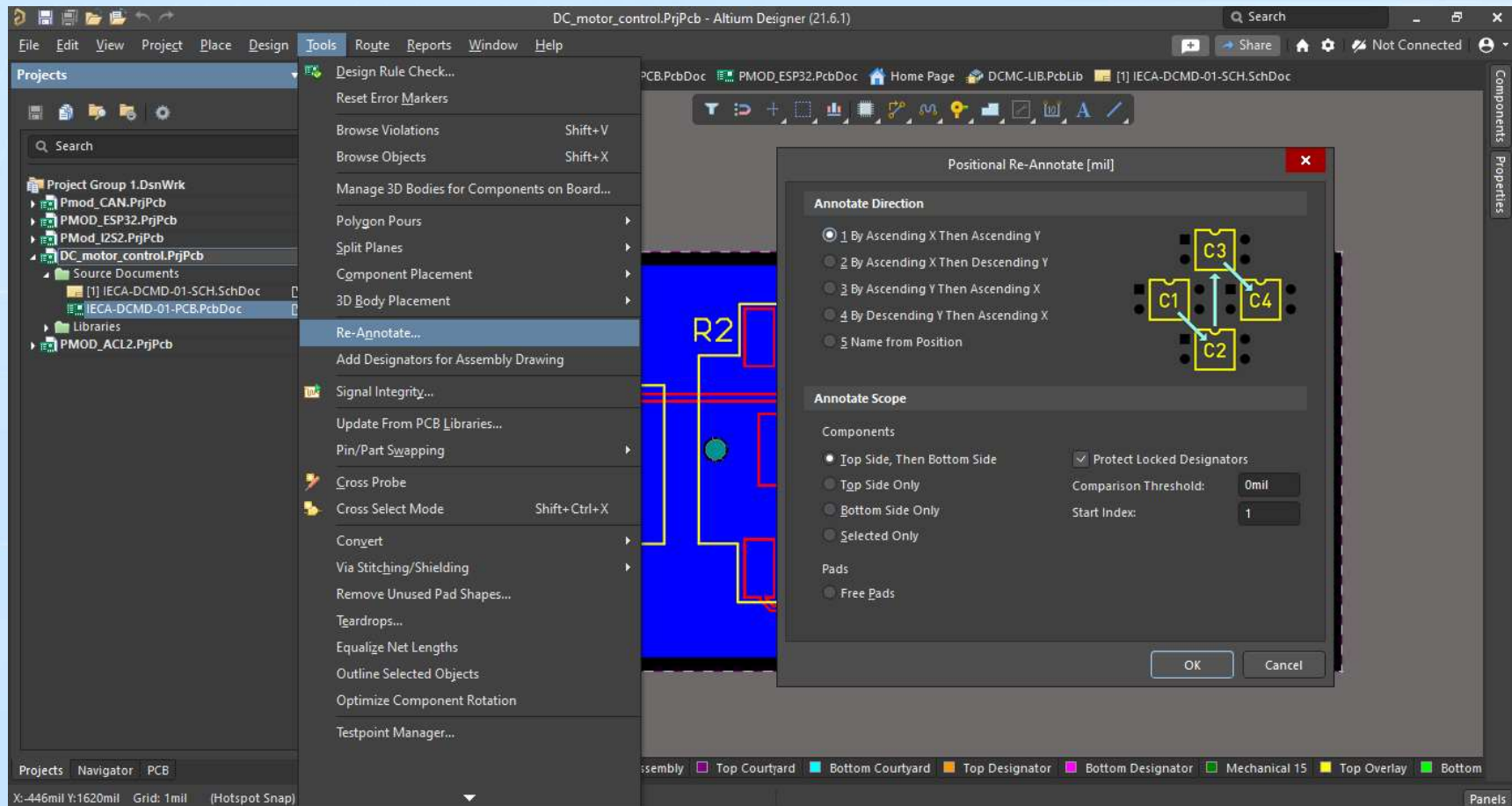
El enrutado puede ser automático o interactivo Se recomienda enrutar manualmente señales críticas y alimentaciones, luego proteger el enrutado y correr el enrutador automático.

Una vez terminado el enrutado, se debe correr el DRC Design Rule Check y corregir los errores.

## Silkscreen

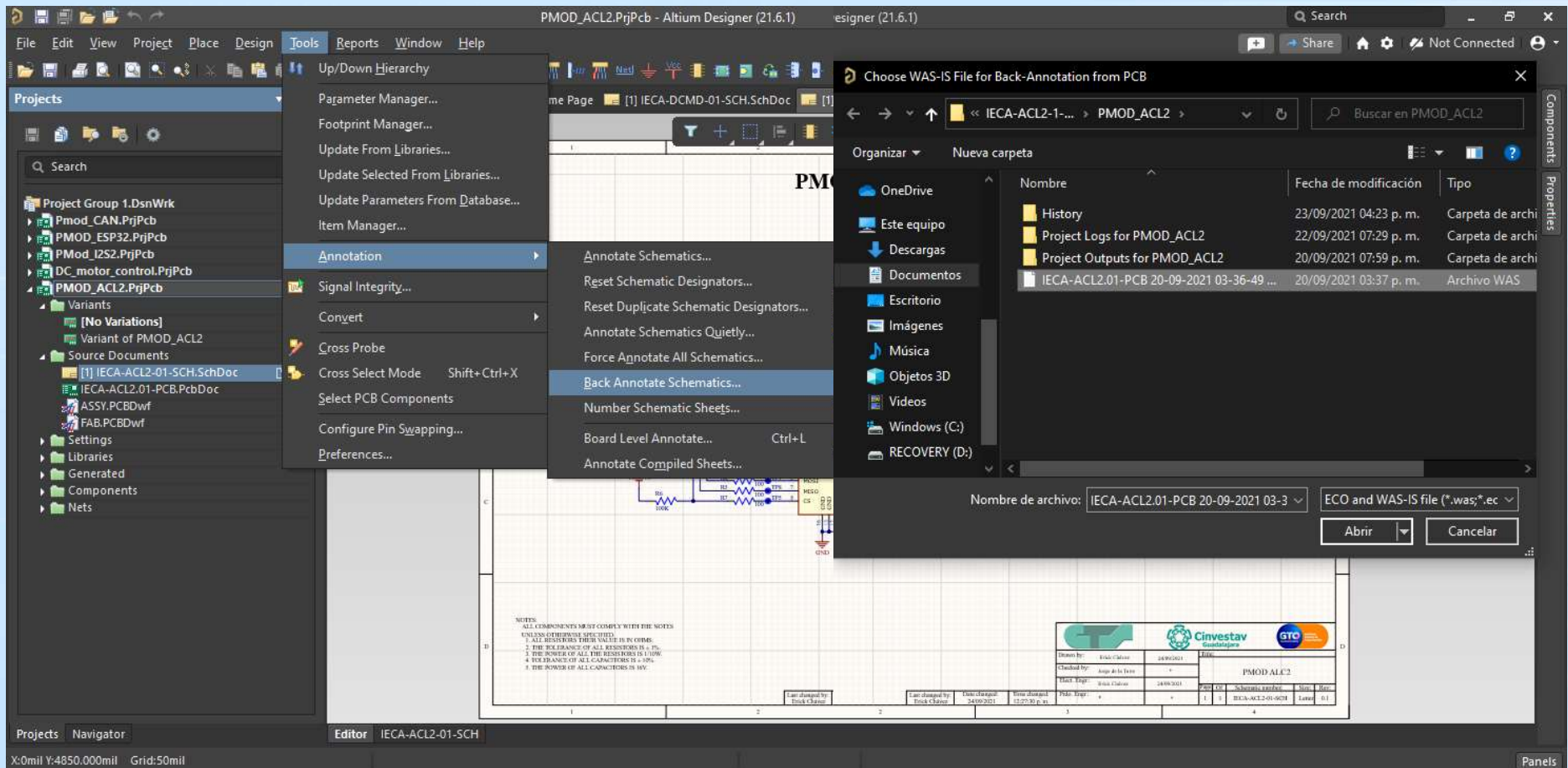
- ❖ El Silkscreen aparece automáticamente en el PCB una vez que se compila el diseño lugar en el cual se asignan automáticamente los valores no definidos que contienen letra + ?
- ❖ El Silkscreen suele ser de color blanco aunque se puede solicitar al fabricante utilizar otros colores siempre y cuando el contraste con la máscara de soldadura sea adecuado.
- ❖ Al agregar el Silkscreen , la mínima distancia con pads o vías, se recomienda de 6 milésimas de pulgada.
- ❖ Es recomendable usar 10 milésimas de pulgada de separación
- ❖ El Silkscreen nunca debe de colocarse sobre estaño o cobre expuesto

## Remuneración de Silkscreen





# Back Annotation



PMOD\_ACL2.PrjPcb - Altium Designer (21.6.1) esigner (21.6.1)

File Edit View Project Place Design Tools Reports Window Help

Up/Down Hierarchy  
Parameter Manager...  
Footprint Manager...  
Update From Libraries...  
Update Selected From Libraries...  
Update Parameters From Database...  
Item Manager...

Annotation  
Signal Integrity...  
Convert  
Cross Probe  
Cross Select Mode Shift+Ctrl+X  
Select PCB Components  
Configure Pin Swapping...  
Preferences...

Annotate Schematics...  
Reset Schematic Designators...  
Reset Duplicate Schematic Designators...  
Annotate Schematics Quietly...  
Force Annotate All Schematics...  
**Back Annotate Schematics...**  
Number Schematic Sheets...  
Board Level Annotate... Ctrl+L  
Annotate Compiled Sheets...

Choose WAS-IS File for Back-Annotation from PCB

Organizar Nueva carpeta

OneDrive  
Este equipo  
Descargas  
Documentos  
Escritorio  
Imágenes  
Música  
Objetos 3D  
Videos  
Windows (C:)  
RECOVERY (D:)

Nombre de archivo: IECA-ACL2.01-PCB 20-09-2021 03-3 ECO and WAS-IS file (\*.was;\*.ec)

Abrir Cancelar

Projects Navigator Editor IECA-ACL2-01-SCH

X:0mil Y:4850.000mil Grid:50mil

Notes:  
ALL COMPONENTS MUST COMPLY WITH THE NOTES  
UNLESS OTHERWISE SPECIFIED.  
1. ALL RESISTORS THEIR VALUE IS IN OHMS.  
2. THE TOLERANCE OF ALL RESISTORS IS ± 1%.  
3. THE POWER OF ALL THE RESISTORS IS 1/10W.  
4. THE TOLERANCE OF ALL CAPACITORS IS ± 10%.  
5. THE POWER OF ALL CAPACITORS IS 1W.

Drawn By	Drawn Date	Drawn Time	Drawn User	Drawn Version
Diego de la Torre	24/09/2021	14:00:00	Diego de la Torre	1.0

PMOD ACL2

Sheet No.	Sheet Count	Sheet Name	Sheet Type	Sheet Date
1	1	IECA-ACL2-01-PCB	PCB	2021.09.24

Panel



## Back Annotation

Altium Designer (21.6.1) - PMOD\_ACL2.PrjPcb

File Edit View Project Place Design Tools Reports Window Help

Projects: IECA-DCMD-01-PCB.PcbDoc, Home Page, [1] IECA-DCMD-01-SCH.SchDoc, [1] IECA-ACL2-01-SCH.SchDoc

Search: [ ]

Project Group 1.DsnWrk

- PMOD\_CAN.PrjPcb
- PMOD\_ESP32.PrjPcb
- PMOD\_I2S2.PrjPcb
- DC\_motor\_control.PrjPcb
- PMOD\_ACL2.PrjPcb
  - Variants
    - [No Variations]
    - Variant of PMOD\_ACL2
  - Source Documents
    - [1] IECA-ACL2-01-SCH.SchDoc
    - IECA-ACL2-01-PCB.PcbDoc
    - ASSY.PCBDwf
    - FAB.PCBDwf
  - Settings
  - Libraries
  - Generated
  - Components
  - Nets

Information

Change(s) made  
23 change(s) were made from previous state  
23 change(s) were made from original state

OK

PMOD ALC2

Revisions

Rev	Description	Date	Checked by
0.1	Initial Design		Jorge de la Torre

NOTES

1. ALL COMPONENTS MUST COMPLY WITH THE NOTES
2. UNLESS OTHERWISE SPECIFIED
3. ALL RESISTORS THEIR VALUES IS IN OHMS
4. THE TOLERANCE OF ALL RESISTORS IS ± 1%
5. THE POWER OF ALL THE RESISTORS IS 1/8W
6. THE TOLERANCE OF ALL CAPACITORS IS ± 10%
7. THE POWER OF ALL CAPACITORS IS 10V

Drawn By: Jorge de la Torre, 24/09/2021, 14:00:00

Checked By: Jorge de la Torre, 24/09/2021, 14:00:00

Part: PMOD ALC2

Rev: 0.1

IECA-ACL2-01-SCH

X:1050.000mil Y:6700.000mil Grid:50mil

PMOD\_ACL2.PrgPcb - Altium Designer (21.6.1)

File Edit View Project Place Design Tools Reports Window Help

Projects

Search

Project Group 1

- PMOD\_CAN.F
- PMOD\_ESP32
- PMOD\_I2S2.P
- DC\_motor.cc
- Source Documents
- [1] IECA-ACL2-01-SCH.SchDoc
- Libraries
- PCB Libraries
- DCMC
- Schematic Documents
- DCMC
- Component Libraries
- PMOD\_ACL2
- Variants
- [No Variants]
- Variant c
- Source Documents
- [1] IECA-ACL2-01-SCH.SchDoc
- IECA-ACL2-01-SCH.SchDoc
- ASSY.PCB
- FAB.PCB
- Settings
- Libraries
- PCB Libraries
- Schematic Documents
- PMOD
- Generated Documents
- Component Libraries
- Nets

Schematic Annotation Configuration

Order of Processing: Across Then Down

Matching Options

Complete Existing Packages: None

Component Parameter: Strictly

Process Location of: Designator

Replace Sub-Parts: Off

Schematic Sheets To Annotate

Schematic Sheet	Annotation Scope	Order	Match
IECA-ACL2-01-SCH.SchDoc	All	0	1

Buttons: All On, All Off

Proposed Change List

Current Designator	Sub	Proposed Designator	Sub	Location of Part
C1		C?		IECA-ACL2-01-SCH.SchDoc
C2		C?		IECA-ACL2-01-SCH.SchDoc
C3		C?		IECA-ACL2-01-SCH.SchDoc
C4		C?		IECA-ACL2-01-SCH.SchDoc
J1		J?		IECA-ACL2-01-SCH.SchDoc
JP1		JP?		IECA-ACL2-01-SCH.SchDoc
JP2		JP?		IECA-ACL2-01-SCH.SchDoc
L1		L?		IECA-ACL2-01-SCH.SchDoc
R?		R?		IECA-ACL2-01-SCH.SchDoc
R?		R?		IECA-ACL2-01-SCH.SchDoc
R?		R?		IECA-ACL2-01-SCH.SchDoc
R?		R?		IECA-ACL2-01-SCH.SchDoc
R?		R?		IECA-ACL2-01-SCH.SchDoc
R?		R?		IECA-ACL2-01-SCH.SchDoc
R?		R?		IECA-ACL2-01-SCH.SchDoc
R?		R?		IECA-ACL2-01-SCH.SchDoc
R?		R?		IECA-ACL2-01-SCH.SchDoc
TP?		TP?		IECA-ACL2-01-SCH.SchDoc
TP?		TP?		IECA-ACL2-01-SCH.SchDoc
TP3		TP?		IECA-ACL2-01-SCH.SchDoc

Information

Change(s) made  
28 change(s) were made from previous state  
23 change(s) were made from original state

Annotation Summary

Annotation is enabled for all schematic documents. Parts will be matched using 2 parameters, all of which must be strictly matched. (Under strict matching, parts will only be matched if they all have the same parameters and parameter values, with respect to the matching criteria. Enabling this will extend the semantics slightly by allowing parts which do not have the specified parameters to be matched.) Existing packages will not be completed. All new parts will be added to new packages.

Buttons: Update Changes List, Reset All, Back Annotate, Accept Changes (Create ECO), Close

Projects Navigator: Editor IECA-ACL2-01-SCH

X:0mil Y:8500.000mil Grid:50mil

Panels

Altium Designer (21.6.1) - PMOD\_ACL2.PrjPcb

File Edit View Project Place Design Tools Reports Window Help

Projects

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Schematic Annotation Configuration

Proposed Change List

Engineering Change Order

Enable	Action	Affected Object		Affected Document	Status		
					Check	Done	Message
Annotate Component(23)							
<input checked="" type="checkbox"/>	Modify	C1 -> C4	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	C2 -> C3	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	C3 -> C2	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	C4 -> C1	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	R1 -> R3	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	R2 -> R5	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	R3 -> R2	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	R4 -> R1	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	R5 -> R7	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	R6 -> R8	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	R7 -> R9	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	R8 -> R6	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	R9 -> R4	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	TP1 -> TP8	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	TP2 -> TP4	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	TP3 -> TP9	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	TP4 -> TP6	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	TP5 -> TP10	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	TP6 -> TP2	In	IECA-ACL2-01-SCH.SchDoc			
<input checked="" type="checkbox"/>	Modify	TP7 -> TP1	In	IECA-ACL2-01-SCH.SchDoc			

4 5 6

Validate Changes Execute Changes Report Changes... Only Show Errors

All On All Off

Update Changes List Reset All Back Annotate Accept Changes (Create ECO)

Close

Close

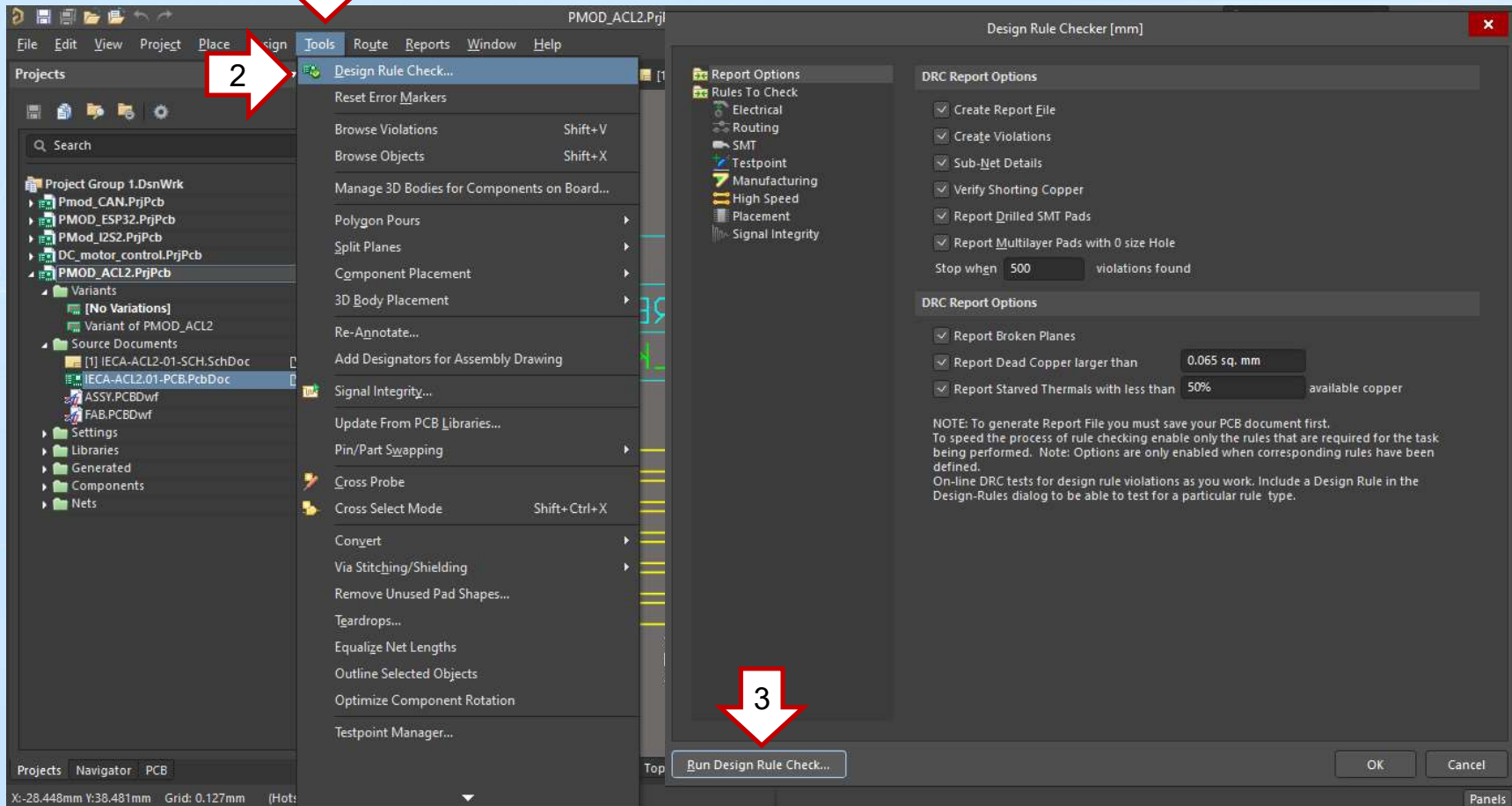
Editor IECA-ACL2-01-SCH

X:0mil Y:8500.000mil Grid:50mil

Panels



## Design Rule Check (DRS)



1

2

3

Design Rule Checker [mm]

Report Options

- Rules To Check
  - Electrical
  - Routing
  - SMT
  - Testpoint
  - Manufacturing
  - High Speed
  - Placement
  - Signal Integrity

DRC Report Options

- ☒ Create Report File
- ☒ Create Violations
- ☒ Sub-Net Details
- ☒ Verify Shorting Copper
- ☒ Report Drilled SMT Pads
- ☒ Report Multilayer Pads with 0 size Hole

Stop when 500 violations found

DRC Report Options

- ☒ Report Broken Planes
- ☒ Report Dead Copper larger than 0.065 sq. mm
- ☒ Report Starved Thermals with less than 50% available copper

NOTE: To generate Report File you must save your PCB document first.  
To speed the process of rule checking enable only the rules that are required for the task being performed. Note: Options are only enabled when corresponding rules have been defined.  
On-line DRC tests for design rule violations as you work. Include a Design Rule in the Design-Rules dialog to be able to test for a particular rule type.

Run Design Rule Check... OK Cancel