Circuit Theory and Electronics Fundamentals

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Laboratory Assignment - T5

Group nº59

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Contents

1 Introduction

The objective of this laboratory assignment is to create a BandPass Filter (BPF) circuit using one OP-AMP with a gain at central frequency of 40db and a central frequency of 1000Hz. The goal is then to attain the maximum value for the Merit (M) by modifying the circuit and its components with some restricted. The expression for M is as follows:

$$M = \frac{1}{Cost \times (CentralfFreqDev + GainDev + 10^{-6})}$$

$$Cost = Cost_{resistors} + Cost_{capacitors} + Cost_{transistors} + Cost_{diodes}$$

$Cost_{resistors} = 1MU/kOhm; Cost_{capacitors} = 1MU/\mu F; Cost_{diodes} = 0.1MU/diode; Cost_{transistors} = 0.1MU/transistor$

The final circuit, displayed in figure 1, utilizes the following components:

- three voltage sources (V_{in} - sinusoidal, V_{cc} and V_{ee})
- one 741 OP-AMP
- three resistors (R_1, R_2 and R_3)
- one capacitors (C_1)

The values associated with each component is displayed on Table 1. The OP-AMP used was already provided as well as the voltage source V_{in}.

Name	Value
V_{cc}	5.00
V_{ee}	-5.00
$R1$	1.0k
$R2$	100.0k
$R3$	10.0k
C_1	220.0n

Table 1: Components' values.

Theoretical and simulation analysis are presented in Section 2 and Section 3, respectively, and the results of each are then compared. Finally, in Section 4 the conclusions of the laboratory assignment are outlined.

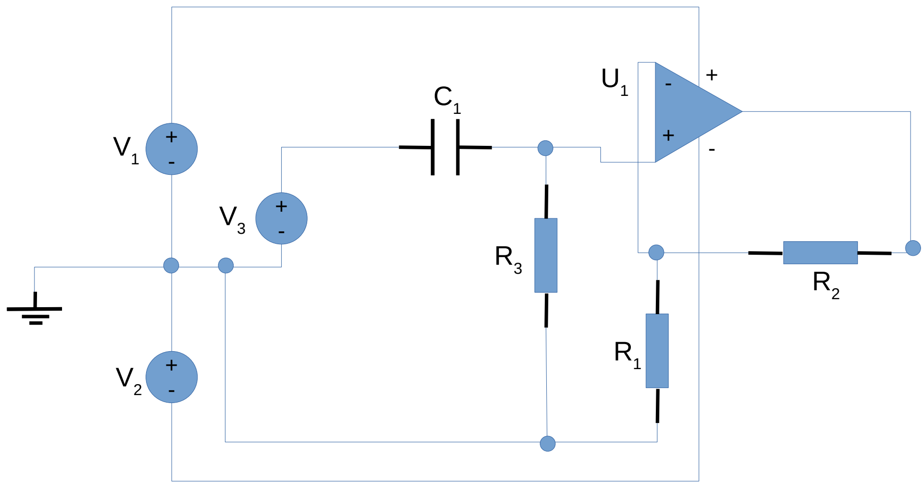

Figure 1: Circuit T5

2 Theoretical Analysis

In this section we will explain the inner workings of the class A audio amplifier created and perform a theoretical analysis of each component. The common Kirchoff laws and the simplified BJT equation were used to perform the analysis.

2.1 Gain stage - Degenerated Common Emitter Amplifier

It is in this stage of the amplifier that most of the signal amplification takes place. This stage is comprised of a NPN tansistor, two capacitors (coupling and bypass) and four resistors (two for the voltage divider, R_1 and R_2, one for the temperature stabilization R_E and another to set the no signal current, R_C).

The base voltage of the transistor needs to be forward biased in order for the NPN transistor to work in the forward-active region. For that reason, a voltage divider is added to make sure that the base voltage is always larger than $0.7V$. A coupling capacitor is added between the voltage divider and the signal source in order to add the input AC signal to the voltage divider DC signal (this will be explained in more detail in the simulation section).

The resistor R_C is used to set the zero signal current that passes trough the BJT.

The resistance R_E adds temperature stabilization and removes the temperature dependency of the gain in the circuit but has the drawback of decreasing the AC gain of the amplifier. A bypass capacitor is used to decrease the gain degenerating effects of R_E on higher frequencies (this will be explained in more detail in the simulation section).

By analysis of the circuit using the mesh method, it is possible to find expressions for the input and output impedances of this stage. The derivation of these equations was performed in lecture 16.

Input impedance:

$$Z_i = \frac{(r_0 + R_c + R_E)(R_B + r_\pi + R_E) + g_m R_E r_0 r_\pi - R_E^2}{r_o + R - R_E}$$

Output impedance:

$$Z_o = Z_x || R$$

$$Z_x = r_0 \frac{\frac{1}{R_E} + \frac{1}{r_{pi}+R_B} + \frac{1}{r_o} + \frac{g_m r_\pi}{r_{pi}+R_B}}{\frac{1}{R_E} + \frac{1}{r_{pi}+R_B}}$$

The Common Emitter has the drawback of having high output impedance. For that reason the Output stage is added as way of reducing the output impedance and to suplly more current to the load.

2.2 Output stage - Common Collector Amplifier

The output stage is comprised of a PNP transistor, a resistor and a capacitor.

This stage has a gain level of almost unity so it is not responsible for the amplification. The main purpose is to decrease the output impedance to work better with the 8*Ohm* load and allow larger currents to flow.

The capacitor is used to remove the DC component of the signal and only allow for the AC signal to reach the output terminals.

By analysis of the circuit using the node methos, it is possible to find expressions for the input and output impedances of this stage. The derivation of these equations was performed in lecture 17.

Input impedance:

$$Z_i = \frac{g_\pi + g_E + g_o + g_m}{g_\pi(g_\pi + g_E + g_o)}$$

This value is higher than the output impedance of the gain stage. Since both the stages are connected in series, they follow the voltage divider law. For that reason, to achive as large as possible gain, it is important that the output impedance of the gain stage is smaller than the input impedance of the output stage.

Output impedance:

$$Z_o = \frac{1}{g_{pi} + g_E + g_o + g_m}$$

This value is low so it can be connected to the load efficiently.

2.3 Circuit frequency response

Due to the use of capacitors in the circuit, the gain is dependent on the frenquecy of the imput. This response was achieved by calculating the equivelent impedance of the braches with capacitors for a set of frequencies.

2.4 Theoretical Results

The obtained results were as follows:

3 Simulation Analysis

In this section, Circuit T4 is reproduced with the help of Ngspice.

Ngspice is a simulator for eletronic circuits that can output a variety of results. This emulator computes the voltages in every node, as well as the potential difference between two given nodes. Apart from that, the group made use of the command *.options savecurrents* which also enables the use of the currents that pass through all branches. Moreover, function to help determine the maximum and interception of the plots were also used.

Firstly, the outcome of the simulation is shown, as well as a brief explanation on how it was achived. Afterwards, a comparison is done between those values and the ones attained in Section 2.

3.1 Simulated results

In this laboratory assignament, the Ngspice script made use of the sames values considered for the Octave script.

Table 2 dislpays the total impedances of the circuit (Input and Output). These are attained by dividing the potencial difference of the sinusoidal voltage source by the current that passes through it at a reasonble instant.

For the Outup impedance a small change in the circuit was done. The original sinusoidal voltage source is connected to the "out" node of the OP-AMP and Ground,a nd in its inicial position is now a short-circuit. Optimally this value should be as close to zero as possible, such is not verified because of the need to improve the Merit.

Name	**Value[Ohm]**
Zin	9.9022 + 0.00223195 j
Abs(Zin)	9.9022
Zout	522.442 + -316.233 j
Abs(Zout)	610.695

Table 2: Total impedance values from Ngspice.

Figure 2 displays vdb_{out} (in decibels) from 10Hz to 100MHz, as well as a constant ($max - 3(dB)$) - this helps to better visualize the passband. The vdb_{out} curve is characteristic of a band pass filter (cutting high and low frequencies).

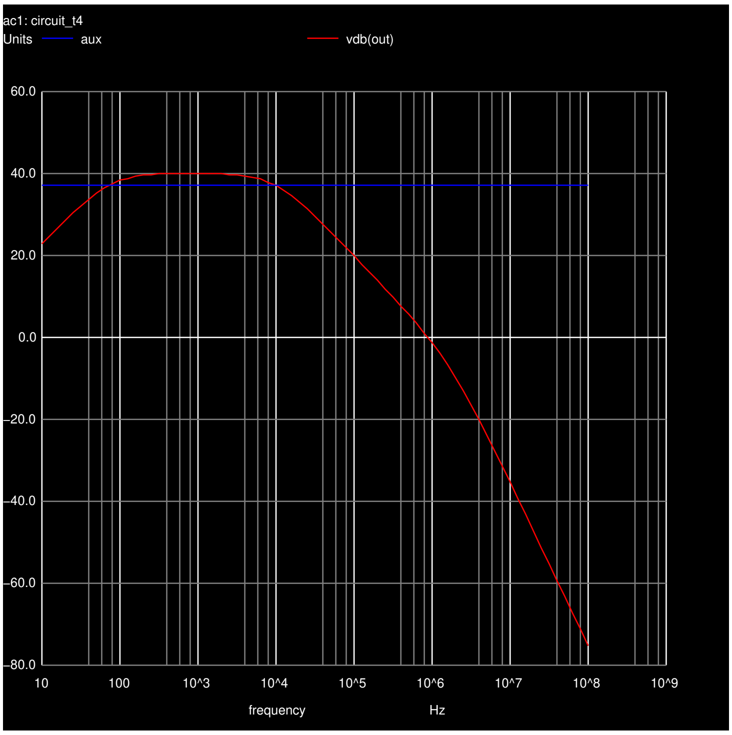

Figure 2: vdb_{out}

This graph is of particular importance because it allows us to obtain the GainDeviation. This is simply given by the absolute value of ($Maximum - 100$), 40db or 100 (linearly) being the Gain at central frequency. Therefore, the closest the maximum of said graph is to 40dB, the lower its deviation is and the higher the Merit will be. This variable has no units.

Moreover, with the plot in Figure 2, we were able to measure the Central frequency. This variable is given by:

$$CentralFreq = \sqrt{(}LowerFreq \times UpperFreq)$$

The *L*owerFreq and *U*pperFreq are the frequencies of the intersection points of the vdb_{out} curve and its max minus 3. Its deviation is *C*entralFreq-1000. This variable is given in Hertz (Hz).

Lastly, the group also used Ngspice to compute the Merit. Table 3 shows all the values necessary to compute the Merit, as well as the Merit itself. Note that the total cost is the sum of the costs of resistors, capacitors and transistors of the total circuit (including de OP-AMP).

Name	**Value**
cost	1.343451e+04
gain	1.003168e+02
gaindev	3.167835e-01
centralfreq	8.476811e+02
centralfreqdev	1.523189e+02
——–	————
merit	4.876656e-07

Table 3: Merit and other variables.

4 Conclusion

In order to perform theoretical and simulational analysis of the circuit Octave and Ngspice were used, respectively.

Theoretical methods were used to compute the gain, impedances and frequency responde of both of the stages. Contrary to past lab assignments the theoretical results differ a lot from the simulated results.

Comparing the frequency response graphs we can see that they are quite different. The most noticeable difference is that the theoretical method does not predict the higher cutoff frequency. This is explained by the fact that the theoretical method considers all the components to be ideal when in reality all of the components have some residual capacitive characteristics which can become noticeable at really high frequencies. In adition it is possible that the BJT model simulates the speed at which a transistor can be responsive.

The impedance and gain also differ differ significantly.

In conclusion, our simulated circuit was able to acheive a decent gain and Merit value and so we considered it a sucess. In addition we were able to understand the functioning principles of a class A amplifier but also were exposed to the difficulty of choosing parameters that optimize the results of complex circuits.