Circuit Theory and Electronics Fundamentals

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Laboratory Assignment - T4

Group nº59

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1 Introduction

The objective of this laboratory assignment is to create an audio amplifier circuit by choosing the architecture of the Gain and Output amplifier stages whilst optimizing the circuit on its Merit (M), that is given by the equation:

$$M = \frac{voltageGain \times bandwidth}{cost \times lowerCutoffFreq}$$

$$cost = cost_{resistors} + cost_{capacitors} + cost_{transistors}$$

$$cost_{resistors} = 1MU/kOhm;\ cost_{capacitors} = 1MU/\mu F;\ cost_{diodes} = 0.1MU/transistor$$

The circuit studied, displayed in figure 1 utilizes the following components:

- two voltage sources (V_1 and V_{cc})
- two transistors (Q_1,Q_2)
- six resistors (R_1, R_2, R_e, R_c, R_{in}, R_{out})
- three capacitors (C_i, C_b, C_o,)

Theoretical and simulation analysis are presented in Section 2 and Section 3, respectively, and the results of each are then compared. Finally, in Section 4 the conclusions of the laboratory assignment are outlined.

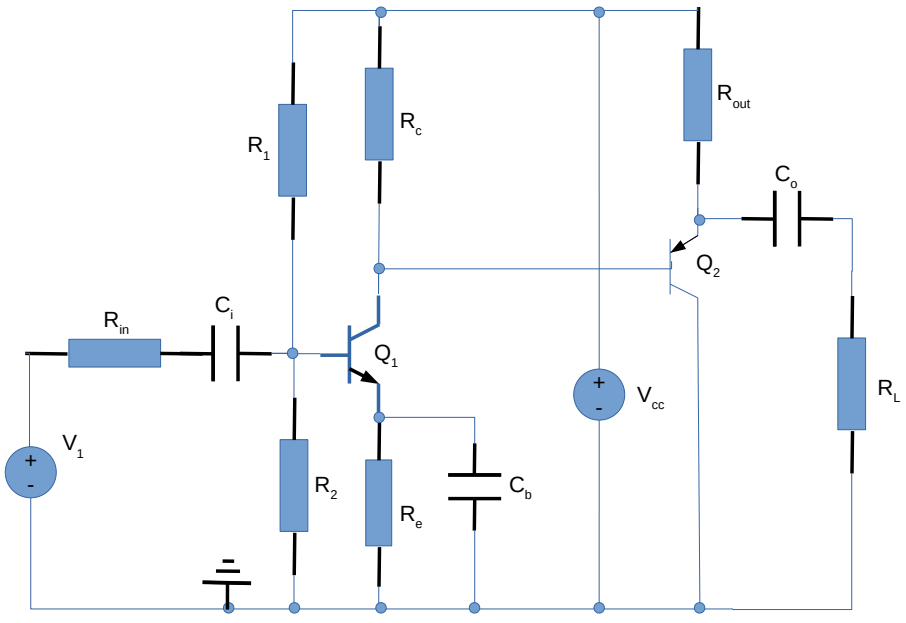

Figure 1: Circuit T4

2 Theoretical Analysis

In this section we will explain the inner workings of the class A audio amplifier created and perform a theoretical analysis of each component. The common Kirchoff laws and the simplified BJT equation were used to perform the analysis.

2.1 Gain stage - Degenerated Common Emitter Amplifier

It is in this stage of the amplifier that most of the signal amplification takes place. This stage is comprised of a NPN tansistor, two capacitors (coupling and bypass) and four resistors (two for the voltage divider, R1 and R2, one for the temperature stabilization RE and another to set the no signal current, RC).

The base voltage of the transistor needs to be forward biased in order for the NPN transistor to work in the forward-active region. For that reason, a voltage divider is added to make sure that the base voltage is always larger than 0.7V. A coupling capacitor is added between the voltage divider and the signal source in order to add the input AC signal to the voltage divider DC signal (this will be explained in more detail in the simulation section).

The resistor RC is used to set the zero signal current that passes trough the BJT.

The resistance RE adds temperature stabilization and removes the temperature dependency of the gain in the circuit but has the drawback of decreasing the AC gain of the amplifier. A bypass capacitor is used to decrease the gain degenerating effects of RE on higher frequencies (this will be explained in more detail in the simulation section).

By analysis of the circuit using the mesh method, it is possible to find expressions for the input and output impedances of this stage. The derivation of these equations was performed in lecture 16.

Input impedance:

$$Z_i = \frac{(r_0 + R_c + R_E)(R_B + r_\pi + R_E) + g_m R_E r_0 r_\pi - R_E^2}{r_o + R - R_E}$$

Output impedance:

$$Z_o = Z_x || R$$

$$Z_x = r_0 \frac{\frac{1}{R_E} + \frac{1}{r_{pi}+R_B} + \frac{1}{r_o} + \frac{g_m r_\pi}{r_{pi}+R_B}}{\frac{1}{R_E} + \frac{1}{r_{pi}+R_B}}$$

The Common Emitter has the drawback of having high output impedance. For that reason the Output stage is added as way of reducing the output impedance and to suplly more current to the load.

2.2 Output stage - Common Collector Amplifier

The output stage is comprised of a PNP transistor, a resistor and a capacitor.

This stage has a gain level of almost unity so it is not responsible for the amplification. The main purpose is to decrease the output impedance to work better with the 8 ohm load and allow larger currents to flow.

The capacitor is used to remove the DC component of the signal and only allow for the AC signal to reach the output terminals.

By analysis of the circuit using the node methos, it is possible to find expressions for the input and output impedances of this stage. The derivation of these equations was performed in lecture 17.

Input impedance:

$$Z_i = \frac{g_\pi + g_E + g_o + g_m}{g_\pi(g_\pi + g_E + g_o)}$$

This value is high so it can be connected to the gain stage efficiently.
Output impedance:

$$Z_o = \frac{1}{g_{pi} + g_E + g_o + g_m}$$

This value is low so it can be connected to the load efficiently.

2.3 Theoretical Results

Name	Value
Ve	1.093271e+00
Vc	9.912854e+00
Vce	8.819583e+00
$Vec2$	1.061285e+01

Table 1: Values from Octave.

Name	Value
$Z1_{In}$	7.822336e+02
$Z1_{Out}$	3.728356e+02
$Z2_{In}$	2.725047e+03
$Z2_{Out}$	2.653788e-01
Zt_{Out}	1.682064e+00

Table 2: Values from Octave.

3 Simulation Analysis

In this section, Circuit T3 is reproduced with the help of Ngspice.

Ngspice is a simulator for eletronic circuits that can output a variety of results. This emulator computes the voltages in every node, as well as the potential difference between two given nodes. Apart from that, the group made use of the command *.options savecurrents* which also enables the output of the currents that pass through all branches. Moreover, function to help determine de minimum, maximum and average of the plots were also used.

Firstly, the outcome of the simulation is shown, as well as a brief explanation on how it was achived. Afterwards, a comparison is done between those values and the ones attained in Section 2.

3.1 Simulated results

In this laboratory assignament, the Ngspice script made use of the sames values considered for the Octave script.

Lastly, the group also used Ngspice to compute the Merit. Table 5 shows all the values necessary to compute the Merit, as well as the Merit itself.

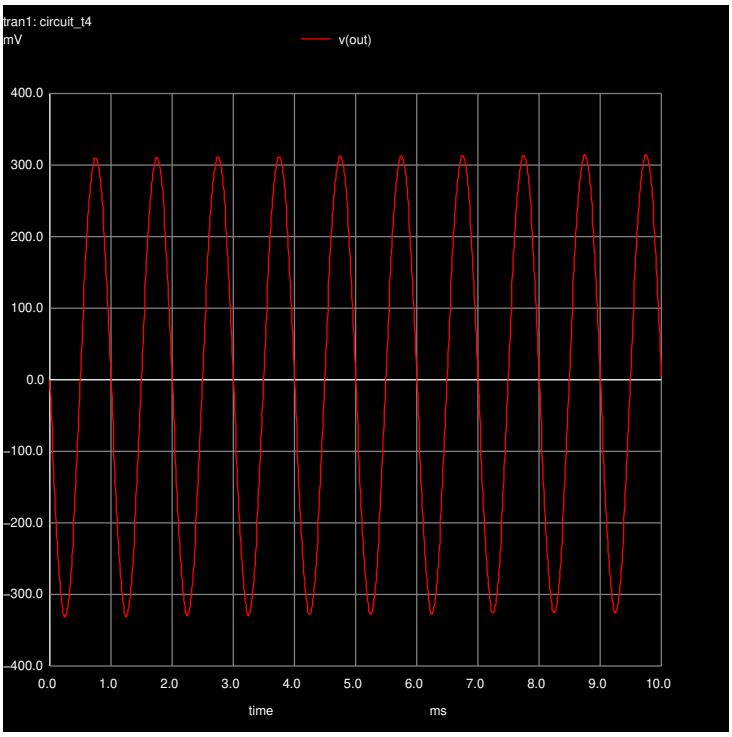

Figure 2: Inicial v_{out}

Name	Value
v(coll)	1.005359e+01
v(emit)	1.117079e+00
v(emit2)	1.086574e+01
v(emit2)-v(coll)	8.121456e-01
v(coll)-v(base)	8.244599e+00
v(coll)-v(emit)	8.936511e+00
v(base)-v(emit)	6.919123e-01

Table 3: Values from Ngspice.

4 Conclusion

In order to perform theoretical and simulational analysis of the circuit Octave and Ngspice were used, respectively. To obtain the theoretical values of the diodes, both Kirchhoff Laws and the V_{on} model were used. Then, in order to graphically obtain the value of V_0 over time, a plot was made and is shown in FIGURE 2. Posteriorly, with the simulation of the circuit we were able to make the same plot as before obtaining approximate results. Finally we proceeded to the optimization of the input values achieving the Merit shown before. Therefore, the objective of the laboratory was achieved succesfuly.

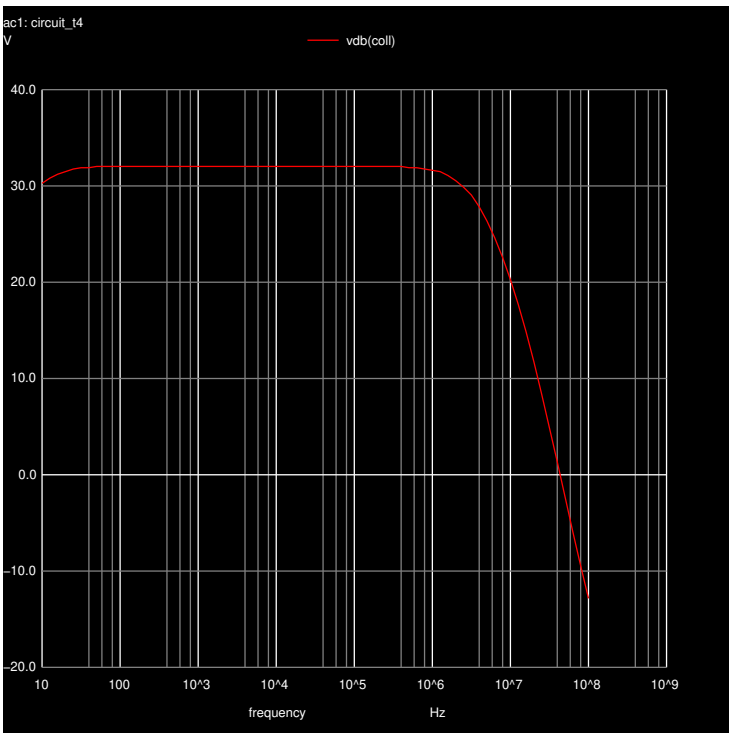

Figure 3: Envelope Detector Circuit v_{out}

Name	Value[Ohm]
Zin	923.912
Zout	3.49807

Table 4: Values from Ngspice.

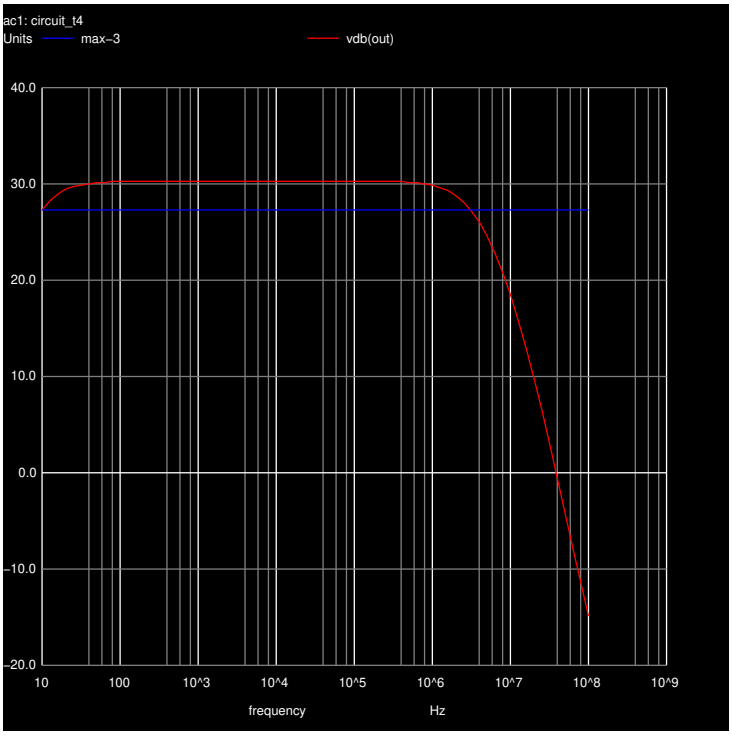

Figure 4: Voltage Regulator Circuit v_{out}

Name	Value
vgain	3.262849e+01
bandw	3.118611e+06
cost	8.160017e+03
lcof	7.972204e+00
———-	————
merit	1.564187e+03

Table 5: Values from Ngspice.