Circuit Theory and Electronics Fundamentals

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Laboratory Assignment - T4

Group nº59

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1 Introduction

The objective of this laboratory assignment is to create an audio amplifier circuit by choosing the architecture of the Gain and Output amplifier stages whilst optimizing the circuit on its Merit (M), that is given by the equation:

$$M = \frac{voltageGain \times bandwidth}{cost \times lowerCutoffFreq}$$

$$cost = cost_{resistors} + cost_{capacitors} + cost_{transistors}$$

$$cost_{resistors} = 1MU/kOhm;\ cost_{capacitors} = 1MU/\mu F;\ cost_{diodes} = 0.1MU/transistor$$

We ended up choosing the circuit displayed in figure **??** utilizing the following components:

- two voltage sources (V_1 and V_{cc})
- two transistors (Q_1,Q_2)
- six resistors (R_1, R_2, R_e, R_c, R_{in}, R_{out})
- three capacitors (C_i, C_b, C_o,)

Theoretical and simulation analysis are presented in Section 2 and Section 3, respectively, and the results of each are then compared. Finally, in Section 4 the conclusions of the laboratory assignment are outlined.

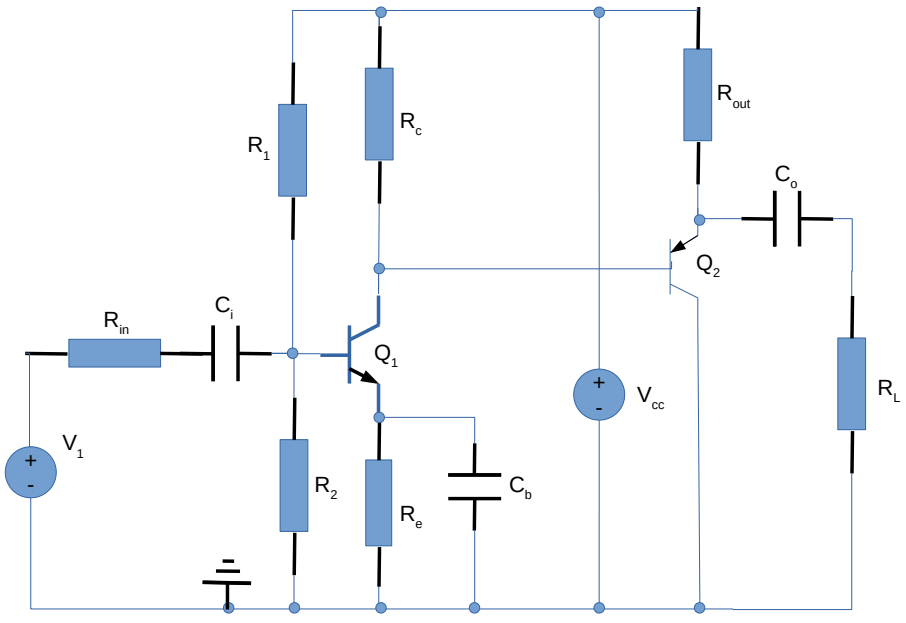

Figure 1: Circuit T4

2 Theoretical Analysis

In this section we will explain the inner workings of the AC/DC converter created and perform a theoretical analysis of each component. For the analysis it was assumed that each component only affects the components that come after it and so does not interfere with the previous analysis. The common Kirchoff laws and diode equations (simplified in some cases) were used to perform the analysis.

2.1 Transformer

The transformer is the component that steps down the supplied voltage. This step is necessary to approximate the supplied 230V to the 12V required. Since it was assumed that the transformer was ideal, its response can me modeled as a simples change in amplitude, that is related with the number of windings by the following equation:

$$V_{out} = \frac{V_{in}}{n}$$

2.2 Envelope Detector

The envelope detector is comprised of two sub-components: The rectifier and a filter. The chosen rectifier for our application was the Full-Wave Bridge Rectifier. The purpose of a rectifier is to turn the AC component of the supply to a DC current. To accomplish this objective the rectifier uses four diodes positioned in a way as to only allow the current to pass one way (shown in diagram). This behavior was achieved in octave by performing the abs() function to the signal and subtracting 2 times the diode's V_{on} voltage (simulating the two diodes the current has to pass through using the V_{on} model).

The filter is comprised of a series resistor and parallel capacitor. Its objective is to stabilize the signal and decrease the voltage ripples caused by the rectifier. This behavior was computed in matlab by comparing the signal voltage at each moment with the equivalent RC circuit voltage, the larger of the two was chosen to be the signal.

$$V_{out} = V_{t_{off}} \cdot e^{-\frac{t-t_{off}}{\tau}}$$

2.3 Voltage Regulator

This component has the objective of limiting the voltage to the desired value and at the same time, by using the non-linear behavior of a diode to decrease oscillations in the signal. The component is comprised of 17 diodes in series to achieve the desired voltage. Incremental analysis performed to find the final output signal.

By solving the following equation using the Newton-Raphson iterative method we can find the operating point voltage.

$$V_0 + R \cdot I_s \cdot (e^{\frac{v}{N \cdot VT}} - 1) - V_e nv = 0$$

Using this result we can find the equivelent resistance for the diodes using the following equation.

$$r_d = \frac{n\eta V_t}{I_s e^{\frac{V_D}{n\eta V_x}}}$$

With this information we can calculate by how much the ripple is decreased.

$$v_0 = \frac{r_d}{r_d + R} \cdot v$$

The output signal is the sum of the DC operating point calculated before and the ripple.

$$V_{out} = N \cdot V_{on} + v_0$$

2.4 Theoretical Results

Name	Value
Ve	8.992935e-01
Vc	3.057109e+00
Vce	2.157816e+00
$Vec2$	3.757109e+00

Table 1: Values from Octave.

Name	Value
$Z1_{In}$	8.064050e+03
$Z1_{Out}$	9.951958e+02
$Z2_{In}$	8.598855e+03
$Z2_{Out}$	3.021730e-01
Zt_{Out}	4.411395e+00

Table 2: Values from Octave.

3 Simulation Analysis

In this section, Circuit T3 is reproduced with the help of Ngspice.

Ngspice is a simulator for eletronic circuits that can output a variety of results. This emulator computes the voltages in every node, as well as the potential difference between two given nodes. Apart from that, the group made use of the command *.options savecurrents* which also enables the output of the currents that pass through all branches. Moreover, function to help determine de minimum, maximum and average of the plots were also used.

Firstly, the outcome of the simulation is shown, as well as a brief explanation on how it was achived. Afterwards, a comparison is done between those values and the ones attained in Section 2.

3.1 Simulated results

In this laboratory assignament, the Ngspice script made use of the sames values considered for the Octave script.

Lastly, the group also used Ngspice to compute the Merit. Table 5 shows all the values necessary to compute the Merit, as well as the Merit itself.

4 Conclusion

In order to perform theoretical and simulational analysis of the circuit Octave and Ngspice were used, respectively. To obtain the theoretical values of the diodes, both Kirchhoff Laws and the

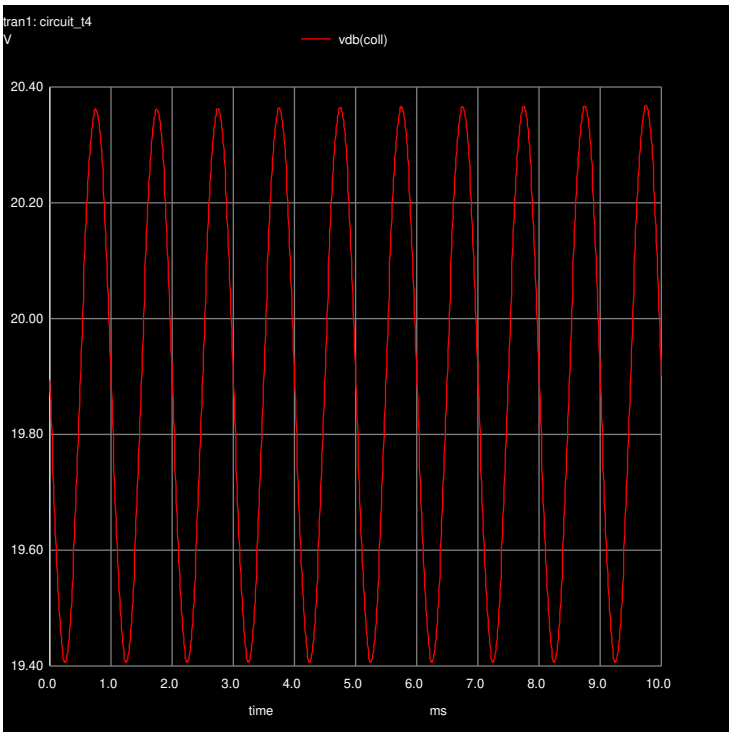

Figure 2: Inicial v_{out}

Name	**Value**
v(coll)	9.879492e+00
v(emit)	1.116248e+00
v(emit2)	1.057056e+01
v(emit2)-v(coll)	6.910627e-01
v(coll)-v(base)	8.071291e+00
v(coll)-v(emit)	8.763244e+00
v(base)-v(emit)	6.919530e-01

Table 3: Values from Ngspice.

V_{on} model were used. Then, in order to graphically obtain the value of V_0 over time, a plot was made and is shown in FIGURE 2. Posteriorly, with the simulation of the circuit we were able to make the same plot as before obtaining approximate results. Finally we proceeded to the optimization of the input values achieving the Merit shown before. Therefore, the objective of the laboratory was achieved succesfuly.

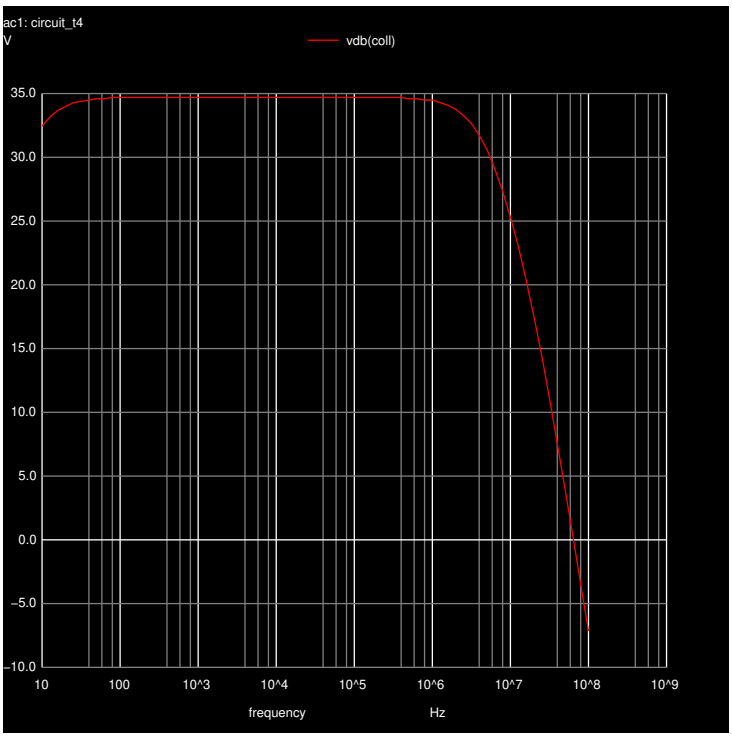

Figure 3: Envelope Detector Circuit v_{out}

Name	Value
zin	9.185934e-01,-1.25938e-01
zout	5.995573e+00,1.774281e-01

Table 4: Values from Ngspice.

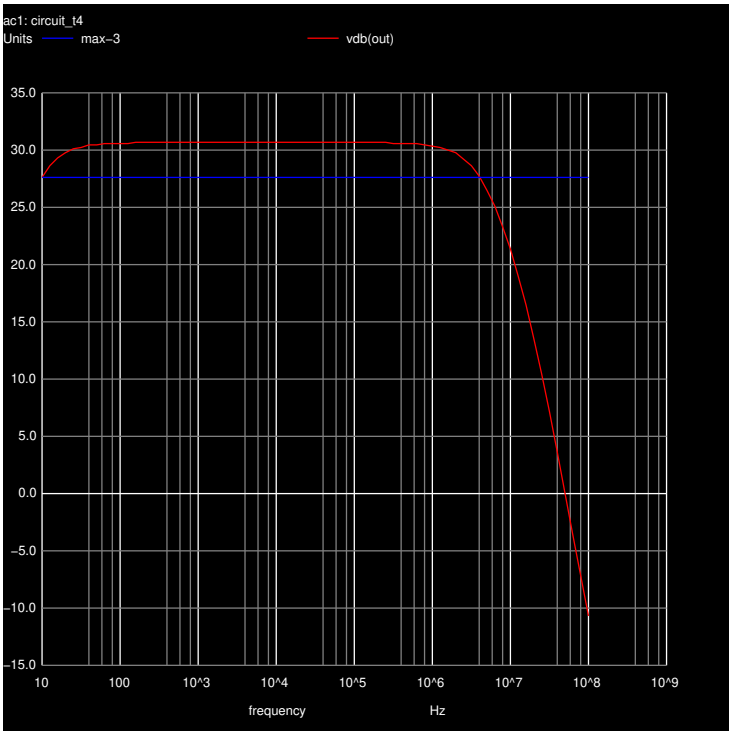

Figure 4: Voltage Regulator Circuit v_{out}

Name	Value
vgain	3.064597e+01
bandw	4.018859e+06
cost	1.058922e+05
lcof	8.036270e+00
———-	————
merit	1.447297e+02

Table 5: Values from Ngspice.