Laboratory practice 4

Sequential 4x4-bit multiplier

Objective

- Implement an iterative 4x4-bit multiplier:
  - To introduce the two operands we will use the switch bank.
  - We will use a ‘Start’ button and a ‘Done’ signal
  - The result of the multiplication will be shown in two 7-segment displays.

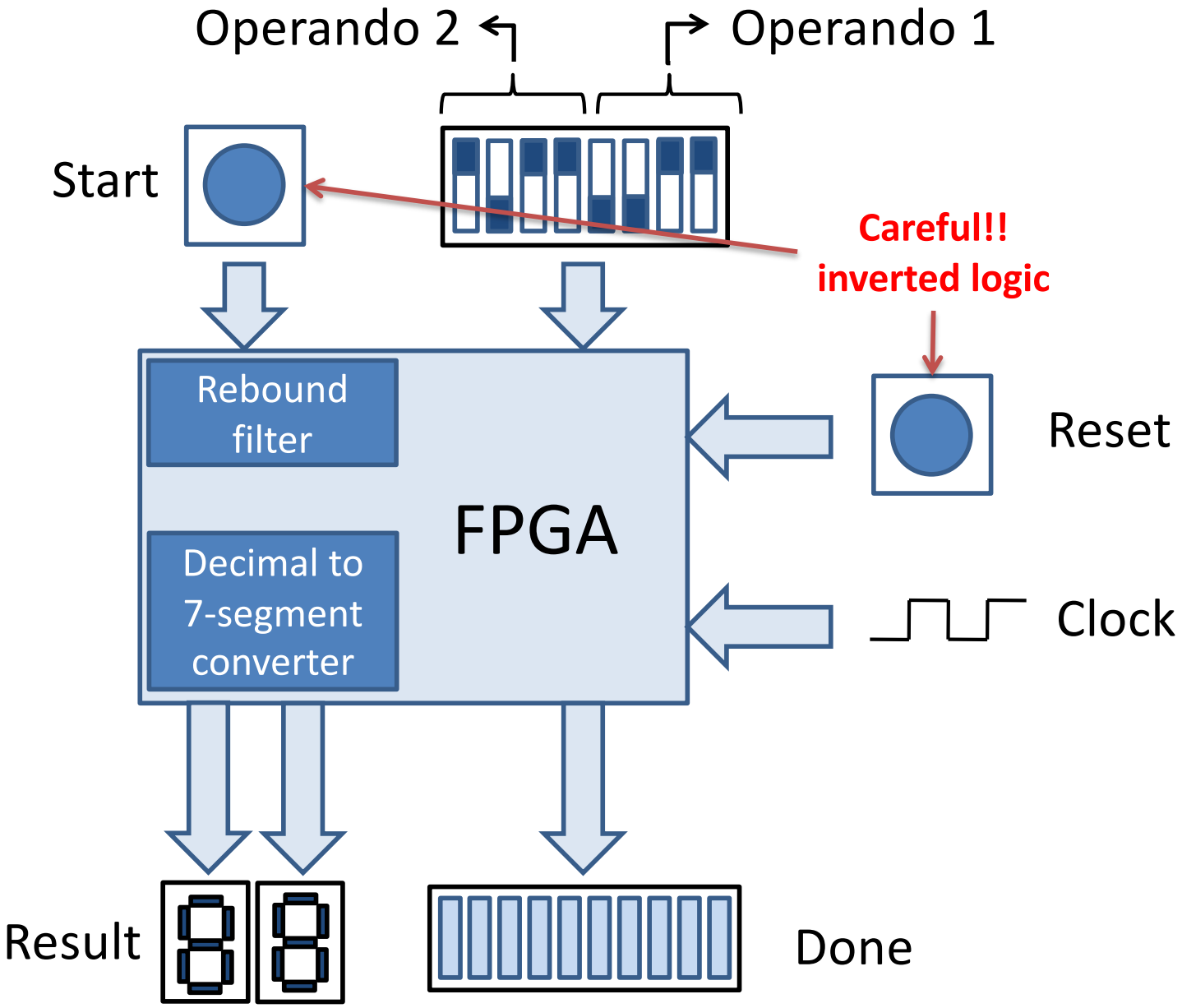
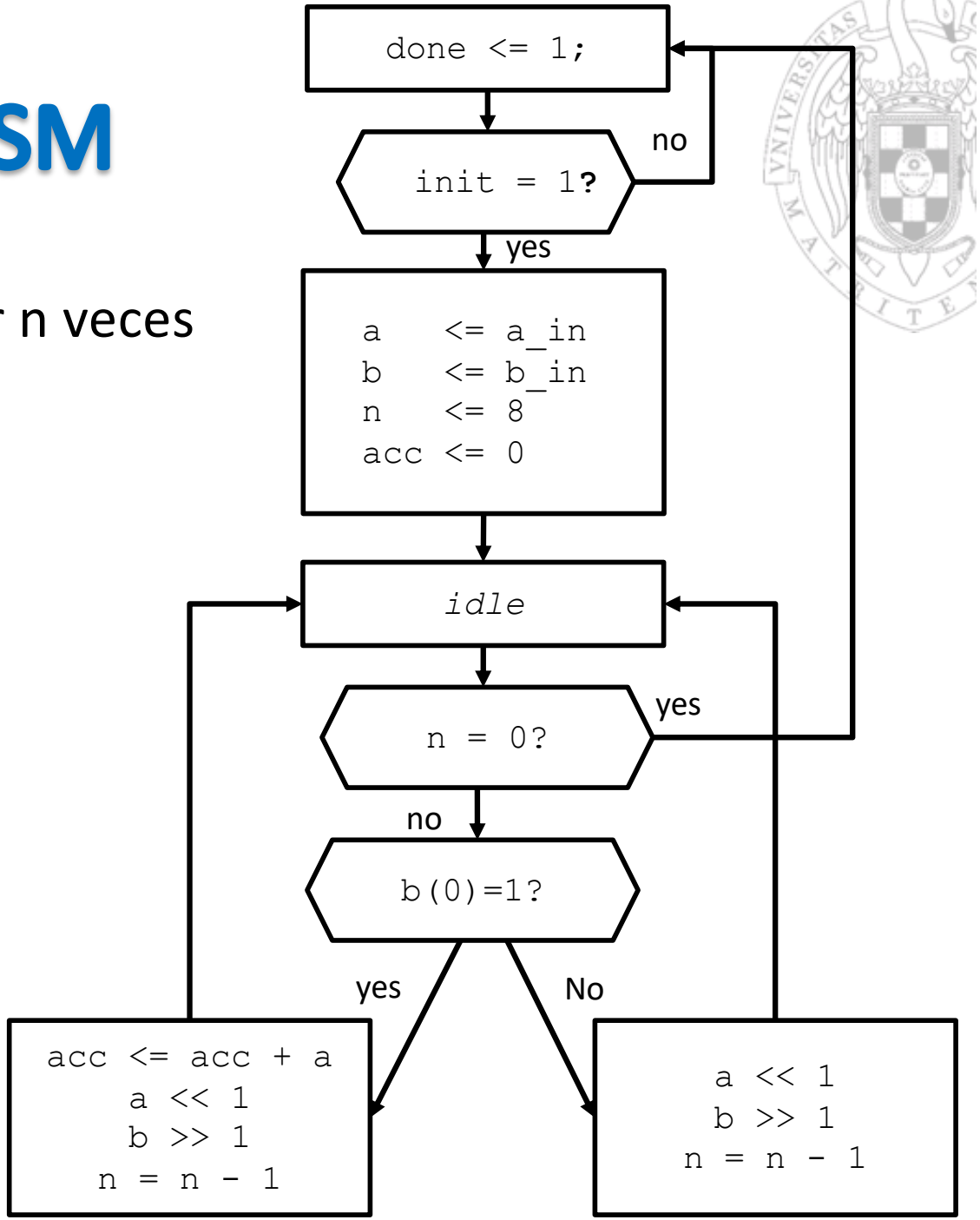

Operando 2
Operando 1
Start
Careful!!
inverted logic
Rebound
filter
FPGA
Decimal to
7-segment
converter
Reset
Clock
Result
Done

Diagrama ASM

- ASM multiplicador: sumar n veces

```
a   = a_in;
b   = b_in;
n   = 8;
acc = 0;

while( n > 0 ){
  if( b(0) == 1 )
    acc = acc + a;
  a << 1;
  b >> 1;
  n --;
}
```



Grading

- The student must go to the laboratory with the multiplier implemented and simulated as homework (use the test bench in the VC, **no modifications allowed**, yes, even the UUT name and interface).
- The student must show the multiplier working, and have to understand the implementation and functionality:
  - If it works properly in the FPGA, 0.2 pts
  - In case of just simulation working, 0.1 pts
- Advanced part 0.5 pts
- Laboratory practice 4 is **NOT** recoverable